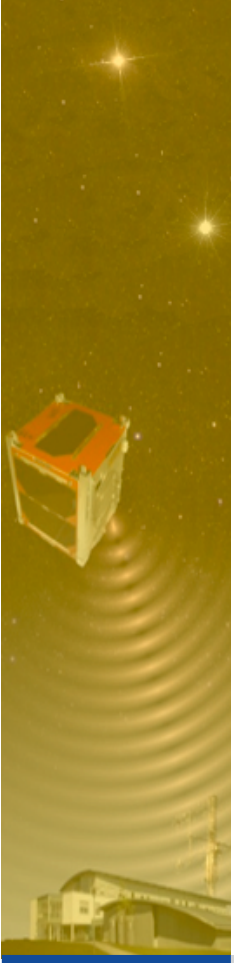

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One good test is worth a thousand expert opinions.

—WERNHER VON BRAUN

Abstract

Small satellites contribute significantly in the rapidly evolving innovation in space engineering, in particular in distributed space systems for global Earth observation and communication services. Significant mass reduction by miniaturization, increased utilization of commercial high-tech components, and in particular standardization are the key drivers for modern miniature space technology.

This thesis addresses key fields in research and development on miniature satellite technology regarding efficiency, flexibility, and robustness. Here, these challenges are addressed by the University of Wuerzburg's advanced pico-satellite bus, realizing a generic modular satellite architecture and standardized interfaces for all subsystems. The modular platform ensures reusability, scalability, and increased testability due to its flexible subsystem interface which allows efficient and compact integration of the entire satellite in a plug-and-play manner. Beside systematic design for testability, a high degree of operational robustness is achieved by the consequent implementation of redundancy of crucial subsystems. This is combined with efficient fault detection, isolation and recovery mechanisms. Thus, the UWE-3 platform, and in particular the onboard data handling system and the electrical power system, offers one of the most efficient pico-satellite architectures launched in recent years and provides a solid basis for future extensions.

The in-orbit performance results of the pico-satellite UWE-3 are presented and summarize successful operations since its launch in 2013. Several software extensions and adaptations have been uploaded to UWE-3 increasing its capabilities. Thus, a very flexible platform for in-orbit software experiments and for evaluations of innovative concepts was provided and tested.

List of Acronyms

MOSFET Metal Oxide Semiconductor Field-Effect Transistor 51

OAP Orbit Average Power 41

OBDH Onboard Data Handling 86

PCB Printed Circuit Board 24

PCU Power Cycle Unit 88

PPT Peak Power Tracking 43

PSA Pseudo Signature Analysis 94

RAM Random Access Memory 85

RBF Remove Before Flight 26

RSSI Received Signal Strength Indication 113

SAA South Atlantic Anomaly 71

SEB Single Event Burnout 74

SEE Single Event Effect 72

SEFI Single Event Functional Interrupt 75

SEGR Single Event Gate Rupture 74

SEL Single Event Latchup 74

SET Single Event Transient 75

SEU Single Event Upset 74

SPA Space PnP Avionics 22

SPE Solar Particle Event 71

SPI Serial Peripheral Interface 81

SWIFI Software Implemented Fault Injection 96

TID Total Ionizing Dose 72

TMR Triple Modular Redundancy 78

TWU Toggle Watchdog Unit 88

UART Universal Asynchronous Receiver Transmitter 25

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1

Introduction

The history of small satellites began in October 1957 with the successful launch of the first Earth orbiting spacecraft Sputnik I. With a total mass of only 83.6 kg the main technical success of the 58.5 cm sphere has been the prove that man-made technology can withstand the hostile space environment when orbiting Earth outside its protecting atmosphere. During its 21 days of active operation, Sputnik I was periodically transmitting radio signals to indicate internal pressure and temperature parameters. The signals could be received by world wide amateur radio operators until the batteries finally depleted and the satellite ceased operation. (Helvajian and Janson, 2008)

According to nowadays classification metric[1] for satellites with a total mass between 10 and 100 kg, Sputnik I has to be classified as a micro-satellite. A low number of even smaller nano-satellites with masses around 10 kg and less have been sent to orbit during the first years of space flight, but with increasing capabilities of launch vehicles also satellites became larger and more powerful. In the following thirty years, miniature satellites seemed to play only a minor role in space business until advances in miniaturization and emerging low-power micro-electronics initiated their renaissance in the late nineties (Bouwmeester and Guo, 2010).

Small satellites promise advantages compared to traditional large systems in several aspects. In fact, they can be built faster, they are cheaper and they can be launched together with other satellites. These aspects rendered small satellites not only attractive for space agencies, initiating related programs for technology demonstration, but also for educational university programs. Offering a similar level of multidisciplinarity at significantly reduced cost and development time, various academic institutions around the world initiated nano-satellite programs, targeting high quality training in the field of satellite engineering and

[1] A common classification metric subclasses small satellites (≤ 1000 kg) as mini ($100-1000$ kg), micro ($10-100$ kg), nano ($1-10$ kg), pico ($0.1-1$ kg) and femto (<0.1 kg).

project management in real space missions.

With the introduction of the CubeSat Design Specification in 1999, hands-on satellite engineering gained significant momentum at educational university programs. The standard defined by Jordi Puig-Suari (California Polytechnic Institute) and Bob Twiggs (Stanford University) in its recent version describes a set of minimal mechanical, electrical, operational and test requirements for a class of cubic pico- and nano-satellites. The great innovation of the CubeSat definition has been the mechanical and administrative decoupling of the spacecraft from the launch vehicle by the standardization of the satellites' launch interface for the Poly Pico-satellite Orbital Deployer (Swartwout, 2013).

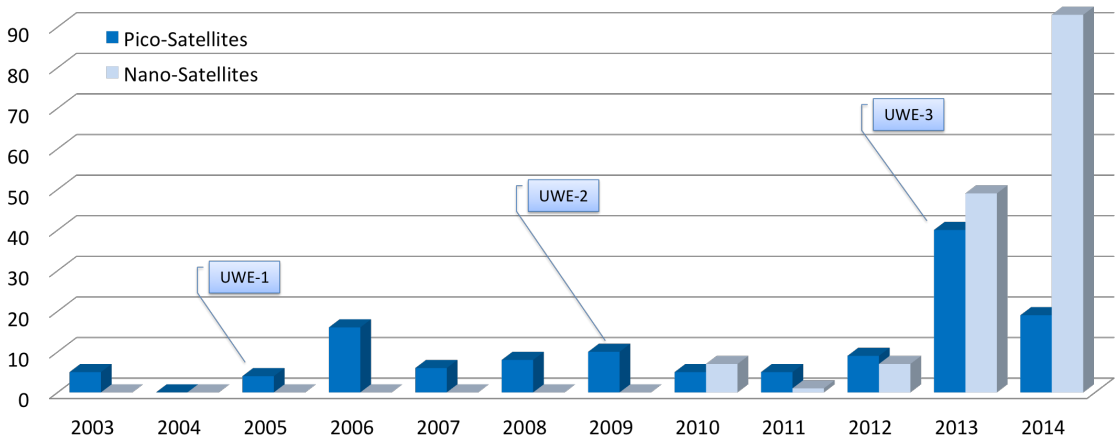


Figure 1.1: Pico- and nano-satellite launches between 2003 and 2014 with indicated launches of the University of Wuerzburg Experimental Satellites.

The flexible and cost efficient access to space promoted by the CubeSat standard paved the way for new players in space business and innovative mission concepts. Raising the acceptance for higher failure risks of an individual mission, the concept further promotes the employment of novel technologies to be tested in orbit. Thus, the CubeSat platform can effectively support early stage technology verification, providing valuable in-orbit performance data even for payloads with lower technology readiness level (Greenland and Clark, 2010). Since the first CubeSat launch in 2003, by now more than 280 pico- and nano-satellites have been brought to orbit by a diversity of launch vehicles (see figure 1.1). Projections for the upcoming years promise that this number will continue to grow rapidly (Buchen, 2014). The current trend indicates that pico- and nano-satellite launches already began to dominate launches of the micro-satellite class in the last years (Agasid et al., 2014).

1.1 Miniature Satellites - Chances and Challenges

Many parallels to the Sputnik I mission can be identified when looking at the capabilities of the first pico- and nano-satellites launched in the last decade. It is clear that the same design constraints which drive down cost and development time impose new challenges concerning resources available on miniature satellites. Restrictions in size and form factor not only call for increased miniaturization of subsystems and components, but further limit the surface area of the spacecraft available for solar power generation.

Limited size, mass, and power budgets are in general critical design drivers regarding processing, communication and attitude control capabilities, and can severely affect reliability due to the increased usage of commercial components with only little provision of redundancies. Reduced attitude control performance can further degrade the link budget, which, together with the absence of advanced groundstation networks, diminish the overall operational capabilities of miniature satellite missions.

However, ongoing research and development has been examining ways to overcome mentioned inherent limitations. Progressive miniaturization, energy efficient hardware designs, advanced deployable structures and increased onboard autonomy are important factors to continue the enhancement of functionalities, especially for pico-satellites. Nevertheless, some hard physical limits might remain insuperable for small scale spacecraft. For example the resolution of an optical payload depends strongly on its aperture size while the performance of a radar system for Earth observation is dictated by the irradiated power in order to take account of the implied path loss (Selva and Krejci, 2012).

For some applications small satellites will never become competitive with larger spacecraft missions and might only play a complementary role. For many other applications, size and mass limitations do not constitute a limiting factor anymore. The current trend indicates that more and more miniature satellite missions start to tackle valuable science questions (Jones, 2014). A review of current and past small satellite applications by Woellert et al. (2011) highlights the rapidly evolving maturity of small satellite technology as a science and technology platform. Up to now, this potential is not yet fully utilized. As a survey conducted by Selva and Krejci (2012) which assesses the current capabilities of CubeSats shows, a variety of technologies with the potential to provide valuable scientific return in the field of Earth observation is already available to be employed on future small satellites missions.

It seems obvious, that small satellite systems will become the key enabling technology for the realization of large constellations or formations of cooperating spacecraft. Distributed space systems are attractive due to their advantages regarding reliability and

performance in many applications. In general, they can offer increased temporal and spacial coverage while providing the capability for incremental upgrading of functionality as well as graceful degradation in case of single spacecraft failures. In particular, the combination of data from multiple perspectives opens the door for a variety of sophisticated measurements such as synthetic aperture interferometry or tomographic reconstruction of three-dimensional targets. Still, immense launch and development cost related to traditional satellite systems constitute a limiting factor for distributed space systems. Miniaturization, mass production techniques, and the capability to deploy a large number of spacecrafts with a single launcher promise cost-efficient and rapid installation of even larger constellations by using capable miniature satellites. A future-oriented example for the commercial potential of distributed small satellite missions might be the Flock constellation of the young company Planet Labs (Butler, 2014). After three cluster launches in 2014, the Flock constellation comprises about 70 Earth-imaging nano-satellites in low earth orbits.

However, despite its great potential to initiate a paradigm shift in modern space flight, miniaturized satellite technology is still in its infancy. In the last decade, a large number of pico- and nano-satellites have been launched by a diversity of university and industrial programs, but by far not all missions could demonstrate successful operation in orbit. In fact, it is not trivial to assess the actual failure rate objectively as sometimes only little information about mission objectives and results is publicly available. Some attempts have been made to investigate the in-orbit performance of launched miniature satellites. A survey by Bouwmeester and Guo (2010) incorporating 94 pico and nano-satellites launched until mid 2009 revealed that only about half of the missions that reached orbit reported full mission success. The comparably high failure risk might explain why the majority of pico- and nano-satellite missions intends or accepts a relatively short target lifetime as reported in the survey.

According to a more comprehensive study by Swartwout (2013), evaluating the in-orbit performance of all pico- and nano-satellites launched between 2000 and 2012, more than 40 % of the CubeSats that reached orbit finally failed to meet their basic mission objectives. Many of the failing satellites did not survive launch and first hours in orbit such that contact could never be established. More than half of the failing satellites were operational for some time before reporting technical issues related to power, communication, mechanics, or the flight processor. Typical failure sources reported include insufficient power generation and unrecoverable processor errors. However, Swartwout concludes that, beside raised attention to thermal design aspects and the inherent risks connected to the utilization of commercial-of-the-shelf components, many failures could have been avoided by more elaborate system-level functional testing.

The study further indicates that university lead missions, which mainly represent the single unit pico-satellite sector, show a significantly higher failure rate compared to industrial led missions, mainly employing larger nano-satellites. Doubtlessly, this can be partially explained by monetary and personnel reasons connected to the disparate natures of educational and commercial missions. Another explanation for the increased failure rate might come along with the specific limitations of a pico-satellite compared to a larger nano-satellite, which typically provides more than three times the volume, mass, and power while relying on the same hardware components. On the one hand the increased necessity for tight integration can severely complicate functional integration testing, which evidently impacts the system's reliability. On the other hand extreme budget constraints limit the option for fault-tolerance enhancement with redundant hardware. A nano-satellite might be able to include redundancy on system level by doubling complete subsystems. This is not easily possible for a one-kilogram system. In fact, only a few subsystems available on the market include inherent redundancy on a single board design, while most commercial devices already use up a significant amount of the power available on a pico-satellite. Thus, many pico-satellite designs just hit the limit of their mass and power budget, even without the extensive provision of backup hardware.

Besides technical challenges due to the extremely limited mass and volume, pico-satellite projects at university level inherently involve challenges due to high student fluctuation together with significant launch delays and limited financial budgets. While a typical pico-satellite project lasts a few years, the active contribution of a student team member is in the order of a few months only. Experiences from more than ten years of educational satellite projects at the University of Wuerzburg show this circumstance causes difficulties concerning project management and quality assurance (Busch et al., 2013b), also for similar academic programs (Birkeland and Gutteberg, 2013). The risk connected to a generation change in the project team is not only the loss of expertise related to a particular component developed, but also the loss of a responsible person ensuring functionality of the inherited developments until actual launch date and beyond. In order to ensure feasibility and continuity of an academic satellite program over long time, special care in the engineering process, especially during soft- and hardware design, integration, and testing, has to be taken.

Since the beginning of this work in early 2009, a clear trend towards the increased utilization of miniature satellites for more and more valuable technical and scientific missions can be recognized. Progress has been made in many technical aspects, rendering miniature spacecraft more and more capable and competitive. Mission concepts targeting scientific objectives beyond low Earth orbits are already on the horizon. Nevertheless,

looking at the continuing trend [2] of relatively short operation times, it must be clear that some challenges still remain. Despite all advantages connected to low cost and high performance of modern micro electronics, one should not lose sight of traditional challenges regarding reliability and durability, especially in the pico-satellite sector.

1.2 The UWE-3 Project

The vision of formations of cooperating pico-satellites seems to be realizable in near future. The University of Würzburg established a roadmap targeting the technology development for the realization of small satellite formations within this decade. The University of Würzburg Experimental satellite (UWE) program was born with the successful launch of UWE-1 in 2005. The first German pico-satellite had the main objective to establish a robust communication link to the ground segment (Barza et al., 2006). Four years later UWE-2 was launched, aiming to demonstrate the capabilities of pico-satellites in the field of attitude determination as an extension of the UWE-1 platform (Schmidt et al., 2009). Due to the nature of the standard components based design with only little redundancies the lifetime of UWE-1 and UWE-2 was limited to a few weeks only.

With the third generation of UWE satellites for the first time a modular and flexible design of the pico-satellite bus was introduced to constitute a robust and generic platform for future UWE missions. The main educational and technical objectives of UWE-3 were defined as:

- Multidisciplinary education of students in real practical satellite engineering and operations.
- Establishing a robust base for future UWE satellites by featuring an advanced modular and flexible architecture of the pico-satellite bus in order to increase reusability, testability, and reliability on the overall system design.
- In-orbit demonstration of a low-power coarse attitude determination and control system as a crucial milestone targeting future pico-satellite formations.

The UWE-3 project has been officially initiated in August 2009 and has been supported by the German national space agency with funding by the federal ministry of economics and technology.

[2] By August 2014, the TUB Small Satellite Database (Buscher, 2014) assigns about 42 % of the 26 small satellites launched together with UWE-3 in late 2013 the status *not active* (31 % *active*, 27 % *unknown*).

1.2.1 General Approach

As its predecessors the UWE-3 pico-satellite adopts the single unit CubeSat standard in order to benefit from frequent and cost-efficient launch opportunities. Its technology mainly relies on commercial standard components due to their significant advantages in cost, availability and performance while minimizing mass, size and power requirements. In order to approach mentioned limitations and challenges coming along with miniaturized spacecraft engineering in the context of educational projects, the soft- and hardware design of the UWE-3 pico-satellite bus is mainly driven by three key components: *flexibility*, *robustness* and *efficiency*.

In the present context, the term *flexibility* refers to the property of an architecture to be easily modified or extended in order to suit future requirements. With the goal to provide a generic satellite platform suitable for future UWE missions a modular bus architecture has been targeted. The functional separation of modules with small and clear interfaces promotes reusability, maintainability and extensibility as components can be designed, tested and upgraded more independently. A modular and flexible bus further supports reliability as well-defined interfaces help to reduce system complexity and facilitate system integration, thus promoting early functional integration testing.

Robustness can be defined as reliable and fault-tolerant operation. Thus, the term describes the ability of a system to accomplish its designated operations during its intended lifetime under normal conditions (*reliability*) and to continue at least reduced operations in the event of the failure of some of its components (*fault-tolerance*).

A proven approach to achieve *reliability* is to privilege simple designs when possible while enforcing unit, integration, and system level verification to ensure functional performance in a large variety of test scenarios. In the optimal case these screenings continuously accompany the entire engineering process in order to verify and maintain desired functionalities of accomplished components and to reveal compatibility issues as early as possible in the design phase. Automated screening procedures can significantly ease and accelerate extensive test campaigns. Thus, they promote frequent conduction of quick unit checkouts or more complex integration self-tests, but also long-term verification experiments on system level. In order to enable and establish the automation of those procedures it is essential that their implementation is supported by the inspected object itself, a design requirement which is often referred to as *design for testability*.

In the present context, *hardware testability* could mean that a functional test configuration can be rapidly set up. The design might further provide access to an adequate selection of electrical test signals even in a functional or tightly integrated configuration of the sys-

tem. Whenever possible, a hardware design should provide for self-monitoring capabilities such that important test indicators are directly feed back to embedded microcontrollers onboard the subsystem to be accessible by internal software. Similarly, *software testability* would require the comfortable access to run-time debug information. The provision of powerful testing libraries and analysis tools can further contribute to enhance software testability.

Some test procedures might require specific external test facilities, such as environment simulators, which generate specific inputs required in order to verify the system's functionality. Despite the challenges imposed by the extremely limited mass and volume of pico-satellites, exactly these properties are very advantageous when it comes to testing as the low weight or power consumption of the miniature satellite allow to design test setups which are much simpler, more compact, and much more cost-efficient than typical test environments of larger spacecraft. Whenever possible, these facilities should support automated test procedures, for example by following common protocols for control and monitoring.

Similar to testability, also *fault-tolerance* usually requires specific design measures to guarantee a certain level of reliability in case of unexpected component failures. In the case of the UWE-3 satellite project fault-tolerance is mainly accomplished by redundancy and failure detection, isolation, and recovery techniques. Assuming that most failures are not inherently destructive, they can be recovered for example by power cycles, as long as key components remain operational such that advanced recovery procedures can be initiated. Thus, as also addressed by Shirasaka and Nakasuka (2011), at least the key components have to be implemented robustly. In particular this applies to the onboard computer, the electrical power system, and the communication system, as their operability guarantees a minimal configuration which would enable access from the ground segment. However, redundancy should be implemented in a compact fashion inside a subsystem rather than doubling the device on the satellite bus as this would in most cases require excessive space. Whenever possible, redundancy should be carried out in a way that redundant units can be operated in parallel, thus adding performance in nominal operation, and degrading gracefully in case of single component failures.

The term *efficiency* describes in general a performance optimization with respect to some valuable resources, such as energy, mass, space, or cost. Thus, efficiency is the key ingredient for miniaturized spacecraft design. On one hand, efficiency can support flexibility and robustness. For example, a space, mass, and power optimized satellite bus allows to include more future extensions. Likewise, a large power budget margin can certainly contribute to robustness. On the other hand, measures targeting flexibility and

robustness might significantly degrade efficiency. In fact, redundancy usually contributes to power, mass, and space requirements and miniaturized components are quite often more vulnerable to radiation effects. Furthermore, a general modular standard can never be as efficient as an optimized design for a single application. Thus, the efficiency requirement has to be carefully traded off against desired flexibility and robustness of the design.

1.2.2 UWE-3 Satellite Bus Overview

The modular UWE-3 bus supports rapid development, integration and testing of the satellite as well as simple maintenance, extension and replacement of subsystems in any configuration during flat-sat development or flight model integration. An overview of the UWE-3 pico-satellite bus is given in figure 1.2. In order to achieve a consistent realization of the mentioned aspects all subsystems of the satellite have been developed in the context of the UWE-3 project. The UWE-3 bus features a dual-redundant low power onboard computer (OBDH), a redundant and scalable distributed electrical power system (EPS), a fully redundant UHF communication system (COMM) and an attitude determination and control system (ADCS) being capable of operating continuously on the small-scale pico-satellite.

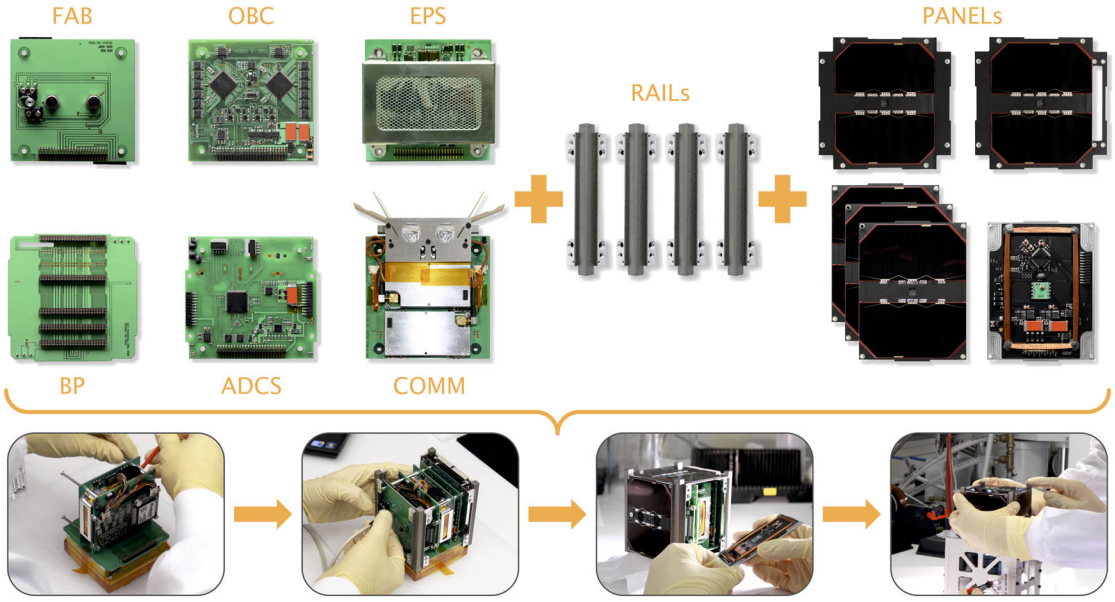


Figure 1.2: Overview of the modular UWE-3 pico-satellite bus being optimized for rapid integration and testing.

Modular Architecture

Based on a generic backplane (BP+FAB) implementing the entire harnessing no additional wiring between the subsystems is necessary. The standardized backplane provides a redundant set of digital communication and analog power lines as well as dedicated control signals to support a broad range of potential subsystems. The resulting electrical inner structure is fully functional, independent of any further structural component. A set of four hollowed rails (RAIL) mounted to the inner structure defines the mechanical interface to the standardized deployment adapter and further constitutes the connection between the inner and the outer structure. The outer structure consists of six similar solar panels (PANEL) which are just plugged to the backplane and mechanically fixed to the rails. Being composed of a double sided printed circuit board with aluminum core the multifunctional panel design combines structural stability, thermal balance, radiation protection, antenna ground plane, and electronics such as the magnetic torquers in an integrated compact and lightweight design. The modular design has been first presented in (Busch and Schilling, 2010) and is described in more detail in (Busch and Schilling, 2012). Experiences obtained during integration, test, launch and in-orbit operations are addressed in (Busch et al., 2013b) and (Busch et al., 2014b).

Onboard Computer

The OBDH core module plays a central role in the design of the UWE satellite bus as it is the only subsystem continuously operating as a dedicated housekeeping module. Thus, the design is optimized with respect to robustness and energy efficiency. The core module is build around two redundant ultra low power microcontrollers. A dynamically decided master-slave configuration enables the instantaneous master module to maintain and re-program the (even unresponsive) slave via its embedded emulation module. Thus, the core module implements mutual flash protection and recovery to increase robustness against radiation induced single event effects in utilized COTS technologies. With less than 10 mW nominal power consumption the design belongs to the most efficient redundant onboard computers available for pico-satellites. Relevant soft- and hardware aspects as well as first test results have been published in (Busch and Schilling, 2013) and first in-orbit operation experiences are outlined in (Busch et al., 2014b).

Electrical Power System

The electrical power system implements two fully redundant power paths for solar power generation, high capacity storage, and voltage conversion to provide most common bus

voltages on the standardized subsystem interface in a robust and efficient way. The system's partially distributed architecture assures that its performance can scale with different satellite configurations and mission scenarios. First results regarding design, test and in-orbit performance have been published in (Busch and Schilling, 2010), (Busch et al., 2013b) and (Busch et al., 2014b).

Communication System

The communication system is build around two separate commercial UHF transceiver modules located on a single subsystem board (see figure 1.3, left) whereas the cold redundant transceivers can be monitored and controlled independently. The board further accommodates two independent omnidirectional monopole antennas. During launch, the antennas are stowed in a box inside the satellite on the communication board in order to be deployed after arrival in orbit. This way, the antenna system is closely coupled to the communication system itself. This configuration simplifies the wiring and antenna matching and further enables extensive testing of the final flight configuration already on subsystem level. Moreover, this configuration enables easy access for maintenance or replacement of the communication system as a whole.

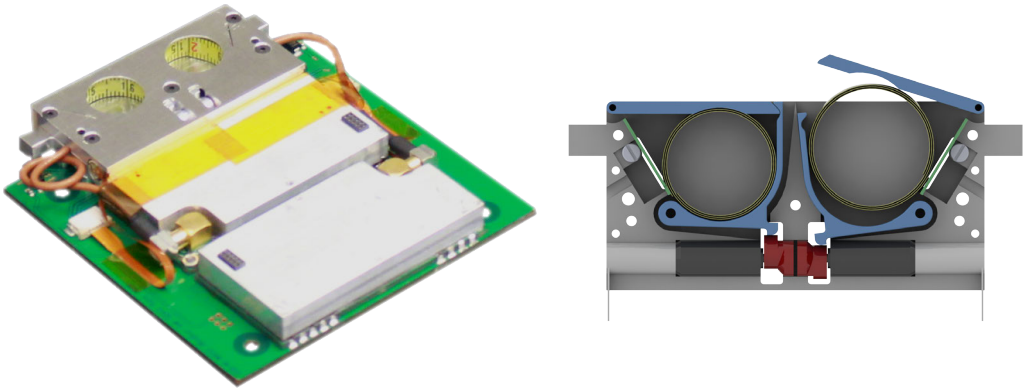


Figure 1.3: Redundant and compact UWE communication subsystem (left). CAD drawing of the non-destructive antenna deployment mechanism with top cover removed (right).

Special focus was put on the design of the deployment mechanism itself. In accordance with the general UWE engineering philosophy also the deployment mechanism was designed to support simple and elaborate testing throughout the entire development cycle of the satellite, especially after integration. For this reason, a non-destructive hold down and release mechanism has been developed. The repeatable mechanism ensures reproducible test conditions for a large number of deployment tests without the need for replacement of

any one-way parts destroyed during antenna release. Thus, the engineering model could demonstrate more than 100 consecutive successful deployments in normal atmosphere and in various thermal vacuum tests. Even the flight model antenna system demonstrated its performance during hot and cold case thermal vacuum tests and after extensive vibration tests during qualification.

A more detailed overview of relevant design aspects of the communication system and the antenna deployment mechanism can be found in (Busch et al., 2013a).

Attitude Determination and Control System

The attitude determination and control system has been optimized for continuous low power operations within the limited resources of a pico-satellite. The hardware implementation comprises a central core module which is implemented as a standard subsystem and a spatially distributed sensor and actuator suite embedded on the satellite's side panels.

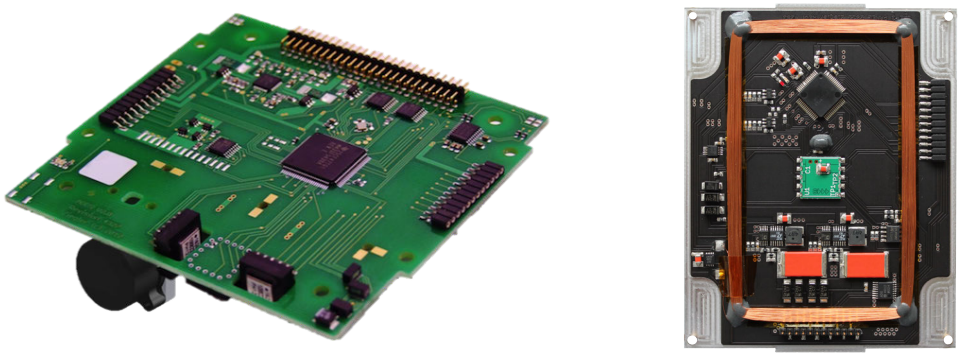


Figure 1.4: Attitude determination and control core module with gyroscopes, magnetometers and a single miniature reaction wheel (left). Backside of a satellite side panel with mounted magnetic torquer, sun sensor and single axis magnetometer (right).

For attitude determination the design combines measurements from nine single-axis magnetometers, three single-axis MEMS gyroscopes and six two-angle sun-sensors in an isotropic Kalman filter. As it can be seen in figure 1.4 a set of three orthogonal gyroscopes and three orthogonal magnetometers is directly located on the core module itself inside the satellite while each of the six satellite side panels further carries a sun direction and intensity sensor as well as an additional single axis magnetometer.

Implemented on an ultra low power microcontroller the Kalman filter is capable of performing quaternion estimations in real-time using optimized SGP4, IGRF and SUN reference model implementations. During nominal operations the system consumes less than 60 mW and can provide an attitude estimation accuracy in the order of a few degrees.

The system further controls the satellite's attitude using six independent magnetic torquers and a single miniaturized reaction wheel which can be used for fast slew maneuvers. The magnetic torquers have been designed to optimize power consumption, mass, space and the produced magnetic moment. Thus, with only 80 mW power consumption a single torquer is designed to provide a magnetic moment of $0.028\,\mathrm{Am}^2$ resulting in a combined torque of up to $4.6 \cdot 10^{-6}\,\mathrm{Nm}$.

The design of the attitude determination and control system as well as specific hardware-in-the-loop test environments have been published in (Kiefel et al., 2011) and (Bangert et al., 2012). Ground testing results are described in (Reichel et al., 2013) and (Busch et al., 2013a) while first in-orbit performance analysis is outlined in (Bangert et al., 2014) and (Busch et al., 2014b), and is further elaborated in (Busch et al., 2014a), (Bangert et al., 2015), and (Busch et al., 2015).

1.2.3 Launch and Mission Operations

Following flight model integration and qualification in March 2013, UWE-3 was launched on Nov. 21st at 07:10:11 UTC on board a Dnepr rocket from Yasny launch base located in Russia (see figure 1.5). It was contained in a triple unit ISIPOD[3] together with the satellites First-MOVE and VELOX-PII and was successfully released 937 seconds after lift-off into a nearly sun-synchronous polar orbit at about 650 km altitude. Its first pass over Würzburg ground station occurred at 08:46:25 UTC with a maximum elevation of 11 degrees during which first telemetry could already be received. The health status of the satellite was very good and batteries were almost fully charged. Within the first months of operations all subsystems and redundancies have been tested, both antennas have been successfully deployed and communication with ground could be established with both radio configurations.

UWE-3 has been successfully operated in orbit far beyond official end of the project in September 2014. Numerous experiments in the field of link quality analysis and attitude determination and control have been conducted whereas software updates allowed to continuously extend the satellite's capabilities in orbit. Most important results and lessons learned during satellite commissioning and mission operations have been published in (Bangert et al., 2014), (Busch et al., 2014b), (Busch et al., 2014a), and (Busch et al., 2015).

[3] CubeSat deployer developed by ISIS (ISIS, 2011)

Figure 1.5: Certificate of launch accomplishment for Dnepr Cluster Mission 2013 as issued by ISC Kosmotras, Russia.

1.3 Thesis Outline

A wide area of interdisciplinary topics have been addressed in this project and several contributions in the field of miniature satellites have been documented in various publications as indicated in the previous sections. Even though these publication constitute the base of this thesis not all of them found their way into this work as a separate section. Nevertheless they are deeply related to the main subject of this thesis, and might possibly serve as sources of further information. The following chapters will focus on selected aspects and architectures related to the core functionality of the UWE-3 satellite bus, with special emphasis on flexibility, robustness and efficiency of the related concepts and implementations.

Following this introduction to miniaturized spacecraft engineering in the context of the UWE-3 project, chapter 2 is devoted to the modular and flexible pico-satellite bus of UWE-3 . After a brief summary of related work concerning modular satellite concepts, the chapter describes the implemented architecture in detail. Experiences with the platform in the satellite engineering process, in particular during development, integration, and test campaigns are presented in order to illustrate the system's advantages in the context of an educational pico-satellite project.

Chapter 3 is dedicated to the satellite's flexible and redundant electrical power subsystem which seamlessly integrates into the modular plug-and-play design of the UWE-3 architecture. After outlining specific challenges connected to electrical power systems of miniature spacecraft a selection of available devices for pico- and nano-satellites is presented. The new concept and implementation of the UWE-3 system is elaborated in detail. The chapter completes by presenting specific test setups and performance results obtained during extensive verification tests of the system.

The robust and energy-efficient onboard computer of UWE-3 is treated in chapter 4, starting with an overview of radiation effects and common mitigation techniques as a main concern regarding the utilization of customary microelectronics in space environment. Following a review about state-of-the-art onboard computers for pico- and nano-satellites, the focus is placed on the concept and implementation of the corresponding hard- and software of the UWE-3 onboard data handling core module. The chapter concludes by presenting experimental results from extensive software implemented fault injection tests carried out to verify the system's performance before launch.

Chapter 5 compiles relevant results obtained during the first year of mission operations. General in-orbit performance of presented technologies is analyzed from telemetry data obtained during first months of operations. Further, a comprehensive uplink performance

experiment is described in detail and measures taken to optimize mission operations efficiency are discussed. The chapter closes by summarizing further experimental results regarding attitude determination and control of the UWE-3 platform.

Finally, chapter 6 concludes this thesis.

2

Modular Satellite Bus

Since the beginning of space age modular satellite architectures have been increasingly discussed because they promise significant economic and technical benefits (Foust, 2005). Today's typical space applications depend on large and expensive satellites which require years to develop due to complicated specialized designs and manufacturing processes. The introduction of standards in satellite designs can significantly reduce development cost and time as it would allow to reuse a single design for a large number of missions, and hence reduce design and fabrication cost which usually accounts for about 60 % of the development costs of common subsystems. Technical benefits arise from the functional separation inherent to modular designs. In contrast to monolithic tightly coupled spacecraft designs, where regressive technology utilization is a mechanism for risk reduction, modular architectures allow independent components to be designed or upgraded and tested individually. Thus, the utilization of new technologies becomes more attractive. (Coffee, 2004)

2.1 Modular Architectures for Small Satellites

A design of a modular architecture for micro-satellites is described by McDermott and Jordan (2005). The so-called SMARTBus defines a set of mechanical, electrical, and protocol interfaces for the interaction of modular spacecraft subsystems. A specific spacecraft can be assembled as a stack of hexagonal module "slices", whereas each of these slices implements a particular subsystem functionality like communication or attitude determination. The project focuses primarily on the communication between the modules and on their autonomous self-configuration capability. An elaborate software stack enables the individual modules to detect, explore and utilize the whole set of modules connected by using mostly established standards like IP, UDP and XML message passing to communicate

between the modules.

Another interesting approach is promoted by Nakasuka et al. (2006) where a micro-satellite design named PETSAT is composed of several so-called functional panels. Each functional panel has a special dedicated function and can be connected to other panels to form the whole system. The flexible configuration can be stowed compactly during launch and extended in orbit to realize one of various possible structural shapes. The communication between the different panels is implemented using a CAN bus interface. In contrast to SMARTBus the modules are not canonically defined by typical subsystem functionalities. Instead, some functionalities like power or onboard data handling are distributed among several panels which enhances the overall system's fault tolerance.

Similar to the PETSAT design Reyneri et al. (2010, 2012) propose a low-cost approach for a modular nano- and micro-satellites architecture called ARaMiS. The standardized building block of ARaMiS is called "smart tile". A tile might be a cube or hexagon and contains, among structure and harnessing, a number of sensors or actuators from different subsystems. This way, major bus functions are split over a number of spatially distributed tiles such that a spacecraft composed out of several fine-grained modules incorporates all subsystems as a whole. The tiles usually form the outer surface of the satellite, leaving the inner part mostly empty to accommodate any user-defined payload. The inter-tile communication is realized with a specifically designed redundant and fault-tolerant multi-master bus system (Speretta et al., 2007).

All these architectures have in common that they split up the main functions of a complex satellite system into smaller and rather independent building blocks with standardized interfaces. This way, a high level of design and cost efficiency can be achieved as the individual modules can be designed, fabricated and tested separately and in large quantities. The possibility for simple reconfiguration provides flexibility to support various mission scenarios whereas the individual modules can be easily substituted due to the power of standardization. However, the presented examples differ in the degree of modularization. A smart definition of the functional blocks, distributing typical subsystem functionalities among several modules, can help to enhance the overall system robustness due to loosely coupled redundant components which operate in parallel. This way also a certain level of continuous scalability of the system performance can be achieved. This means that the total system capabilities can be easily scaled to the mission requirements by just adding several similar modules to the setup. The examples further deviate in the definition of the module interface. Some modules require a very elaborate protocol interface to support a high degree of automatic configuration and therefore rely on a more complex technical infrastructure like an IP stack. Others have a less restricted definition of the modules

mechanical interface in order to provide more flexibility to adapt to specific mission requirements.

However, it can be seen that modularization comes at a price. It is commonly believed that modular spacecrafts become larger and more massive as the individual components cannot be integrated as tightly as it can be done in customized designs (Foust, 2005). Functional separation and standardization might introduce additional overhead regarding secondary aspects of separated components or extensive component interaction (Coffee, 2004). Following restrictive standards might further reduce flexibility and efficiency as it could lead to oversized or over-designed spacecrafts (Cohan et al., 2006). A spacecraft can likely end up to be more capable then needed and hence be less optimized for a specific mission (Foust, 2005).

It is obvious that the optimal degree of modularization is a tradeoff between economic and technical efficiency versus mass, volume and power efficiency. Cohan et al. (2006) attempted to quantify this tradeoff and determine the optimal degree of modularity with an quantitative analysis based on simulations. Considering cost, lead-time, reliability and economic feasibility as performance metrics, they determined an optimal degree of modularity of about 60 % according to their model.

2.2 Standardization for Pico- and Nano-Satellites

Besides architectural modularization, another approach to enhance flexibility, reduce cost and promote rapid launches is miniaturization and standardization of deployment interfaces. Especially with the introduction of the CubeSat Design Specification[1] (CDS) a standard for the design of pico- and nano-satellites was provided to reduce cost and development time and to increase the accessibility to space and sustain frequent launches (Twiggs, 2003). The main key to success of the CubeSat program has been the standardization of the satellite's mechanical envelope to enable the utilization of a common launch adapter. Mainly defined in a single page document, the CDS requires a CubeSat not to be larger than a cube with 10 cm side length and to have a total mass not exceeding 1.3 kg (see figure 2.1). Following the standard enables a CubeSat developer to launch his satellite cost efficiently together with other CubeSats using a commercially available pico-satellite orbital deployer. The utilization of a standardized deployer renders a CubeSat technically and administratively independent from the launch vehicle as the satellite itself only needs to be compatible with the deployer. This way, the CubeSat standard provides a high degree of flexibility and

[1] i.e. CDS REV 12 (Stanford University and California Polytechnic Institute, 2009)

cost efficiency to the developer regarding the selection of the launch provider. (Chin et al., 2008)

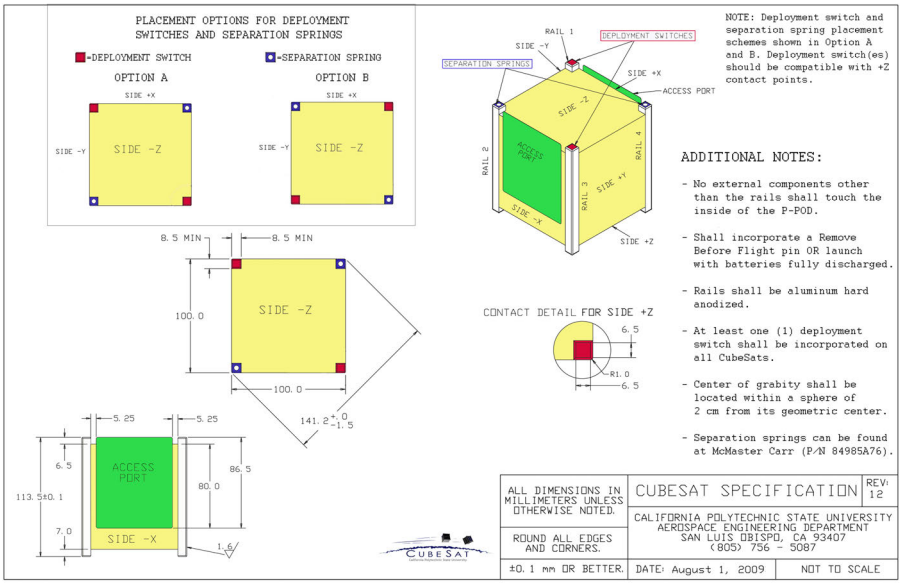


Figure 2.1: Extract from the CubeSat Design Specification Rev. 12 (Stanford University and California Polytechnic Institute, 2009)

The drawback, from developer's perspective, is that the adherence to the CubeSat standard entails a paradigm shift where the satellite's outer structure is more or less paramount. Thus, it also constitutes a further hard constraint among extreme limitation of mass, space and power budgets which are the typical critical design drivers for miniaturized satellites.

Nevertheless, by now more than 80 educational institutions from all around the world have been attracted by the flexible and cost efficient access to space provided by the CubeSat standard. Thus, the program not only takes forward the research in science and technology related to small satellites, but also significantly contributes to education as it provides unique training platforms for the next generation of scientists and engineers. (Chin et al., 2008) (Woellert et al., 2011)

As CubeSat projects at university level typically inhere high student fluctuation together with significant launch delays and limited financial budgets, optimizations in all related activities like design, production, review, integration and testing are necessary to ensure feasibility and continuity over long time. It seems obvious that a CubeSat project could significantly benefit from modular satellite architectures. The decomposition of the individual satellite functionalities into separate moderately independent modules with small and clearly defined interfaces reduces the individual task complexity and hence

promotes steep learning curves as well as the ability to easily replace subsystems after design iterations or even reuse parts from previous missions. The individual modules could be designed, manufactured and tested individually before integration into the "hot" design to be launched. Thus, tasks like re-design or improvement of modules could be much easier accommodated within the context of student projects which typically last only between three and nine months.

In the last decade a variety of satellite platforms adhering to the CubeSat Design Specification have been implemented. As the CDS mainly specifies the satellite's interface to the launch adapter, existing CubeSat implementations vary widely in terms of electrical and protocol interface design as well as in the mechanical design of the interior components. Nevertheless, with increasing availability of commercial CubeSat hardware, in the last years a specific subsystem interface definition has been frequently adopted by various suppliers. The so-called CubeSat Kit Bus[2] has been inspired by the industrial PC/104 embedded PC bus, mainly adopting the board's form factor and stackability. Similar to the industrial PC bus the CubeSat Kit Bus interconnects individual modules via a separate stackable connector beside the original PC/104 interface.

The wide adoption of the subsystem board specification demonstrates the advantages of standardization in the commercialization of miniature satellite components. A large number of CubeSats have been at least partly using commercial CubeSat Kit Bus compatible subsystems since the first launch of a CubeSat Kit based system in 2007. However, the interface definition implies some disadvantages, especially for its utilization on capable miniature single unit CubeSats. In particular, the specification's stack structure requires high currents and high data rate signals to pass through all connectors between source and target module, thus degrading path efficiency and data quality due to cumulative wiring losses. The relatively large subsystem connector of the CubeSat Kit Bus incorporates in total 104 pins and consumes about 15 % of the board space and $15-25$ % of the inter subsystem space, but only a fraction of the available pins is typically used. As the pin assignment is not completely specified, incompatibilities have been observed when combining hardware from different suppliers (Nohka et al., 2012) (Bouwmeester and Santos, 2014). Further, the bus definition does not specify redundancy concepts such as duplicated communication buses.

While the CubeSat Kit Bus specification mainly concentrates on the specification of interior subsystem modules, other approaches follow an holistic approach of structural and electrical modularity. A modular architecture for nano-satellites following partly the CDS has been promoted by McNutt et al. (2009). The design attempts to scale down an

[2]CubeSat Kit™ (Pumpkin, Inc., 2010)

available modular plug-and-play infrastructure for bigger satellites, the so-called Space PnP Avionics (SPA), and applies it to the CubeSat form factor. The resulting architecture evolved to a symmetric arrangement of hinged panels, which themselves accommodate the satellite subsystem components. These modules are interconnected in a plug-and-play manner using an extended USB interface and a central hub.

The central question connected to further standardization of pico- and nano-satellite technology is how to combine the power of modularization with the launch flexibility promoted by CubeSat standard while taking into account the typical constraints of miniature satellites such as limited mass, space and power budgets. Despite the progress made in the field of miniature satellites it can be seen that the combination of modularity and miniaturization inheres still challenges when further miniaturization is required to target capable pico-satellite missions. In the following sections the requirements and trade-offs defined for the modular UWE satellite bus are described and the implementation and test results of the first demonstrator UWE-3 are presented.

2.3 The UWE Satellite Bus Concept

Experiences from the previous UWE missions indicated that the re-utilization of a system, which is not inherently designed to be extended, can hardly be upgraded without producing a significant increase in total system complexity. Figure 2.2 (left) shows the flight model integration of UWE-1 and its successor UWE-2 (right), which has been developed as an extension of the UWE-1 platform. Especially fixed dependencies between electronics and structural components of the former platform limited its flexibility regarding subsystem re-alignment and harnessing for the optimal integration of the newly developed attitude determination system and its sensor suite. Further, the remaining power and mass budget as well as the available space were almost exhausted. The resulting design proved to complicate integration, testing and maintenance such that after first integration of the flight hardware no modifications to the configuration were possible anymore.

One of the most important design rules of the next generation UWE platform constitutes the support for simple, standardized and continuous testing at satellite bus architecture, as well as for the subsystems. For the bus architecture this implies the requirement for simple and quick assembly and disassembly of the entire setup. The prototype can thus be easily tested and debugged in a flight model configuration and disassembled again for further modifications with a minimum of time and cost overhead. In addition, even though it is not intended to disassemble the flight model for late modifications, it would be possible if needed.

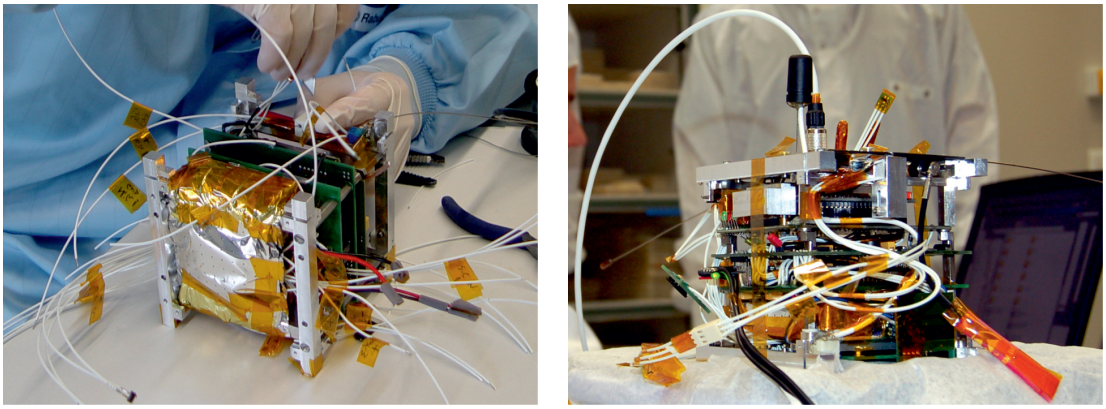


Figure 2.2: UWE-1 flight model integration in cleanroom (left). UWE-2 flight model as an extension of the UWE-1 platform (right).

Further objectives for the conception of the UWE bus beside mass reduction, compactness and efficiency was modularity, with special focus on support for future extension. The careful definition of simple and clear mechanical, electrical and protocol interfaces significantly decrease complexity, reduce dependencies and ensure compatibility in future. Hence, in contrast to many other CubeSat Missions, the design philosophy for the UWE next generation is to preserve the authority over the subsystem interface, relying on third party products only on component level. This way individual components can be much easier replaced or upgraded at subsystem level, while maintaining compatibility to the satellite bus.

2.4 Modular Structure of the UWE Bus

According to Baldwin and Clark (2000) the power of modularization arises mostly from the reduction of inter-modular dependencies to a standardized minimum. In case of a satellite system it seems natural, to canonically map typical subsystem characteristics also to the module level. Subsystem interfaces comprise mechanical, thermal, electrical and protocol functionalities. Thus, special subsystems such as structure, thermal control, or the electrical power system require special care as they critically influence the inter-modular interface.

The thermal interface is not a critical issue in most pico-satellite applications due to reduced heat dissipation on the power limited satellite together with the usually close distance to Earth in a Low Earth Orbit (LEO). In fact, the majority of miniature satellite platforms solely rely on passive thermal control mechanisms (Selva and Krejci, 2012). More demanding are the mechanical interfaces with their impact on mass and volume,

which are main design drivers within the limits of small satellites. On one hand the CubeSat Design Specification dictates a certain set of constraints for the satellite structure. On the other hand various subsystems require specific positions or alignments within the satellite. Subsystems like attitude determination require exposure of their sensors to the space environment with a specific alignment, whereas the temperature sensitive batteries require to be positioned in a thermally protected environment in the center of the satellite. A modular structure has to support both kind of requirements in a miniaturized and compact fashion while maintaining flexibility and standardization at the same time.

The UWE pico-satellite bus structure complies with the CDS. The CDS requires the satellite to provide four rails at parallel edges which are separated by 10 cm from each other and define the physical contact interface to the pico-satellite launch adapter (see figure 2.1). The panel surfaces between the rails ($-$X, $+$X, $-$Y, $+$Y) and the two surfaces on top ($-$Z) and bottom ($+$Z) must not exceed 6.5 mm from the rail surface to prevent them from touching the launch adapter. Separation springs and kill switches must be accommodated inside the rail ends on the top ($-$Z) side to ensure and indicate proper separation from other CubeSats and the launch adapter. The satellite can be accessed for maintenance at the $-$X and $+$X side after integration into the launch adapter.

The UWE pico-satellite bus structure defines the mechanical components and the alignment of the subsystem modules inside the satellite. In order to ensure comfortable access to all subsystems in a functional configuration and to protect the interior from environmental hazards the mechanical (outer) structure is decoupled from the electronics (inner) structure.

2.4.1 Inner Structure

The inner structure is based on a stack of several subsystem boards. The set of subsystems, each implemented on an individual PCB, include all typical satellite subsystems like power, onboard computer, communication and attitude determination and control, optimized with respect to size and mass. The subsystem boards are mechanically fixed in position by four sets of steel screws, which provide a good thermal resistance and constitute, except for electrical connections, the only physical connection of the inner structure to the outer structure.

As the usage of wired connections typically consumes more space and is often uncomfortable to handle in miniaturized systems, the UWE pico-satellite bus design tries to avoid any need for cables by using a backplane. The individual subsystems are entirely interconnected with the other subsystems by the backplane with standardized connectors

so that no further wiring is necessary. This way, the individual boards can be packed with arbitrary high density, still providing a high degree of flexibility for the alignment of the subsystems in the inner structure.

The generic subsystem interface combines multiple digital interfaces like UART or I^2C along with various GPIOs lines and power interfaces for different voltages. Moreover, several general purpose lines as well as dedicated signal lines such as for global reset or debug support are available on the bus. Thus, most potential future extensions can be supported. A detailed overview of the mechanical and electrical interface definition can be found in appendix A.1.

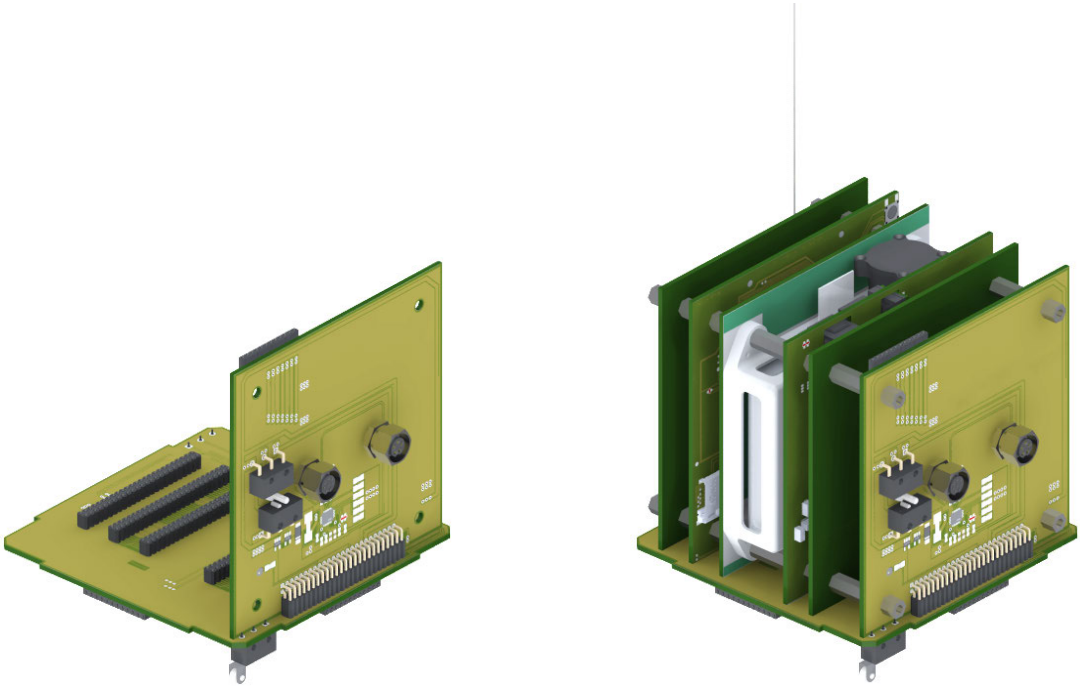


Figure 2.3: Drawing of the UWE inner structure. The individual drawings show the backplane and the Front Access Board only (left) as well as the complete inner structure in a functional configuration (right).

The subsystem electronics arrange for a standard circuit for power control, power monitoring and latch-up protection in terms of individual definable over-current shutdown, which can be controlled via I^2C interface. Analog channel buffers decouple the digital interface lines on the backplane from the corresponding interfaces of the subsystems. This enables to completely power down individual subsystems and to protect the digital buses from undesired bus allocations of malfunctioning subsystems.

The backplane is supplemented by the so-called Front Access Board (FAB) so that it can further provide electrical interfaces for all side panels of the outer structure. Moreover,

the FAB accommodates digital and power connectors of the umbilical line as well as the Remove Before Flight (RBF) switch which are accessible from the outside via notches in the −X side panel. Micro separation switches are located on the backplane itself, so that their physical contacts are located inside the side rails in order to comply with the CDS.

In the configuration shown in figure 2.3 the satellite is fully functional from an electrical point of view. In this configuration (optionally with externally connected side panels) the entire functionality of the subsystems can be tested including subsystem interference tests. The design moreover allows easy assembly and disassembly so that subsystems can be replaced with minimum effort.

2.4.2 Outer Structure

The link between the electrical (inner) and the mechanical (outer) structure is realized by four identical and symmetrical side rails which are attached to the steel screws and provide the required mechanical interface to the launch adapter (see figure 2.4). The rails are manufactured from temperature stable aluminum and are further hard anodized on the outer surfaces to prevent them from electrical conduction and cold welding during launch. The rails are hollowed on their inner side to save mass. They further provide contact faces, as well as mounting threads for the panels on the outer sides.

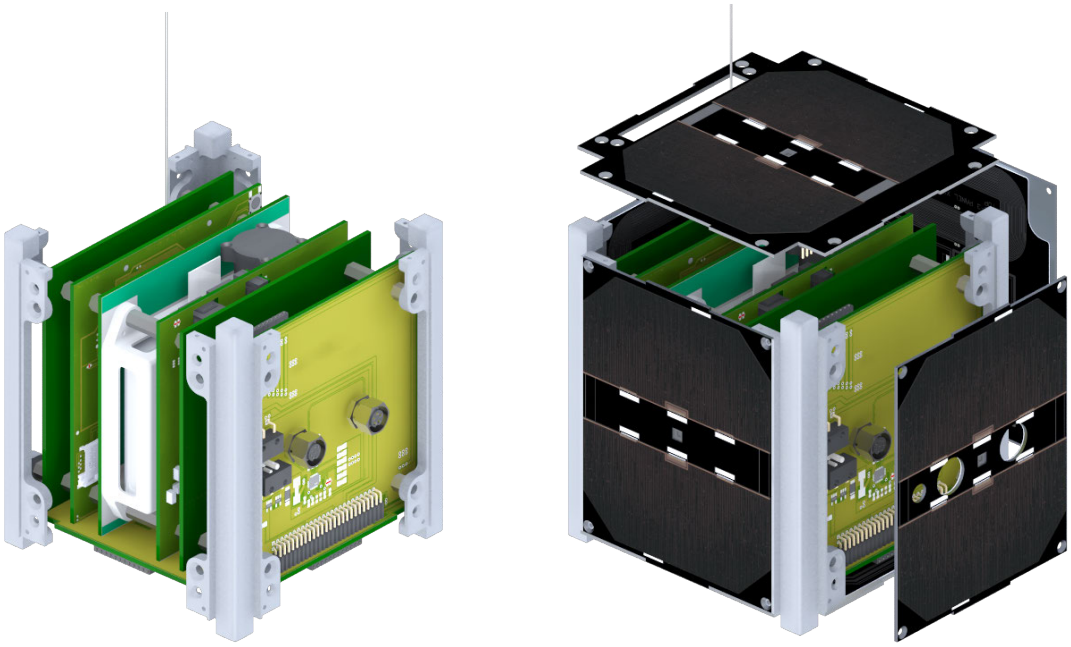


Figure 2.4: Drawing of the UWE outer structure. The individual drawings show the outer structure with CDS compliant rails (left) and multifunctional side panels (right) connected to the bus.

The six side panels play a special role in the modular design. The panels are made from aluminum to provide good heat conduction for thermal balance and good electrical conduction which is beneficial as the pico-satellite's metal frame is typically part of the antenna system, acting as a ground plane. Moreover, a millimeter of aluminum can significantly shield the interior from radiation in space environment (see figure 4.1). On the other hand the pico-satellite's panels usually carry the solar cells as well as other sensors (e.g. sun or star sensors), which must be exposed to the outer environment. For this reason a design consisting of a double sided PCB with aluminum core was chosen (see figure 2.5). Thus, the panels combine electrical with mechanical requirements, providing functionalities of mechanical stability, thermal balance, radiation protection, antenna groundplane, and power or sensor electronics in an integrated compact and lightweight design.

The panels can be simply plugged into the backplane and fixed at the side bars, which allows comfortable assembling and disassembling for maintenance after integration or flight-model-realistic testing during development. Once connected to the bus, the panels automatically determine their location on the satellite so that they can configure themselves correspondingly.

Figure 2.5: The side panels as a double layer PCB with aluminum core combine functions of structural stability, thermal balance, radiation protection, antenna ground plane, and electronics like wiring or sensor electronics in an integrated compact and lightweight design.

2.5 Standardized Test Interface

Beside standardized mechanical and electrical interfaces also some common protocol interfaces have been specified for the UWE bus. In particular, specific protocols have been defined in order to promote hard- and software testability of the individual components

developed. Beside support for in-system-debugging in terms of live memory inspection and breakpoint debugging, the test interface accounts for a bidirectional communication link for logging, event triggering and runtime data exchange. Especially the communication interface is crucial when it comes to automated hardware-in-the-loop tests. In order to encourage involved software engineers to utilize this opportunity frequently from the beginning, a set of protocols and software tools has been developed which allow to define and perform automated tests of the embedded software and provide access to relevant runtime debug information with minimal effort.

2.5.1 Lightweight and Simple Debug Protocol

The UWE-3 debug protocol is a lightweight and flexible link protocol for simple structured data exchange. It was introduced for two purposes. First, to provide a framework with a set of handy functions in order to reduce the initial workload whenever test interaction with an embedded component might be helpful. Second, to enable independent, maintainable and hence sustainable software development by many developers working on the same hardware but on different tasks.

In order to be deployed on various embedded architectures the protocol is implemented in ANSI C with a minimal footprint. The protocol allows the developer to send and receive data packets via a set of virtual data channels. As long as the developer uses a unique channel for his specific application, collisions with other services, available or implemented in future, are avoided. The protocol also identifies events of packet loss and data corruption. Further, it reliably handles packet synchronization after corrupted packets have been received for any reason. As the average protocol overhead is only about four bytes, the protocol can be used effectively with low transmission rates.

A virtual channel might transport a defined set of structured data frames from a PC to the embedded device and vice versa. These data frames are typically defined as nested C-struct types including arbitrary primitive data types. On PC side, two protocol implementations exist: A Java based implementation and a pure MATLAB implementation. In both implementations a set of convenience functions takes care of automatic serialization from and de-serialization to the corresponding high level data types in Java or MATLAB. Thus, arbitrary subprotocols can be implemented within seconds.

While the MATLAB frontend is usually used for rapid implementation of automated test and data logging scripts, the Java frontend can be used to implement proven protocols for data exchange with a solid platform independent user interface. For this reason, a generic and extensible user interface application is provided to the students. Basing on the Eclipse

Rich Client Platform, the software combines a handy user interface framework with a powerful plugin functionality. This way, any extension implemented can be encapsulated as a modular plugin which perfectly accompanies with the protocol philosophy of promoting sustainable software in the context of educational projects.

Despite various device specific protocol definitions, a few services implemented are more generic and useful in most embedded applications to support robust software development. Two of them are described in more detail in the following sections.

2.5.2 Embedded Unit Testing

One of the most frequently used services implemented for the debug protocol is a framework for embedded unit testing. It brings along several C macros for rapid test definition and execution of assertions. An example test case implementation can be seen in listing 2.1. Once declared anywhere in the source code a specifically developed preprocessor explores all available test definitions and links them into a test database structure during compile time. At runtime, a list of available test cases and their hierarchical relations can be requested via the debug protocol. A specific view in the user interface presents the test cases in a tree view and lets the developer select a subset of tests for execution. This will trigger the corresponding source code to execute the implemented assertions. Any performed assertion will update the user interface which displays a colored status bar indicating progress and success (see figure 2.6). A second view displays all messages logged by a set of convenience macros for more detailed analysis.

Listing 2.1: Simple distributed definition of embedded unit test case.

```
EUNIT_DEFINE(mytest, "description", 2, $myparenttest) {
        ... //do some stuff, e.g. value = calculateValue()
        EASSERT("assertion␣#1", value >= 10, "error:␣%i<10", value);

        EASSERT("assertion␣#2", value <= 20, "error:␣%i>20", value);
}
```

The unit testing framework has shown great acceptance among the developers due to its simple and distributed way of defining test cases which further supports parallel development without the need for maintaining a central database of tests. This way, any code developed any time during the development cycle for testing any specific part of the hardware or software, remains accessible in the system to be executed any time in future.

2.5.3 Embedded Variable Synchronization

A similar and not less powerful framework implemented on the debug protocol is the so-called variable synchronization. Instead of the normal declaration of a static variable a specific macro can be used to publish the variable also via the debug protocol (see listing 2.2). The variable itself can still be used in the same way as before, but it can now further be read and written via the PC user interface. Optional hooks for the registration of external *set* and *get* events can be registered in terms of function pointers. This way an externally modified or requested value can be further synchronized with hardware periphery such as connected I^2C devices.

Listing 2.2: Definition of synchronized variable simply replaces conventional static variable definition.

```
//static int16_t myvariable;
VARSYNC_DEFINE(myvariable, int16_t, "description",
               &setFunction, &getFunction, $myparentvariable);

void getFunction{void} {
        //get call hook, e.g. read value from external hardware
}

void setFunction{void} {
        //set call hook: e.g. write value to external hardware
}

void main(void) {
        ...
        myvariable = 0xFFFF; //use variable locally as usual
        ...
}
```

The user interface displays the entire variable tree and enables to poll recent variable values as well as to overwrite a specific value at any time. All values received can be plotted over time and are further logged to a file for later analysis. The variable synchronization protocol constitutes a powerful tool allowing the software developer to get access to the running software by simply adding a line of code. Using the protocol with the MATLAB frontend renders the framework as a valuable tool for script based hardware-in-the-loop tests. In the scope of the UWE-3 project it has been frequently used for data logging during long term tests, for quick identification of adequate parameters and for verification of

formula implementations by simply comparing the embedded calculations with MATLAB reference implementations.

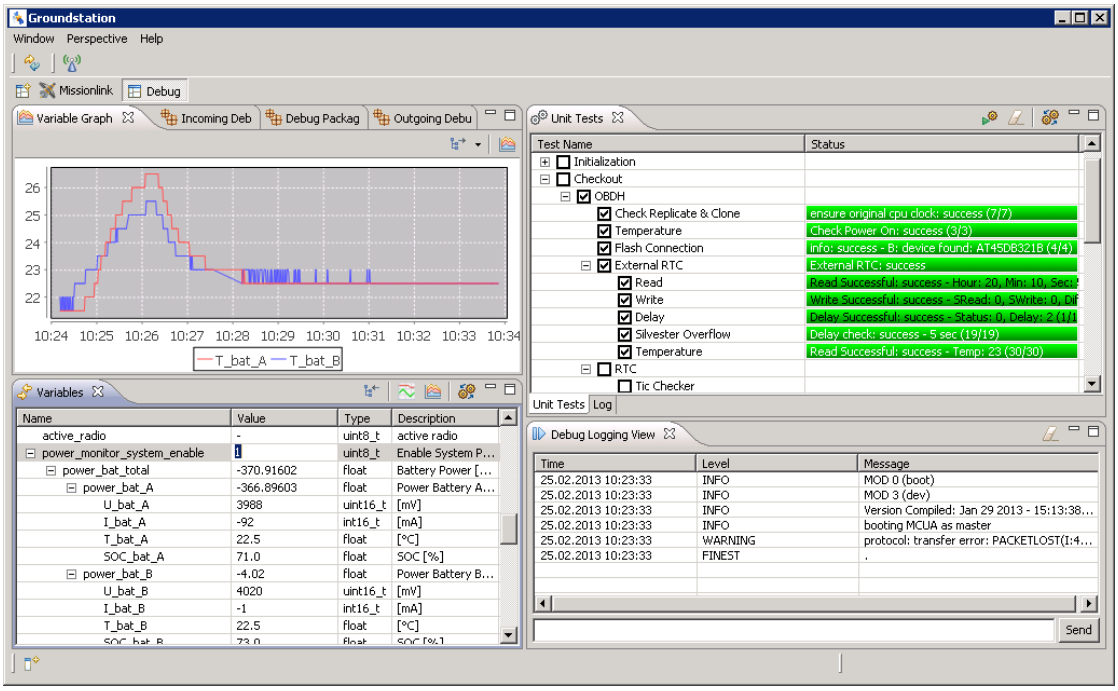


Figure 2.6: Screenshot of the Java debug protocol frontend showing views for embedded unit test and embedded variable synchronization.

2.6 Structural Simulation

A detailed 3D model of the satellite design based on SolidWorks 2008 (SP2.1) has been used to determine and adjust the platform's mass distribution prior to production and integration. Due to the flexible subsystem relocation on the backplane the design's center of mass could be placed within a few millimeters close to the satellite's geometric center. A detailed overview of the platform's geometric and mass distribution properties is shown in table 2.1 and figure 2.7.

2.6.1 Static Acceleration Analysis

The presented satellite design avoids conventional dedicated structural frames and relies mainly on the structural performance of the integrated panels and system boards. A static acceleration analysis has been performed on the 3D model in order to reveal the design's response to equivalent static acceleration forces as expected during launch. For this task, a

Parameter	Unit	Value
Total Mass	g	1041
Dimensions	mm	
L_x		106.00
L_y		106.00
L_z		113.50
Including panels, each protruding 3.00 mm from the −X, +X, −Y, and +Y side respectively. Excluding protruding spring plungers and separation switches.		
Geometric Center	mm	
GC_x		50.00
GC_y		50.00
GC_z		56.75
Related to geometric reference frame with origin on the outer corner of the -Z contact area on rail 2 (CDS), aligned such that the individual axes point normal towards the corresponding +X, +Y, or +Z side (see figure 2.7, top).		
Center of Mass	mm	
CoM_x		53.37
CoM_y		49.59
CoM_z		56.07
Related to geometric reference frame with origin on the outer corner of the -Z contact area on rail 2 (CDS), aligned such that the individual axes point normal towards the corresponding +X, +Y, or +Z side (see figure 2.7, top).		
Moments of Inertia	$g \cdot mm^2$	
I_{xx}		2013270.70
I_{yy}		1992787.93
I_{zz}		1989353.37
Related to mass reference frame with origin in the center of mass, parallel to geometric reference frame.		
Products of Inertia	$g \cdot mm^2$	
I_{xy}		1410.16
I_{xz}		31584.36
I_{yz}		-18389.40
Related to mass reference frame with origin in the center of mass, parallel to geometric reference frame.		

Table 2.1: CAD generated properties describing satellite geometry and mass distribution.

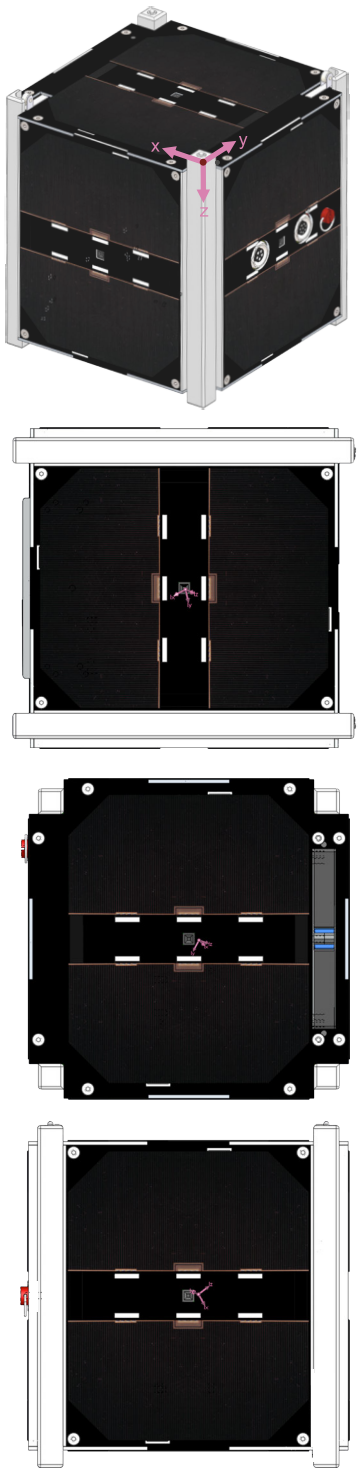


Figure 2.7: CAD drawings indicating geometric reference frame (top) and location of the center of mass as seen from +X, +Z, and +*Y* side (bottom) respectively.

reduced 3D model which reflects all relevant parts contributing significantly to structural stability and mass budget has been used. Minor contributions like small screws, connectors, spring plungers, deploy switches, integrated circuits, etc. have been omitted to reduce the model's complexity.

The analysis has been performed with the SolidWorks COSMOS toolbox. Figure 2.8 shows the corresponding mesh used for the structural simulation. The mesh has been generated by applying global contacts between the different parts of the model.

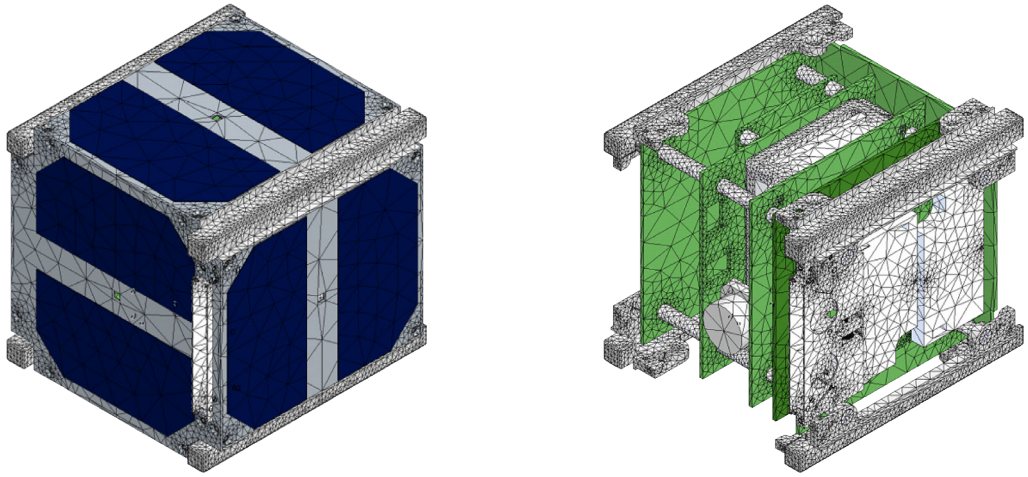


Figure 2.8: Reduced structural model used for finite element analysis (right view with hidden panels). The shown mesh comprises 226.204 elements and 441.057 nodes.

According to the launch provider the satellite would be exposed to a longitudinal acceleration of up to 10.5 g combined with transversal forces in the order of 3.4 g whereas the exact orientation of the launch adapter has not been fixed at this time. In order to simulate the structural response to all possible accelerations present during launch, longitudinal and traversal force vectors have been applied to each possible ordered pair of orthogonal satellite sides. In each scenario, evenly distributed normal forces were applied to the corresponding contact areas on the CubeSat's rails. The resulting accelerated rigid body motion has been compensated using the *Inertial Relief* option of the used solver.

The maximum deformation in terms of relative node displacement have been recorded for each simulated scenario. The results show that the structural deformation for all scenarios is limited by a comparatively small relative node displacement in the order of 10^{-4} m which occurs predominantly in the interior of the satellite (see figure 2.9). The complete result set can be seen in appendix A.2.

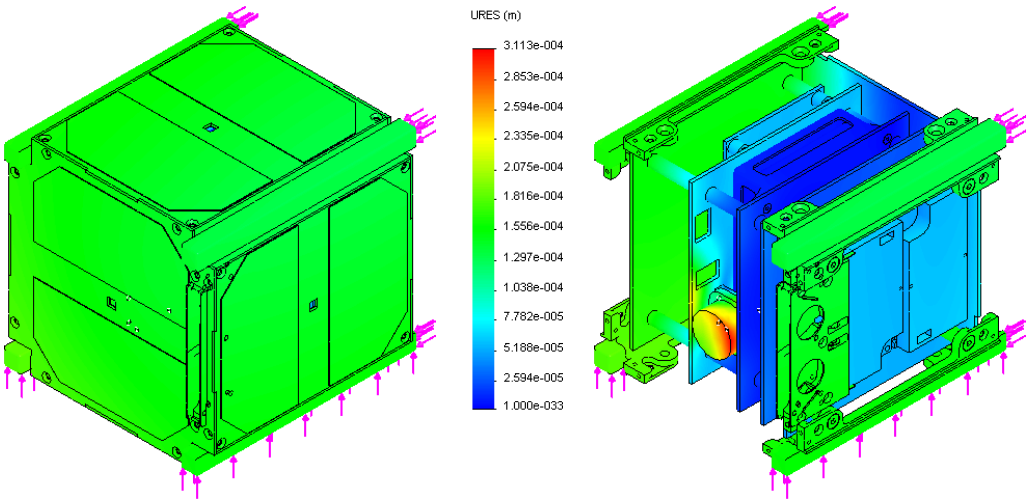


Figure 2.9: Static acceleration analysis result showing maximal relative node displacement for launch equivalent longitudinal acceleration on +Z axis and transversal acceleration on +Y axis.

2.7 Development, Integration and Test

After finalization of the individual subsystem developments a final design freeze has been initiated in late 2012 before flight model production, integration and test campaigns have been completed in first quarter of 2013. The UWE-3 flight model has been shipped to the launch site in late 2013. After final checkout at the launch site, approximately 4 weeks prior to lift-off, the satellite has been activated for launch and the launch adapter has been integrated into the upper stage of the launcher. The following sections summarize the engineering process of UWE-3 from development until launch.

2.7.1 Development and Production

Already during design phase the modular architecture could demonstrate effectiveness as it simplified the concurrent and independent design and test of the individual subsystems. Typically two to three design and test iterations were necessary to realize an error-free and optimized subsystem prototype. In this process the standardized subsystem interface significantly reduced the complexity of the test setup as a prototype could be easily tested separately on a generic prototype interface board (see figure 2.10, bottom, right).

The prototyping board itself realizes the inter-subsystem harnessing by mimicking the satellite's backplane while further providing comfortable access to all relevant power and data lines on the bus. More complex tests could be performed as required by simply adding

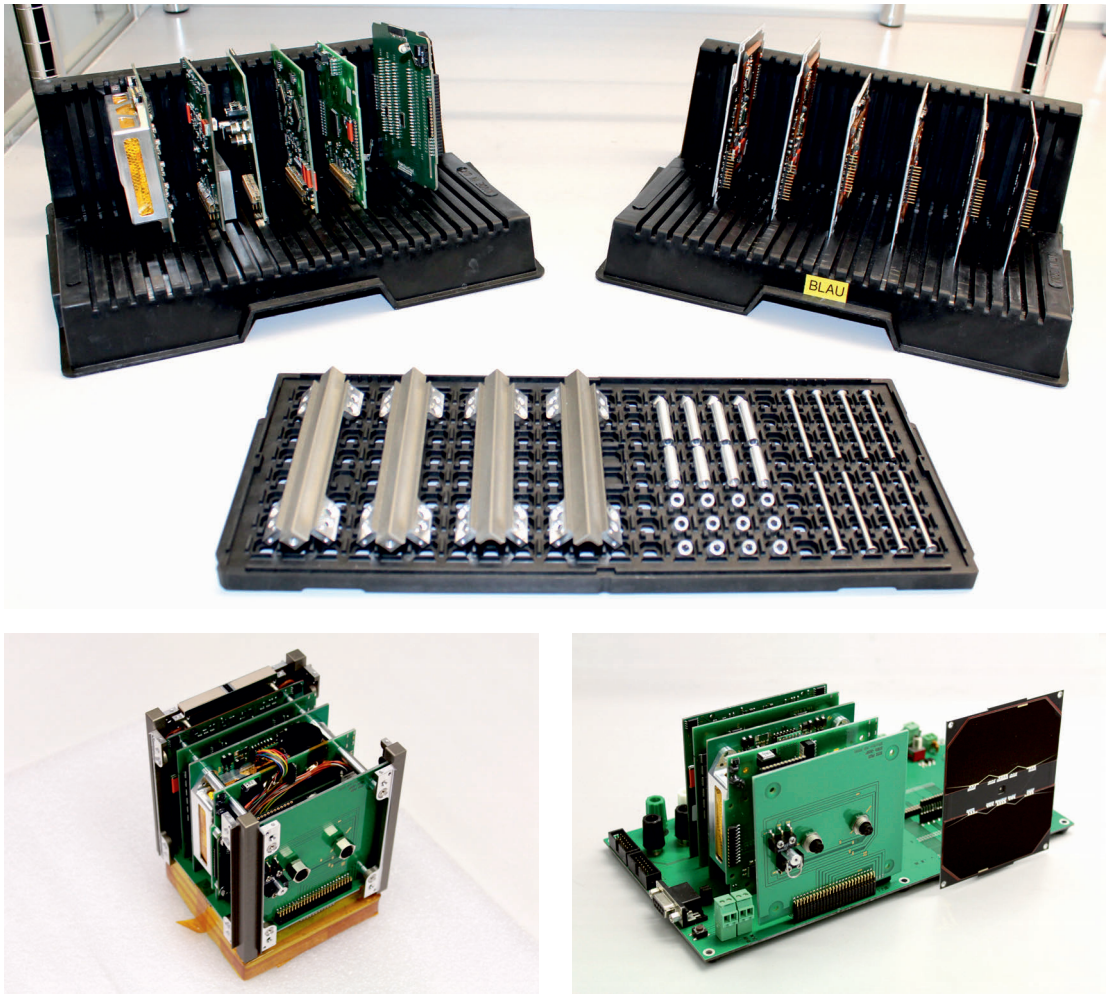


Figure 2.10: UWE-3 flight model parts comprising subsystem PCBs, multifunctional side panels and mechanical rails (top). Functional assembly in flight-like configuration (left) and prototyping configuration (right).

additional subsystem boards to the setup, whereas the standardized interface ensured compatibility between different versions of currently available and quite often shared test hardware.

Already during prototype development, functional tests have been performed as often as possible in flight-like configuration (see figure 2.10, bottom, left) in order to reveal compatibility problems as early as possible during design phase. The modular architecture allowed rapid reconfiguration of the prototyping test setup to an integrated flight-like configuration and back again. A short briefing was usually sufficient to enable a new student team member to build up the completely integrated satellite model from its individual components as shown in figure 2.10 (top).

2.7.2 Integration, Test and Launch Preparation

The described advancements related to modularity and testability introduced by the UWE architecture could especially be demonstrated during integration and acceptance test campaign of the flight model. In beginning of 2013 the complete flight model could be assembled from its individual subsystems and tested for functionality within a few hours only. Figure 2.11 documents the integration and functional test procedure in the university's cleanroom. Starting with the empty backplane the individual subsystems have been inserted one by one before the boards have been fixed in place by attaching the side rails to the board structure. Afterwards the setup has been activated and extensively tested by running a suite of predefined system checkout test cases in order to verify the subsystem functionality and the inter-subsystem connectivity.

With all tests passed the integration has been continued by plugging in the side panels to the satellite bus and fixing them to the rail structure. Once all panels had been attached, the satellite was activated again to run an auto-configuration script on the panels. As all panels are usually programmed with the same software image, the initialization routine ensures that the panels automatically identify their location on the bus to initialize the individual configuration memory with the corresponding addresses and configuration parameters. The integration campaign has been completed with a final unit test run also including the panel checkout test cases.

Two weeks after integration and functional tests of the flight hardware the satellite has been subject to an intensive thermal-vacuum, vibration, and acceleration test campaign conducted at external test facilities. For this campaign a proto-flight test philosophy has been chosen where the flight hardware was tested according to qualification levels combined with acceptance test durations. The test levels were selected according to the specifications provided by the launch provider.

During both, acceleration and vibration tests, the satellite was located electrically inactive inside a test launch container to simulate launch conditions. After each test run the satellite has been visually inspected and further activated to execute previously mentioned checkout self-tests. Especially mechanical actuators such as the reaction wheel and both antenna deployment mechanisms were intensively verified. Due to the revertible antenna deployment mechanism the deployed antennas could be easily stowed again inside its housing after each test-run without the need for exchanging any mechanical parts. The test campaigns could be successfully completed without any unexpected issues.

Several thermal-vacuum tests have been performed in-house during development phase on various prototypes. In the context of the acceptance test campaign an extensive twenty-

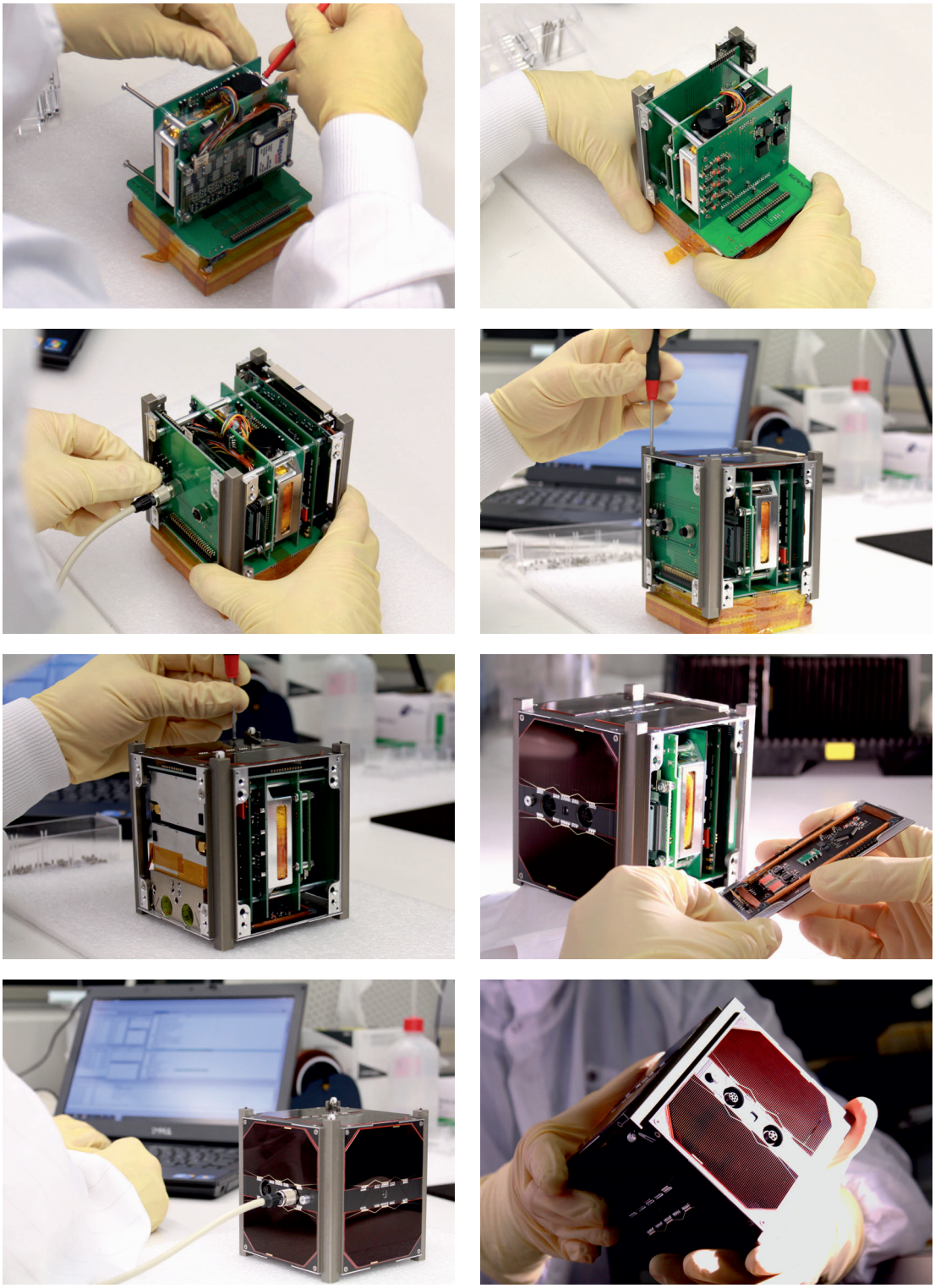


Figure 2.11: Picture series documenting UWE-3 flight model integration. After inserting the subsystem PCBs into the backplane and fixing them with the rails the functional setup can be tested. Afterwards, the multifunctional side panels are plugged to the backplane and fixed to rails before the complete setup is tested again using a set of precompiled unit tests.

four hours thermal-vacuum verification test has been conducted on the proto-flight model. Besides the internal housekeeping sensors about 15 additional thermo elements have been installed on relevant structures inside the satellite to achieve a comprehensive overview of thermal distribution during the test (see figure 2.12, top). The satellite itself has been placed thermally decoupled in the center of a 2 m chamber. Several power and data lines of the satellite's umbilical line have been fed inside the chamber to be controlled and monitored from the outside. An additional UHF antenna was placed inside the chamber in order to be able to verify the radio communication during extreme conditions.

The test has been started with the hot case, heating up the thermal shroud to collect all temperature measurements well above the expected operational maximum of about 55 °C. Afterwards the thermal shroud has been cooled down for an extended period while all relevant measurements converged close to the expected operational minimum of −40 °C in the cold case (see figure 2.12, bottom). Both test cases have been concluded with the deployment of one of the redundant antennas followed by a complete system self-test including UHF communication.

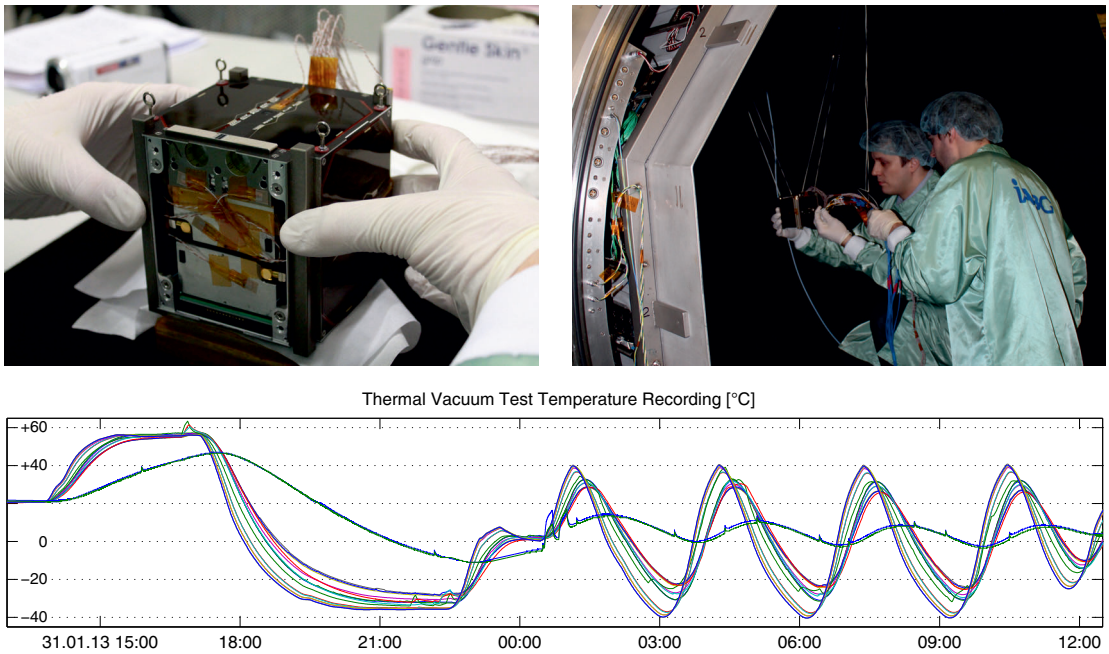


Figure 2.12: Thermal vacuum test of flight model (top) during acceptance test campaign. Recording of various temperatures measured at different locations on the satellite during the 24 hours test run (bottom).

After testing mentioned extreme operation conditions several temperature cycles have been conducted to simulate temperature variations in orbit. The cycles were controlled such that the outer panel structure was exposed to temperatures between the expected

nominal limits of about −40 °C to +40 °C. In order to accelerate the convergence to a steady state the sequence has been started with the expected average temperature of about 0 °C at nearly all locations. In the course of the test run self-tests of all relevant subsystems have been executed periodically and different low and high power operation modes have been verified. As it can be seen in figure 2.12 (bottom) the satellite's thermal behavior quickly converged and all interior components remained periodically stable within −30 °C and +30 °C during thermal cycling.

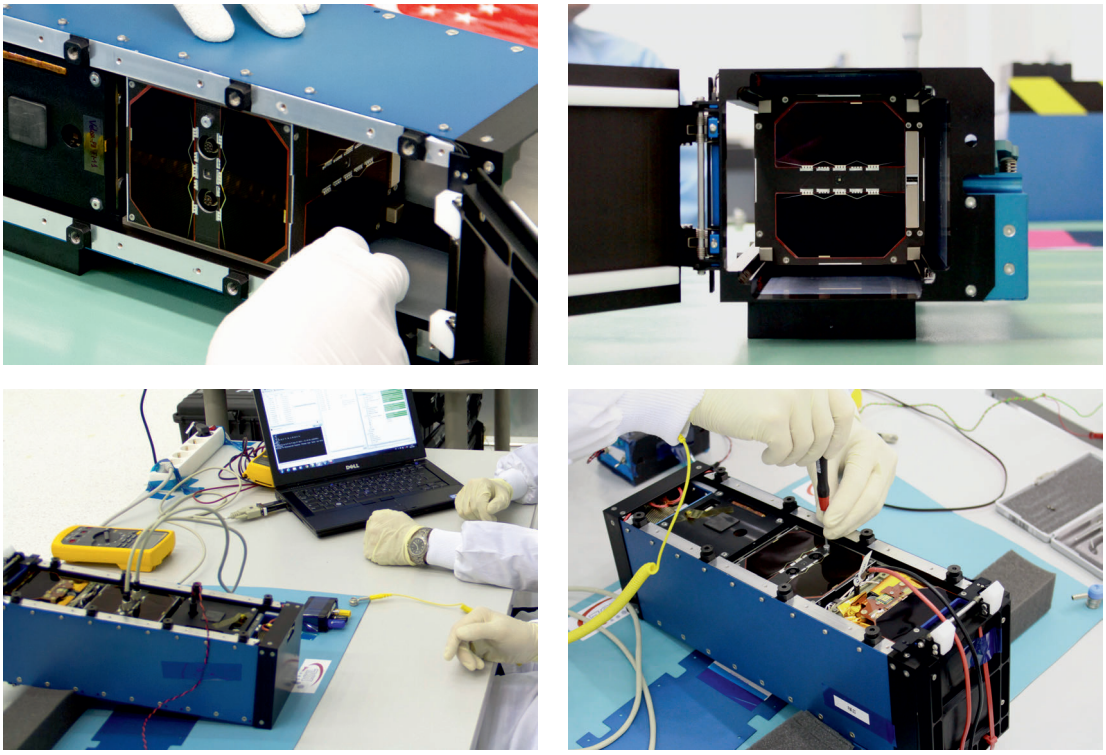


Figure 2.13: Integration of UWE-3 flight model into triple unit launch adapter together with VELOX-PII and First-MOVE (top). Pre-launch checkout tests and final flight activation at launch site (bottom).

Even though nearly all test cases showed similar results compared to previously conducted tests in-house during development phase, some irregularities have been observed during the final proto-flight test campaign. In particular, comprehensive radio communication tests under thermal-vacuum conditions have never been tested before on the completely integrated satellite. Unfortunately, the proto-flight model showed significant temperature dependent communication link degradations on both redundant transceivers. While first investigations were focused on the thermal stability of the transceiver's RF front-end, the fault could finally be revealed as a slight deviation of the microcontroller's internal oscillator controlling the asynchronous UART link between the transceiver and the onboard

computer. Fortunately, this could be easily accounted for by adjusting the software to use a more precise external oscillator for clock generation of the communication interface.

With all acceptance tests passed the flight model has been integrated into a triple unit launch adapter for further storage and transportation to the launch site. As it can be seen in figure 2.13 (top) UWE-3 has been located on the middle position between two further pico-satellites sharing the same launch adapter. Approximately four weeks prior to lift-off a final checkout has been conducted at the launch site itself where the satellite could be accessed within the launch adapter for the last time (see figure 2.13, bottom). Without any significant discharge observed the satellite's batteries had now been completely charged from about 60 % state-of-charge for proper storage to 100 % state-of-charge for launch. After final activation and execution of the complete checkout test suite the flight model has been armed for automatic activation after ejection from the launch adapter.

2.8 Summary

This chapter addressed relevant aspects regarding the motivation, design, implementation, and application experiences of the modular and flexible pico-satellite bus introduced with UWE-3. The current state-of-the-art has been presented in terms of a brief summary of related work concerning modular satellite concepts and small satellite platforms. The fundamental concepts of relevant design and implementation aspects have been elaborated in detail. Finally, general experiences illustrating the system's advantages in the context of an educational pico-satellite project during development, integration, and test campaigns have been discussed.

Further in-orbit performance measurements of the platform's thermal behavior in space are described in chapter 5.1.1. Final conclusions regarding design, application, and operation of the modular satellite bus are consolidated in chapter 6.1.

3

Flexible and Robust Electrical Power System

Increasing system complexity of modern miniature satellite platforms together with typically constant mass and size constraints imposed by the underlying standards emphasizes the demand for robust and energy efficient Electrical Power Systems (EPSs) at minimized mass and volume. Even though these requirements sound similar for the majority of space systems, it is clear that the requirements and challenges for small satellite missions might differ from the design drivers of traditional large, high power missions.

The most critical design constraint imposed by a typical pico-satellite mission constitutes the limited size and mass budget available on a miniature satellite. This is especially relevant for the design of an EPS as the batteries together with its support structure constitute a significant amount of the total mass budget. Also electrical components especially for high power conversion such as filters or large coils can significantly contribute to the mass budget.

As for all subsystems on a spacecraft reliability and failure-tolerance are the most important design drivers. This is especially true for crucial subsystems such as the EPS. Concepts like redundancy and derating can provide a certain level of robustness but usually at the cost of mass, size and efficiency. In the majority of traditional space applications it is required that less than 10 % of the power capability can be lost due to single component failure. Additionally, the individual components are used far below $(60-70\,\%)$ the ratings used in commercial electronics (O'Sullivan, 1994).

Considering the limited size of a pico-satellite it is clear that the power available on the spacecraft is extremely limited. Selva and Krejci (2012) and Bouwmeester and Guo (2010) state that the Orbit Average Power (OAP) of available single unit CubeSats is in the order of 1 W. The exact number depends on a lot of factors such as orbit, geometry of solar

panels, and efficiencies of the power bus. For a single unit CubeSat equipped with solar cells on each surface an exemplary OAP estimation can be as follows:

The maximum power generated by a single side panel equipped with state-of-the-art triple junction solar cells[1] operating at $+40\,°C$ is about $2.25\,W$. In case the satellite is slowly spinning about a single axis, the ratio of average illuminated surface area to the one of a single panel can be approximated by $1.3 - 1.5$. Assuming further an eclipse time[2] of $40\,\%$ the generated average power per orbit is consequently limited by $1.7 - 2.0\,W$. This boundary value does not yet include any losses in power path, storage, and conversion which can easily sum up to $40\,\%$ for higher currents. The estimation further assumes that the solar cells are always operated at the instantaneous maximum power point. This is not a trivial requirement for an uncontrolled satellite as both, cell temperature and irradiation might vary rapidly with time for each individual panel. Having in mind that available radio subsystems for CubeSats typically consume already $100 - 400\,mW$ in stand-by or that the operation of a single state-of-the-art reaction wheel for pico-satellites requires $700\,mW$ (Stoltz et al., 2008) it is clear that efficiency is an important design driver for pico-satellite missions.

Other challenges arise from thermal issues. Batteries usually require special care involving thermal insulation and active heating to ensure operation within allowed temperature ranges and to achieve optimal performance throughout the entire orbit. The absence of complicated thermal control structures further implies special care to avoid hotspots due to thermal dissipation in inefficient high power paths.

However, one of the most important requirements for modern pico-satellite missions is flexibility. Typical electrical power subsystems for spacecrafts comprise power generation, storage, conversion, and distribution. The sizing or selection of the individual functional blocks highly depends on the mission requirements (Wertz and Larson, 2005). In order to enable rapid satellite development a generic electrical power system for small satellites has to be designed to support a multitude of mission scenarios. It needs to be scalable with peak power and average power requirements and must be adaptable to various mission parameters and spacecraft configurations without requiring a complete redesign (Clark and Mazarias, 2006).

In the progress of the UWE-3 project special focus was put on the design of a flexible power system which seamlessly integrates into the modular plug-and-play design paradigm of the UWE architecture. In the following sections an overview of common electrical power systems for pico-satellites is presented before the concept and design of the UWE-3

[1] e.g. series connection of two GaAs solar cells (3G28C) from AZUR SPACE as employed on UWE-2
[2] e.g. eclipse time of a typical sun-synchronous LEO such as used for UWE-2

EPS are described in detail and performance results from various verification tests are discussed.

3.1 Electrical Power Systems for Pico-Satellites

There is a variety of common topologies for electrical power systems of solar powered spacecrafts. The basic approaches are Peak Power Tracking (PPT) and Direct Energy transfer (DET) whereas both architectures can operate on either a regulated or an unregulated bus (Wertz and Larson, 2005). However, for the utilization on a miniature spacecraft in low Earth orbits Clark et al. (2008) suggest that the most efficient topology is PPT operating on an unregulated bus. The basic architecture of this topology is illustrated in figure 3.1.

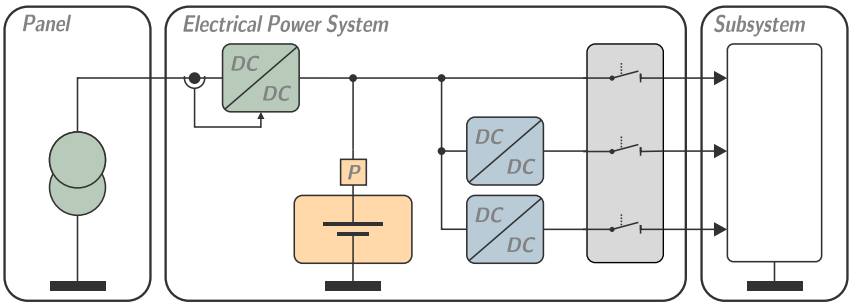


Figure 3.1: EPS architecture for pico-satellites with PPT topology and unregulated bus. The diagram shows individual blocks for power generation (green), storage (orange), as well as conversion (blue) and distribution (grey) to the subsystems.

The architecture is constructed around a battery (here shown with protection circuit) which defines the bus voltage of the unregulated power bus. The battery acts as a buffer storing exceeding power produced by the solar cells and providing energy during eclipse or whenever instantaneous peak power requirements can not be accomplished by the solar power alone. This configuration allows maximum efficiency during eclipse as no power conversion is necessary to discharge the battery on the bus.

Various specific power systems have been implemented in the context of recent small satellite projects. Some of them became available on the market as generic electrical power systems for pico- and nano-satellites. In particular, the CubeSat Kit™ Liner EPS (Pumpkin, Inc., 2012), the NanoPower (GOMSpace, 2014b), and the CubeSat Power (Clyde Space, 2012b) belong to the most established commercial systems (Agasid et al., 2014) and are presented in the following.

CubeSat Kit™ Liner EPS

As one of the first commercial power systems available for pico- and nano-satellites the CubeSat Kit™ Liner EPS provides basic functionality for power storage and conversion (see figure 3.2). Centered around two (four) serial connected Li-poly batteries with 1500 mAh capacity each and built-in under-voltage, over-voltage, and over-current protection, the Linear EPS provides an unregulated battery bus of $6-8.2\,\mathrm{V}$ ($12-16.4\,\mathrm{V}$) to the satellite.

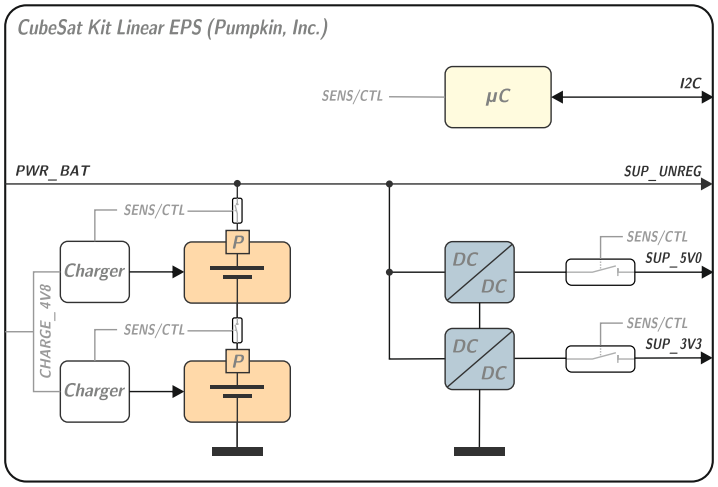


Figure 3.2: EPS architecture of the CubeSat Kit Linear EPS (Pumpkin, Inc., 2012).

In addition, the device implements two independent regulated buses which are supplied by two low-dropout regulators for central conversion of 3.3 V and 5 V respectively. Each regulated bus is further protected by a current limited switch. An onboard microcontroller provides relevant monitoring and control capabilities via an I^2C compatible interface.

The Liner EPS does not directly include any built-in power generation circuit such as for interfacing solar cells. Instead, two separate charger circuits are provided to re-charge the disconnected batteries in parallel when supplied by an external voltage source (e.g. via USB by ground support equipment).

NanoPower (P31u)

The NanoPower EPS in principal implements the basic PPT architecture with unregulated battery bus as depicted in figure 3.1. As shown in figure 3.3, a fixed number of three peak power tracker circuits is directly implemented on the board. Two series connected Li-ion batteries with 2600 mAh total capacity and battery protection circuit supply the unregulated power bus within a voltage range of $6-8.4\,\mathrm{V}$.

Beside the unregulated bus, two independent buck-converters provide regulated 3.3 V and 5 V whereas a fixed set of power distribution switches with latching current limiters control six individual regulated power lines for particular subsystems. A central embedded microcontroller with I^2C compatible interface is responsible for peak power tracking control, power monitoring, and power distribution control.

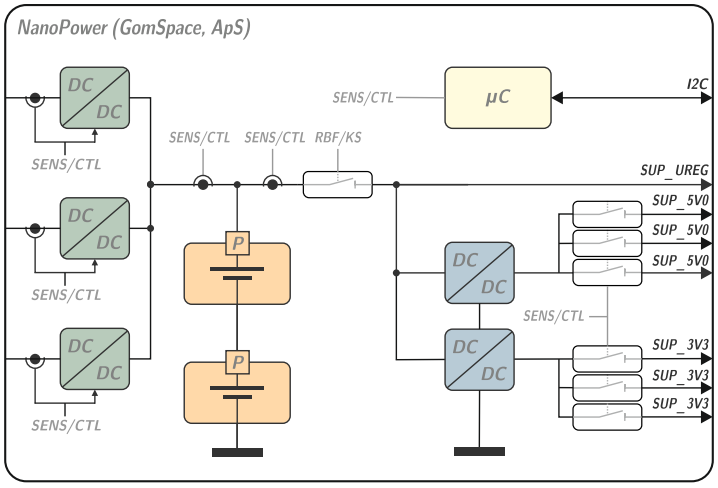


Figure 3.3: EPS architecture of the NanoPower EPS (GOMSpace, 2014b).

CubeSat Power (2s1p)

Similar to the NanoPower, the CubeSat Power EPS implements the basic PPT architecture with unregulated battery bus whereas a two series cell Li-poly battery with 1250 mAh total capacity provides 7.4 V nominal unregulated bus voltage. Beside cell balancing and protection circuits, the battery daughter board accommodates a thermostatically controlled battery heater. (Clark et al., 2008)

In contrast to the block diagram depicted in figure 3.3 the CubeSat Power EPS implements only single protection switches for the unregulated and the regulated power lines. Further power distribution for power control, protection, and monitoring of up to 24 individual subsystems is implemented on a separate power distribution board.

3.2 Concept of a Flexible and Redundant EPS

None of the electrical power systems presented implements inherent redundancy for power generation, storage, conversion or distribution. In fact, several components such as central microcontrollers or batteries constitute critical single point of failures. As a pico-satellite

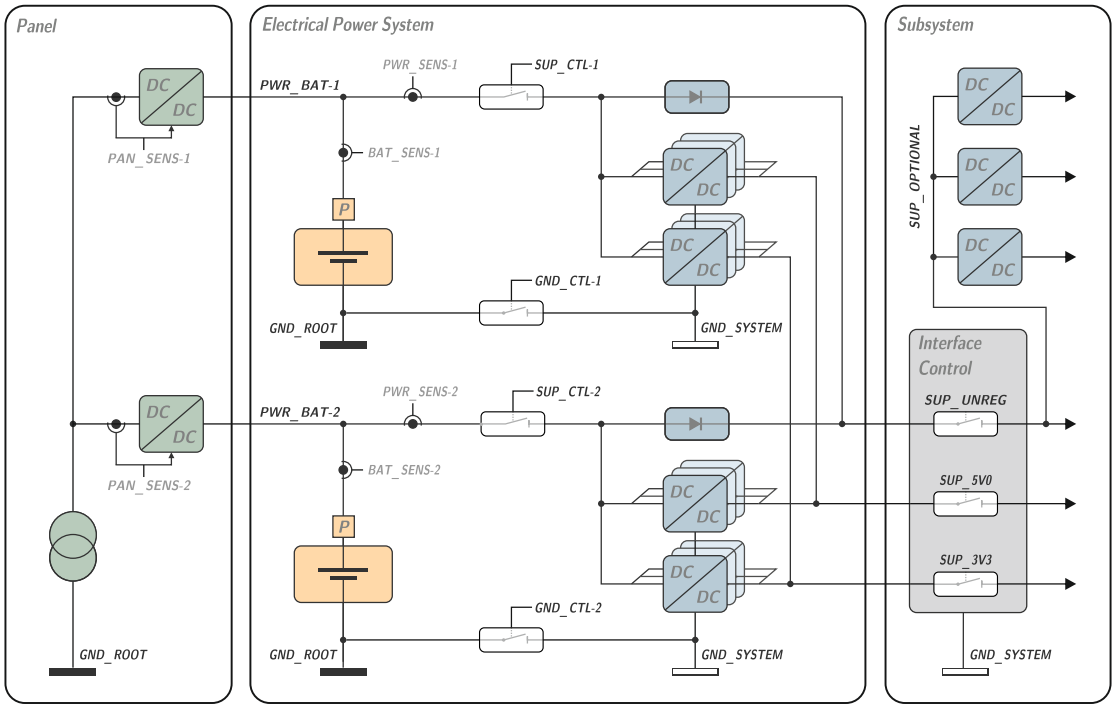


Figure 3.4: Distributed architecture of the UWE-3 Electrical Power System.

can usually not afford to double complete subsystems due to mass and space constraints, a miniature EPS for pico-satellites has to include redundancy already on component level. Thus, by alternatively supporting parallel and exclusive operation of redundant components, a smart design can provide combined performance with graceful degradation.

Considering the specified requirement for scalability and flexibility in a modular architecture, the integrated design of an EPS in a single module is not optimal as different components of the EPS scale with different mission requirements. Looking at the power generation part which typically comprises solar cells and a peak power tracking unit, it can be seen that it scales with the number of solar panels available. This is especially true, when the individual solar arrays deviate in temperature or solar irradiation due to a different alignment on the satellite. The power storage, which comprises mainly the batteries and the corresponding protection circuits, is more likely to scale with the total power requirements and the overall mission scenario in terms of eclipse times. Power distribution simply scales with the number of subsystems available, whereas the power conversion again scales with the peak power requirements of the individual subsystems.

For this reason a distributed topology was selected for the architecture of the UWE bus. As it can be seen in figure 3.4, the power generation part of the EPS is located on the multifunctional side panels and is therefore closely coupled with the solar cells. A

default power conversion block is provided on the central electrical power module board to generate most common bus voltages. Additionally, each subsystem might generate any required supply voltage directly from the unregulated bus. The power distribution can be distributed among the subsystem modules such that each subsystem can be supplied by the same power lines while the performance of the distribution block can be optimized to the requirements defined by the individual subsystem. The power storage is located on the central subsystem module as battery systems can be handled more efficiently in a single centralized manner regarding energy-mass-ratio of available batteries and supporting components for mechanical, thermal and electrical protection.

The overall EPS design for the UWE-3 bus comprises two complete independent power paths for redundancy reasons. In nominal operation only one path contributes power while the other path is in stand-by or battery charge and maintenance state. However, both power paths should be able to supply the bus simultaneously for high power requirements or emergency modes. Additionally to the redundant power paths further redundancies come along with the parallelized nature of the power converters.

3.3 EPS Implementation for UWE-3

The described concept of a distributed EPS has been implemented for the UWE-3 pico-satellite bus whereas special care has been taken to seamlessly integrate the system into modular plug-and-play paradigm of the satellite architecture. Figure 3.5 shows a picture of the power storage board implementing two fully redundant power paths in terms of storage and default power conversion capacity. The implementation of the redundant and distributed power generation is located on the satellite's multifunctional side panels shown in figure 3.6. The following sections describe relevant details related to the implementation of power generation, storage, conversion and distribution.

3.3.1 Power Generation

The architecture's power generation is located on the side panels of the satellite bus. Two triple junction Ga-As cells are directly mounted on a panel, connected in series by the panel's electronic layers (see figure 3.6, left). Each panel takes account for proper peak power tracking of their solar cells and feed the generated power to the redundant battery buses. Thus, all six individual panels contribute to the total power generated in an independent and loosely coupled manner. This introduces a high level of redundancy and enables graceful degradation of the power generation system in case of any malfunction on

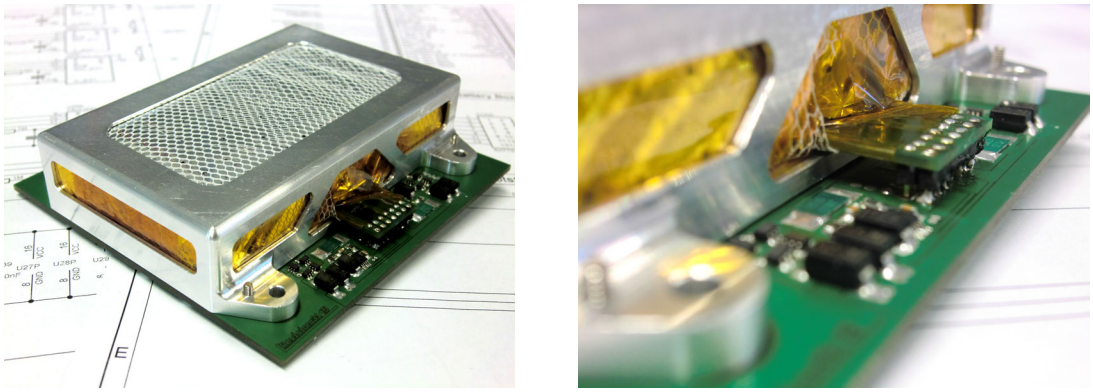


Figure 3.5: Picture of the power storage module of the UWE-3 bus.

a panel.

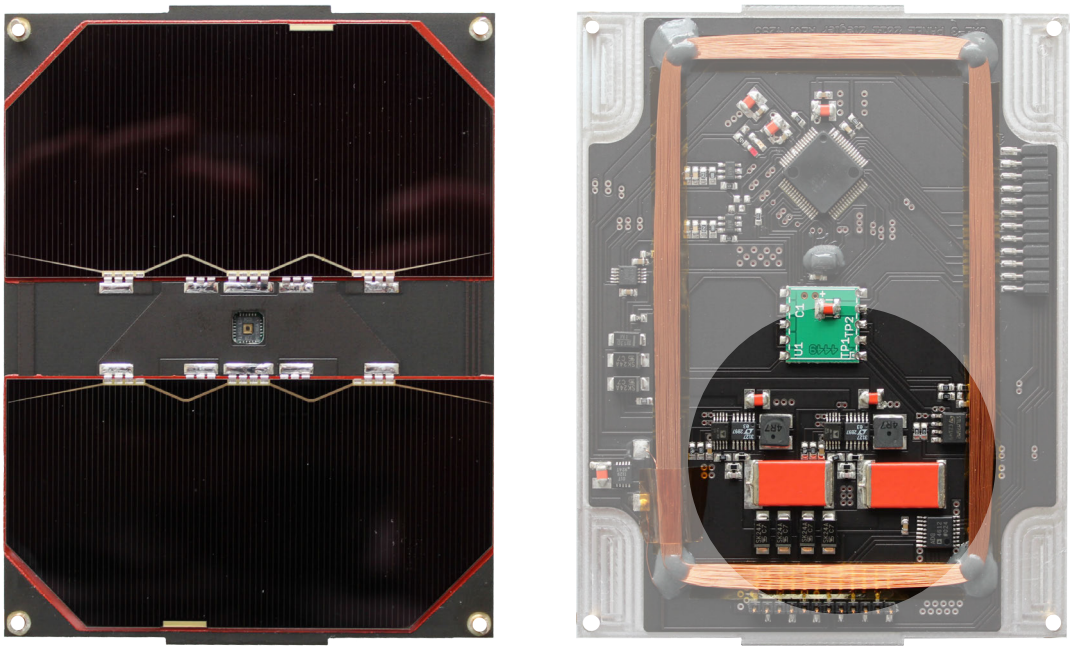


Figure 3.6: Multifunctional side panel with mounted solar cells on the top side and redundant peak power tracking circuits for both independent power paths implemented on the back side.

The relatively small currents on a single panel allow the utilization of multiple compact and efficient power converters, such that each panel can supply both redundant power paths independently (see figure 3.6, right). As the solar array voltage, when operating at the maximum power point, is higher than the maximum battery voltage for the entire range of expected panel temperatures, a highly efficient DC/DC converter with step-down topology can be used for maximum power point tracking.

As a single panel is typically exposed to individual irradiation and temperature conditions due to the geometry of the satellite, the peak power tracking algorithm is implemented directly on the panel such that optimal performance can be achieved for each panel separately. In order to account for potential rapidly changing conditions the panel's embedded controller adopts the Incremental Conductance (INC) peak power tracking method (see Reisi et al. 2013) to efficiently control the power converters which feed the generated power to the unregulated battery buses.

3.3.2 Power Storage

The power storage module itself carries two redundant Li-Ion batteries with 2.6 Ah each. The batteries are mounted on a separate board which accommodates further electronics for battery protection, power and temperature monitoring, fuel gauging and thermal control (see figure 3.7). The embedded board itself is mounted on the power storage module with a lightweight support structure. Being thermally insulated by several layers of Multilayer Insulation (MLI) the heat transfer to the carrier board is reduced to the electrical connection (see figure 3.5, right).

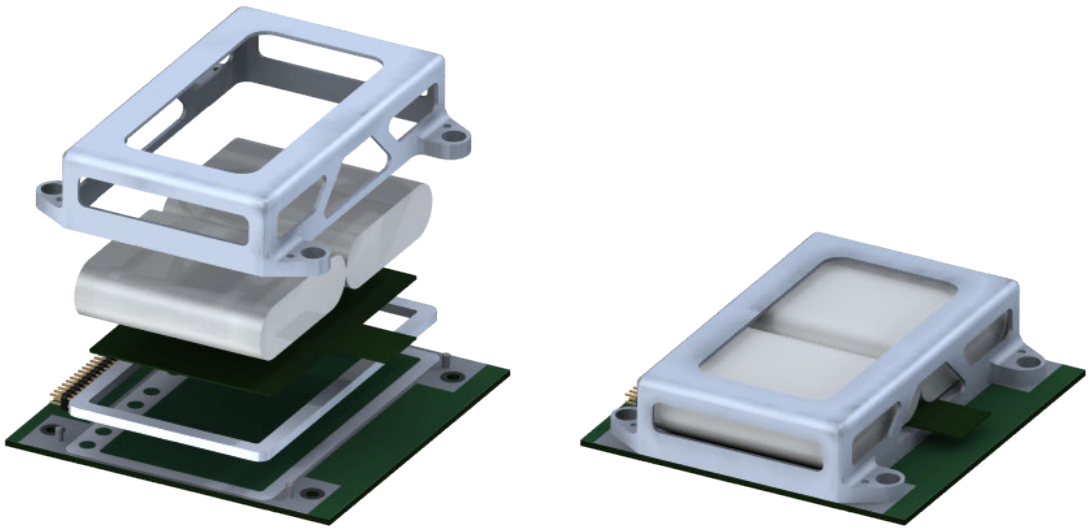


Figure 3.7: Exploded view drawing of the energy storage module carrying two redundant Li-Ion batteries inside a thermally insulated structure.

As both redundant battery paths are directly routed to the backplane the total capacity available in a satellite configuration can easily be extended by plugging another power storage module into the bus to operate the batteries in parallel.

Quad-redundant main switches in a series-parallel topology allow to reliably switch on and off the power bus for each battery such that the entire satellite can be power cycled. The switches are controlled by dedicated I/O lines (SUP_CTL) on the backplane. Timer circuits ensure that the switches are closed by default as long as the signal on the SUP_CTL lines remain constant for a certain time.

3.3.3 Power Conversion

The design of the modular EPS architecture allows for a parallelized power conversion. This topology provides an additional level of redundancy and further supports spatial distribution of heat dissipation, thus avoiding hotspots in centralized high power components.

The power conversion design for the UWE bus utilizes Low-Dropout Regulators (LDOs) for the generation of the 3.3 V. As the nominal voltage of the unregulated bus stays within 3.4 V to 3.9 V, the conversion efficiency does not drop below 85 % which renders the solution as a good compromise. For the generation of the 5V bus a parallelized configuration of charge pumps is used due to their simple and robust working principle and extreme compact footprint. These devices can provide stable output voltages at reasonable efficiency of about 70 % for comparatively high currents.

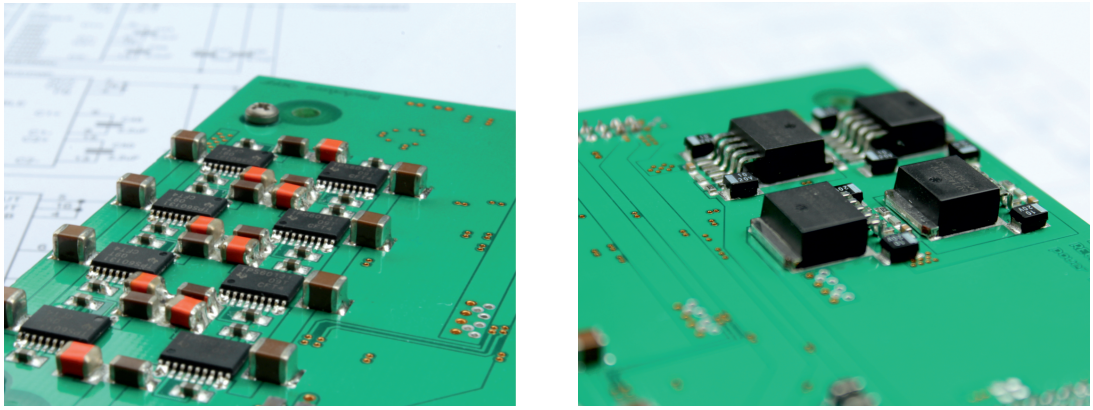


Figure 3.8: A cluster of multiple parallelized charge pumps (left) and LDOs (right) enable high power voltage conversion in a compact and continuously scalable manner and further efficiently distributes heat dissipation to avoid thermal hotspots.

A set of power converters is located on the power storage subsystem in order to provide a default conversion capacity of 2 x 6.0 A on the 3.3 V bus and 2 x 1.2 A on the 5 V bus. Figure 3.8 shows a cluster of parallelized charge pumps (left) and parallelized low-dropout regulators (right) implemented on the bottom side of the power storage board.

3.3.4 Power Distribution

The main role of the power distribution system of a spacecraft is to provide load monitoring and control for the individual subsystems and to protect them from over-voltage, under-voltage and over-current conditions, for example caused by latch-ups in the device. In contrast to many traditional large satellites and also in contrast to available commercial power systems for small satellites, such as the PDM (Clyde Space, 2012a), the NanoPower (GOMSpace, 2014b), or the XEPS (BCT, 2014), the power distribution of the UWE-3 EPS is implemented in a distributed way.

Besides the unregulated battery bus also 3.3 V and 5 V power lines are available to the subsystems to be able to supply most types of electrical components. The power buses are distributed to the subsystems via shared power lines on the backplane, while individual power switches with monitoring and protection circuits are directly located on the individual subsystem modules. This topology reduces the number of power lines required on the backplane and ensures that the power distribution capabilities scale with the number of subsystems, being always optimized to their individual requirements.

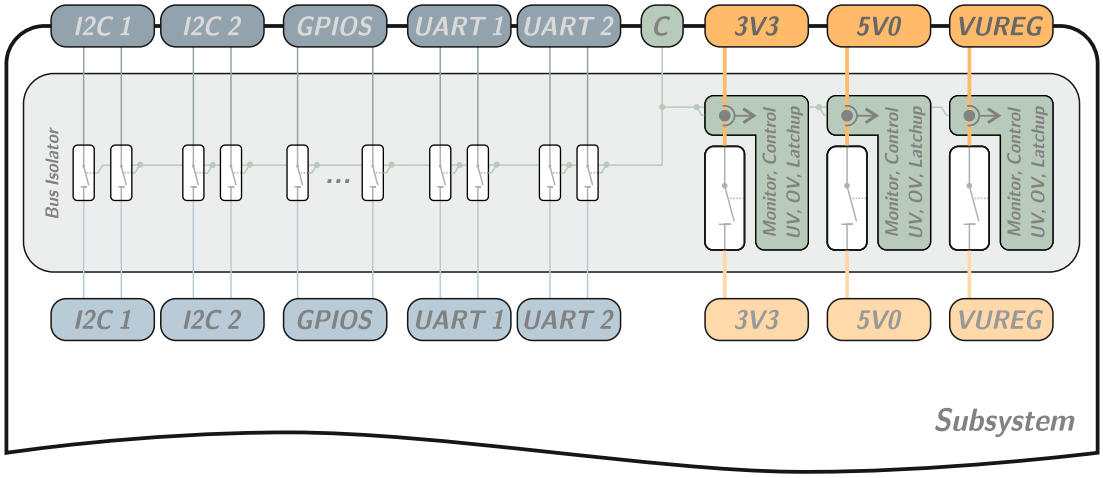


Figure 3.9: UWE-3 standard subsystem interface (module interface controller) with bus isolators and power monitor, control and protection.

A standard interface circuit, the so-called module interface controller, has been defined to be implemented on each subsystem of the satellite. A block diagram of the circuit which controls all relevant power and data lines connected to the backplane is shown in figure 3.9. The individual power control circuits are build around a configurable hotswap controller which itself serves the gate of an n-channel power MOSFET realizing the power switch. Beside power switching, voltage and current monitoring, and fault protection the circuit implements a current rate controlled soft-start to enable proper switching of high capacitive

loads.

In order to ensure that a subsystem can be completely powered down while other subsystems connected to the backplane are still operating on shared data lines, the module interface controller provides electrical isolators for each relevant data signal used on a subsystem. Robust analog switches with over-voltage and power-off protection guarantee that all data lines are high impedance when no power is supplied to the subsystem. Thus, it is ensured that no parasitic current paths, e.g. via standard CMOS ESD protection diodes, prevent the circuit from properly powering down or even cause permanent damage to the device. Further, the protection switches can be used for fault isolation in case a subsystem causes unintentional interferences on the signal bus.

Both, bus isolators and power monitoring and control circuits can be accessed via a digital interface on the backplane to be operated remotely by the satellite's onboard computer.

3.4 Verification Tests

Design and proper dimensioning of the electrical power system is one of the most crucial tasks related to satellite engineering. As all other subsystems directly depend on its service it is obvious that a severe failure of the EPS can quickly result in total mission loss. Beside extensive simulation, adequate testing of the hardware is essential to verify the system's performance before launch. The necessity for intensive testing is even more important for small scale satellite systems. According to Clark et al. (2008) the power system belongs to the most common failure sources for CubeSat projects in the last decade.

Small scale satellite projects are typically challenged by extremely limited energy budgets. In order to support experiments with higher power requirements, the mission plans often allow to operate the satellite in negative power budgets for some orbits. Hence, the power consumption is considerably varying during nominal operations. Temporarily increasing currents might further degrade conversion efficiencies and resistive path losses such as contact resistances or internal battery resistances. This is especially true for low operating voltages which is usually the case for smaller satellites. As example one can assume a combined path resistance of 120 mΩ due to contributions from load switches, shunt resistors, connectors etc. A high power operation drawing 3 A at a bus voltage of 3.6 V results in a resistive path loss of 10 %. As the limited energy available on a pico-satellite does usually not allow to provide for large safety margins, a robust power budget estimation is not trivial.

For mentioned reasons the entire hardware of the satellite's power supply chain has to be

tested carefully in order to identify its actual performance under realistic conditions. The following sections describe test procedures and results of hardware performance analysis tests conducted on the UWE-3 engineering model. Beside a setup for long-term power budget verification a power conversion performance analysis and a thermal dissipation analysis of the parallelized power converter architecture are presented in detail.

3.4.1 Conversion Performance Analysis

The UWE-3 electrical power system implements a redundant and scalable power conversion architecture based on clusters of parallelized low dropout regulators and charge pump circuits as described in section 3.3.3. Extensive tests have been carried out in order to characterize the system's performance concerning effective conversion efficiencies and inherent load distribution for the entire range of operating conditions.

The test setup is depicted in figure 3.10. The central block represents the two independent power paths, each being composed of several parallel converters. Both chains are connected to a separate programmable power supply to mimic the individual unregulated power buses at different battery charge states. A programmable load connected to the combined output represents power consumers supplied by the corresponding regulated bus.

The test sequence is executed by a MATLAB script which is responsible for monitoring and controlling power supplies and programmable load. For each configuration $C = (\hat{U}_A, \hat{U}_B, \hat{I}_L)$, specifying desired bus voltages $\hat{U}_A$, $\hat{U}_B$ and load current $\hat{I}_L$, actually measured supply voltages U_A, U_B and currents I_A, I_B of both paths are recorded together with the corresponding load measurements U_L and I_L.

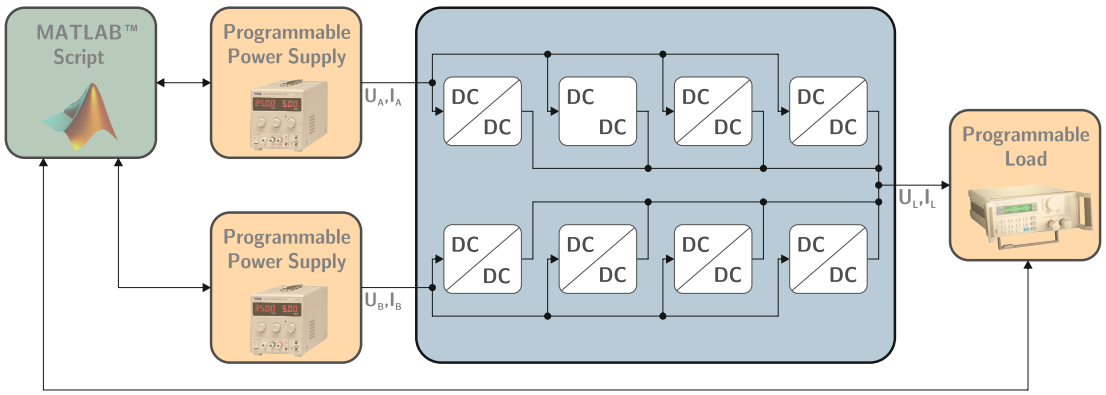


Figure 3.10: Test setup for parallel power regulator performance analysis.

Due to the automatization of the test process a large number of configurations can

be examined. Corresponding effective conversion efficiencies η and the relative power contributions α and $\beta = 1 - \alpha$ of the converter chains A and B can then be determined as follows:

$$\eta_c = \frac{U_L I_L}{U_A I_A + U_B I_B} \tag{3.1}$$

$$\alpha_c = \frac{U_A I_A}{U_A I_A + U_B I_B} \tag{3.2}$$

$$\beta_c = \frac{U_B I_B}{U_A I_A + U_B I_B} \tag{3.3}$$

For the analyzation of the 3.3 V low dropout regulator cluster a large configuration room with roughly 1500 configurations has been tested. Within several hours, the automated procedure examined all combinations of bus voltages $\hat{U}_A$, $\hat{U}_B \in \{3.40, 3.45, \ldots, 4.20\}$ [V] and load currents $\hat{I}_L \in \{0.5, 1.0, 1.5, 2.0, 3.0\}$ [A]. For the majority of the tested configuration the down-converted output voltage remained stable around 3.3 V even for very high currents. For low bus voltages and very high currents the output voltage dropped slightly due to resistive losses in the path (e.g. switches, shunt resistors, wiring, and connectors).

For the case that $U_A = U_B$ all four LDOs are operating quasi in parallel. Figure 3.11 shows the corresponding conversion path efficiency η as a function of bus voltage $U_A = U_B$ and load current I_L. It can bee seen that the conversion path efficiency drops linearly with increasing bus voltage due to the nature of linear regulators. For higher currents the path efficiency also degrades due to resistive path losses mentioned. However, for the typical operating range the efficiency remains well above $85 - 80\,\%$ for currents up to 2.5 A.

For the case that $U_A \neq U_B$ path and conversion efficiencies differ such that the load is naturally distributed among both power paths. Figure 3.12 visualizes the relative load distribution $\alpha = 1 - \beta$ depending on measured bus voltages U_A and U_B for various load currents I_L. It can bee seen that for small currents the entire load is efficiently supplied by mainly one path while the remaining devices are in stand-by. This preference is related to slight deviations in PCB design and manufacturing deviations in the devices itself. With increasing current the load distribution becomes more symmetrical being mainly determined by the ratio of bus voltages. Thus, the stronger battery would automatically take over more load.

The corresponding conversion efficiencies η are depicted in figure 3.13. As expected, for low currents the plots resemble the efficiency of the preferred path. For higher currents

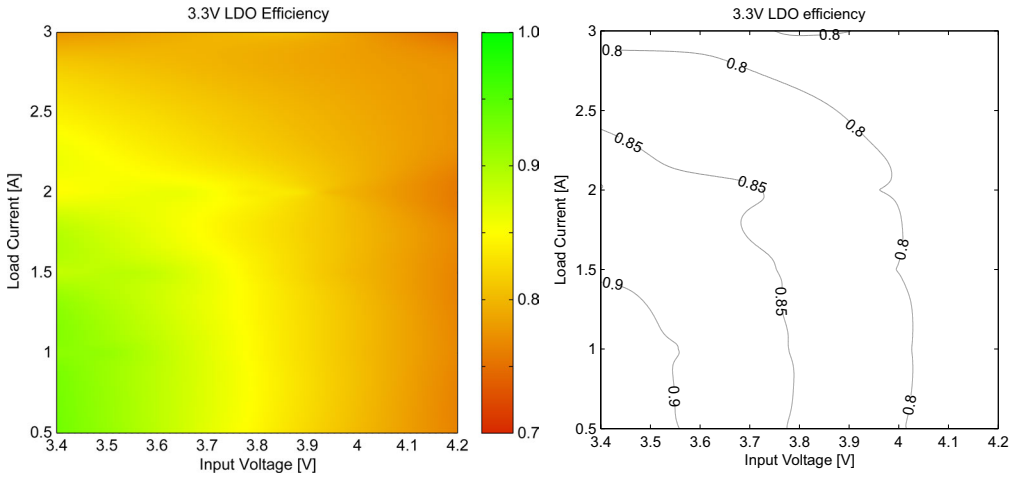


Figure 3.11: Efficiency performance of 3.3 V low dropout regulator cluster for varying input voltage $U_A = U_B$ and load I_L.

the remaining devices take over a portion of the load, resulting in a symmetric dependency of the efficiency on the bus voltages as already observed in figure 3.11.

With a similar experiment the performance of the 5 V charge pump cluster has been analyzed. In about 2300 measurements the configuration range specified by the bus voltages $\hat{U}_A, \hat{U}_B \in \{2.7, 2.8, \ldots, 4.2\}$ [V] and load currents $\hat{I}_L \in \{0.150, 0.300, 0.600, 0.900, 1.500, 2.000\}$ [A] has been examined automatically. For the entire test range the charge pumps proved stable voltage conversion showing only slight voltage drops when exceeding the combined maximum load current of 4×0.3 A as specified for the individual devices.

Figure 3.14 shows the conversion path efficiency η as a function of combined bus voltage $U_A = U_B$ and load current I_L. Due to the more complex nature of a charge pump circuit its conversion efficiency is not linear as it was the case for the LDOs. In order to assure optimal efficiency over a wide operation range the devices make use of adaptive mode switching for selective operation with different fixed conversion factors. For low currents the efficiency is around 90 % for input voltages between $3.7 - 4.0$ V, dropping to 75 % on average for lower voltages. For very high currents the efficiency degrades down to $60 - 75$ % especially for high input voltages.

Again, figure 3.15 and 3.16 show the natural load distribution $\alpha = 1 - \beta$ and corresponding conversion efficiencies η for the case that both redundant unregulated buses simultaneously supply the 5 V bus with $U_A \neq U_B$. Similar to the LDO cluster analysis it can be observed that for low currents, which can easily be contributed by a single converter device, the entire load is handled by a preferred conversion chain while the other devices are inactive. Thus, also η resembles the efficiency of a single chain independent of the

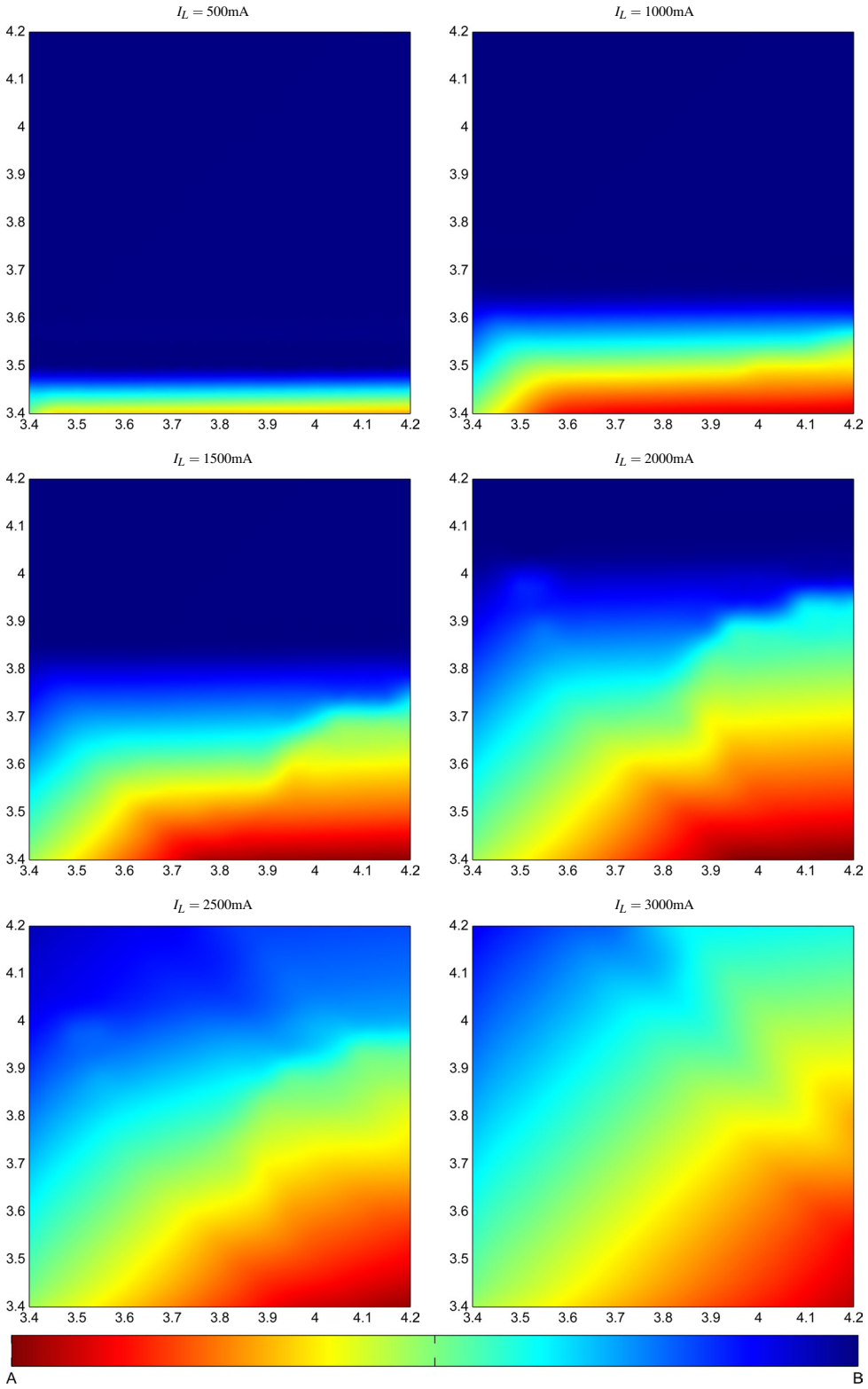


Figure 3.12: Load distribution performance of 3.3 V low dropout regulator cluster for varying input voltages U_A [V] on x-axis and U_B [V] on y-axis.

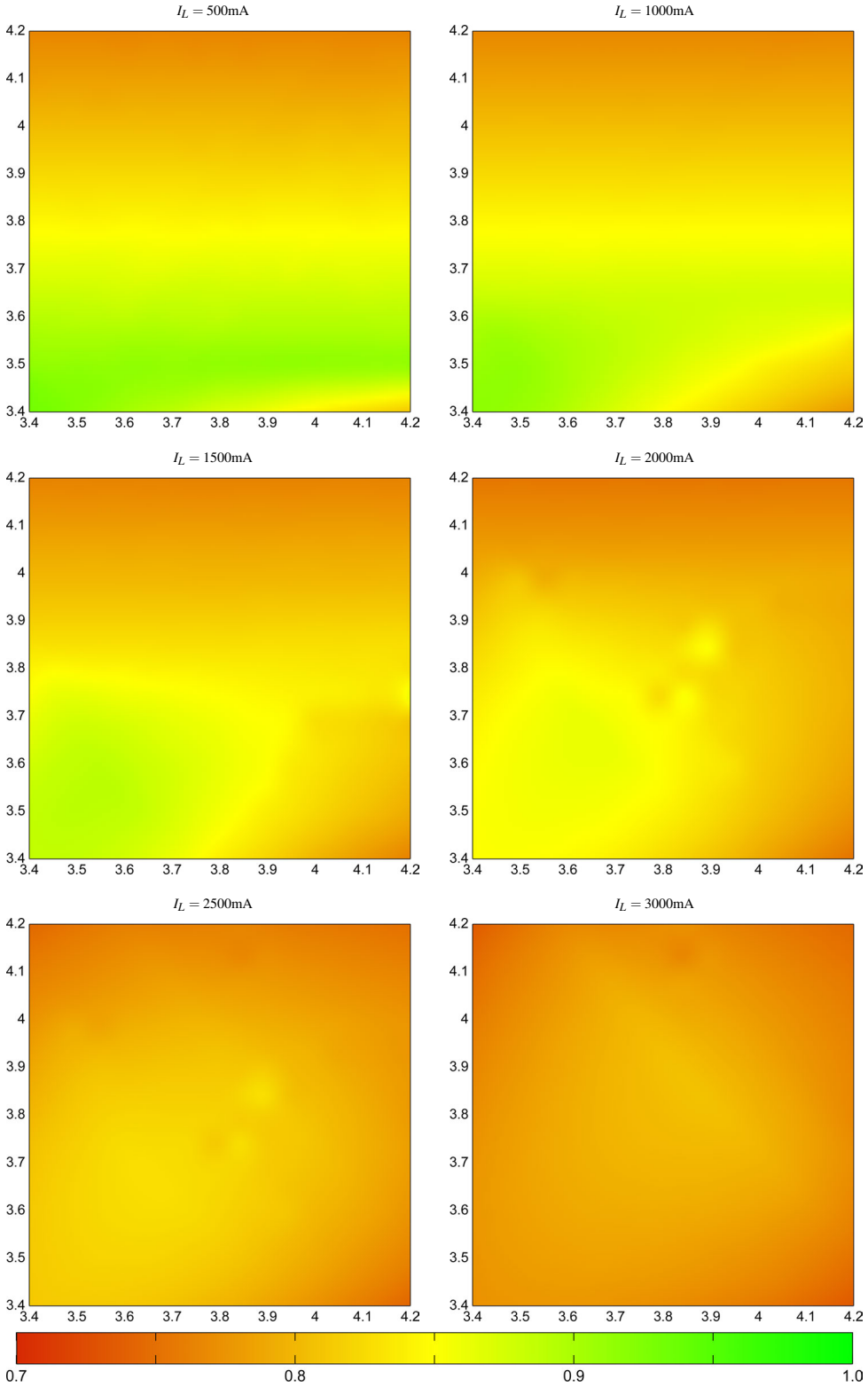


Figure 3.13: Efficiency performance of 3.3 V low dropout regulator cluster for varying input voltages U_A [V] on x-axis and U_B [V] on y-axis.

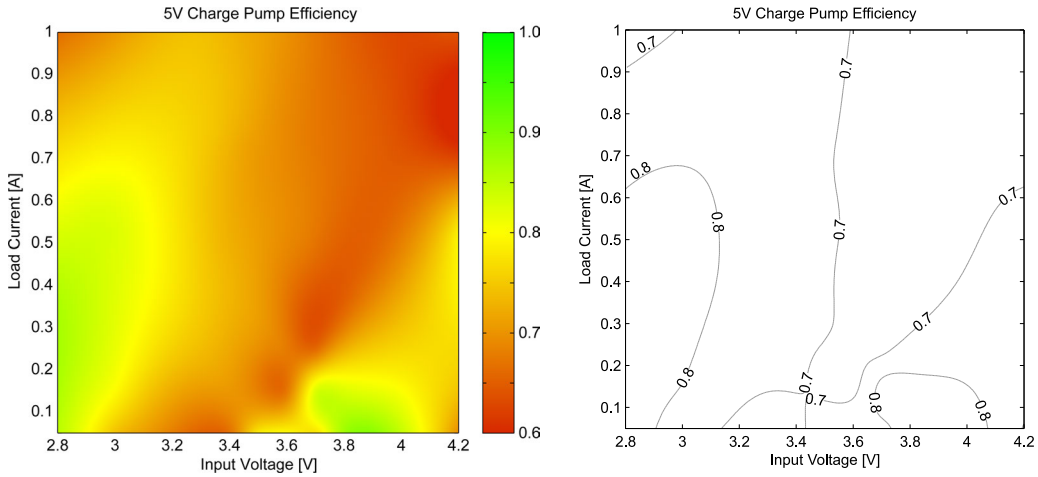


Figure 3.14: Efficiency performance of 5 V charge pump cluster for varying input voltage $U_A = U_B$ and load I_L.

input voltages. As soon as the load exceeds 300 mA the second path begins to take over a portion of the load. With increasing load both, efficiency and load distribution plots, show symmetric dependency on the bus voltages.

3.4.2 Thermal Performance Analysis

A major advantage of a distributed conversion architecture besides robustness and scalability is its natural spatial distribution of heat dissipation. It is obvious that thermal hotspots constitute a significant threat in the absence of thermal balancing by atmospheric convection. This is especially challenging when the entire load passes through single centralized circuits with moderate efficiencies. In order to demonstrate the thermal distribution for the decentralized architecture implemented several thermal imaging experiments have been conducted on the UWE-3 electrical power system.

The test setup is depicted in figure 3.17 (top, left) whereas the electrical setup has been implemented according to figure 3.10. Being operated on the flat-sat prototyping adapter the power conversion unit could be monitored with an infrared camera while altering the input voltages and electrical load connected to the board. This setup allows to visualize active components due to their thermal dissipation and allows to reveal general thermal hotspots during high power operation. Due to technical constraints these experiments have been conducted within normal atmosphere such that absolute temperatures indicated might not necessarily reflect real operating conditions in vacuum. However, the results demonstrate the advantages of distributed conversion clusters and provide detailed information on its internal operations.

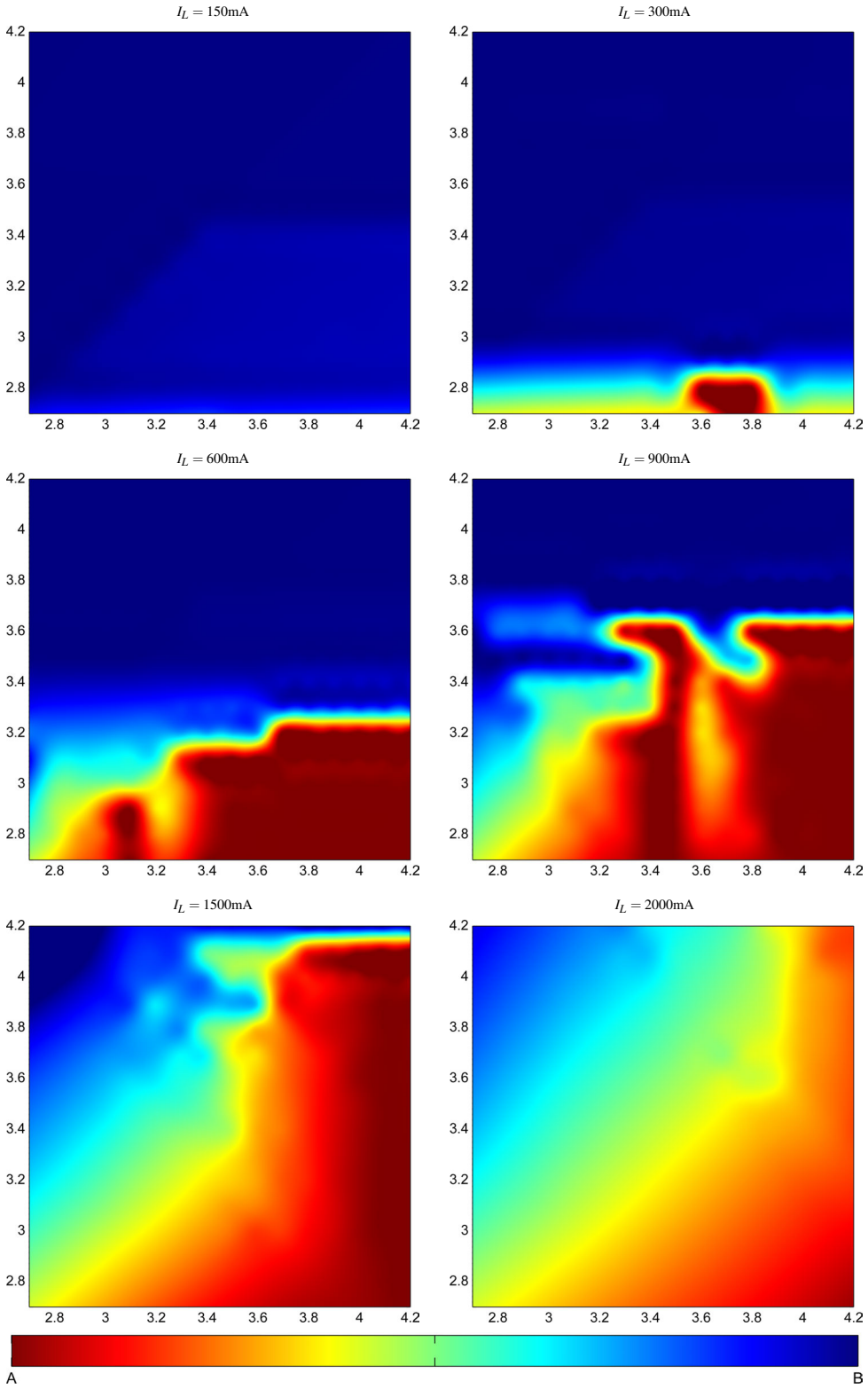


Figure 3.15: Load distribution performance of 5 V charge pump cluster for varying input voltages U_A [V] on x-axis and U_B [V] on y-axis.

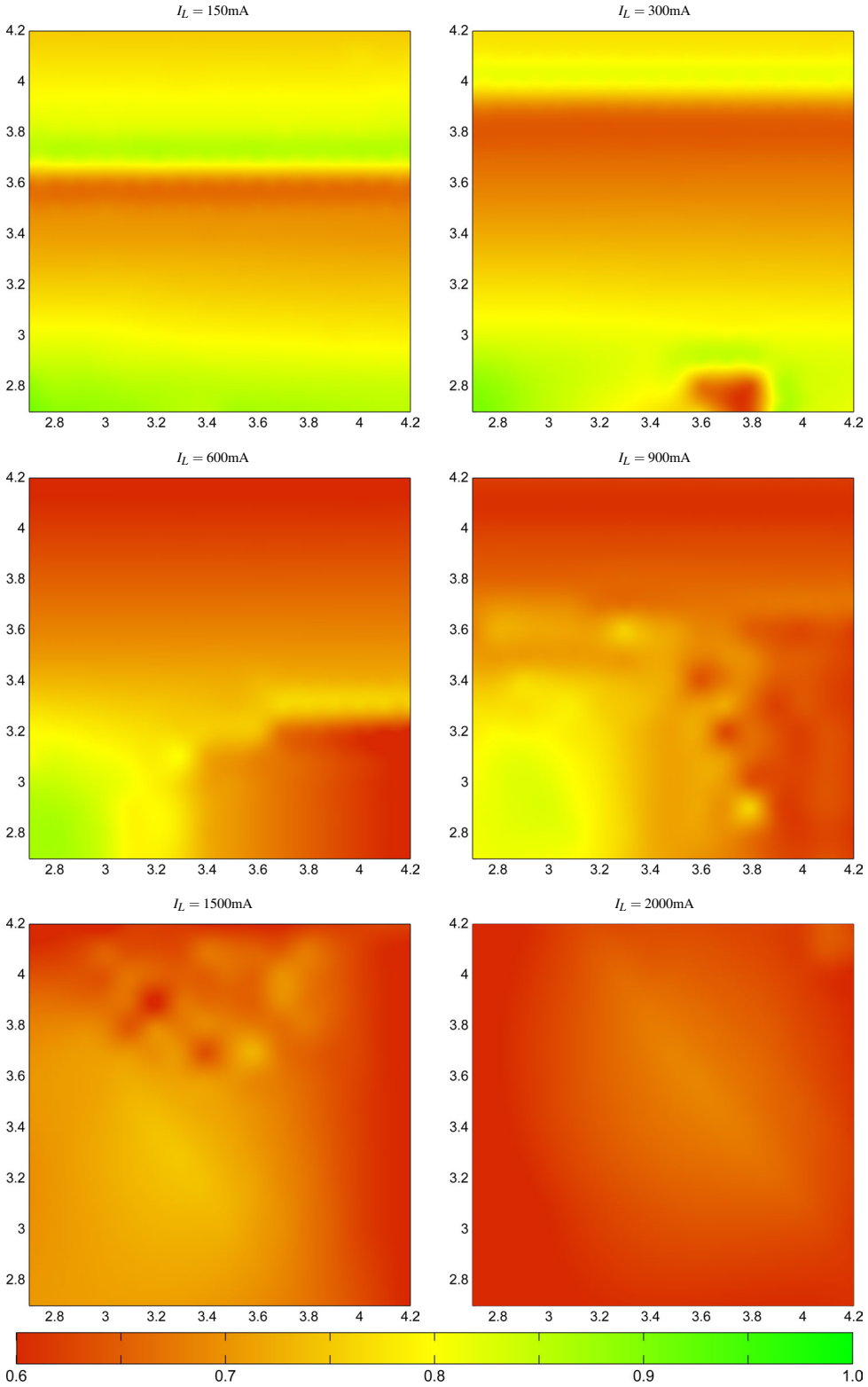


Figure 3.16: Efficiency performance of 5 V charge pump cluster for varying input voltages U_A [V] on x-axis and U_B [V] on y-axis.

For each regulated power bus two experiments have been conducted. One experiment investigates the thermal distribution for a constant load I_L and varying path voltages U_A and U_B to demonstrate the performance for inter-path load sharing. The other experiment visualizes the thermal behavior of a single path for constant voltage U_A (or U_B) with increasing currents I_L, thus demonstrating the path's performance for intra-path load sharing. Each picture presented has been acquired after fixed timespans for thermal relaxation with the load turned off followed by a thermal settling time after activation of input voltages and electrical load.

Figure 3.17 shows the results of the charge pump cluster experiment for inter-path load sharing. In order to ensure a significant thermal response of the majority of the devices a high load current of 2 A has been chosen. The first picture (top row, right) shows the thermal response for equal input voltages $U_A = U_B = 3.45\,\mathrm{V}$. It can be seen that about five to six out of eight converters are active whereas the load is more or less equally distributed among both paths. With changing input voltage ratio it can be observed that the load distribution becomes asymmetric such that the path providing higher bus voltage dominates. With increasing load on a single path more converter devices on it become active. The middle row shows the load transition to path B, the bottom row shows the load transition to path A respectively. The images further visualize the thermal response of the quad-redundant main switches for path A (bottom row, top left location) and path B (middle row, top right location).

The results from the intra-path load sharing experiment of the charge pump cluster are presented in figure 3.18 and figure 3.19. The image series show the single path thermal response to varying loads I_L at fixed input voltages. The thermal images clearly show how the number of active converter devices increases with the load. Starting with only one active device for $I_L = 150\,\mathrm{mA}$ finally all devices become active for the maximum load of $I_L = 1.5\,\mathrm{A}$. In principle, both paths show similar behavior. However, the order of activation of the individual converters depends on input voltage, board design and device specific deviations.

Similar experiments have been conducted to demonstrate the inter and intra path load sharing of the 3.3 V low dropout regulator clusters. Figure 3.20 shows the cluster's thermal response to varying input voltage ratio at constant load to demonstrate equal load sharing (middle, $U_A = U_B$), and the exclusive load transition to path A only (left, $U_A >> U_B$) and to path B only (right, $U_B >> U_A$).

Figure 3.21 indicates the intra-path load sharing of the parallel LDOs on path A with constant input voltage $U_A = 4.2\,\mathrm{V}$ and increasing load $I_L \in \{0.5, 1.5, 2.5\}$ [A]. It can be seen that with increasing load the thermal activity of a single device increases initially

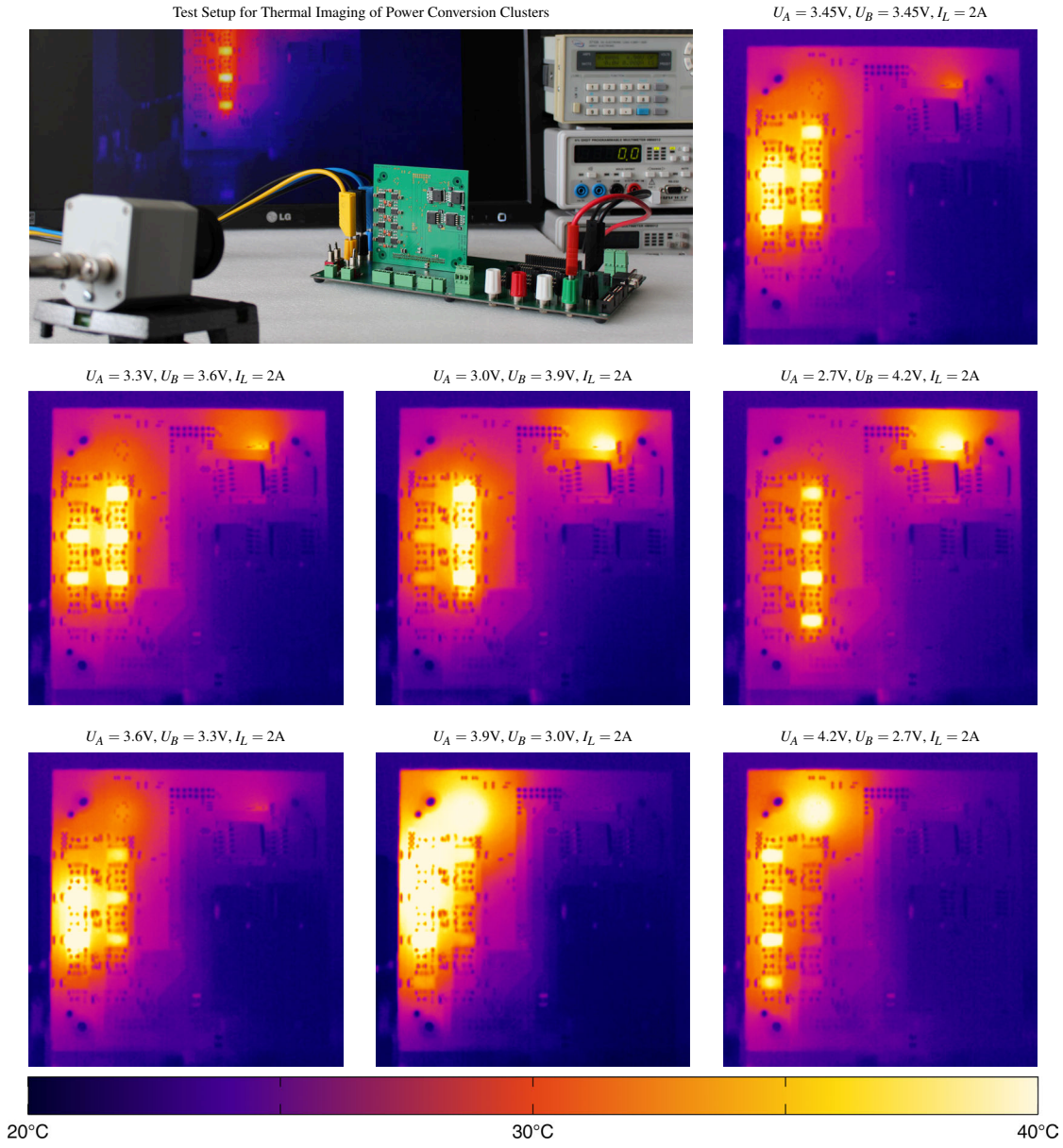


Figure 3.17: Thermal distribution performance of 5.0 V charge pump cluster for varying input voltages U_A and U_B with constant load I_L.

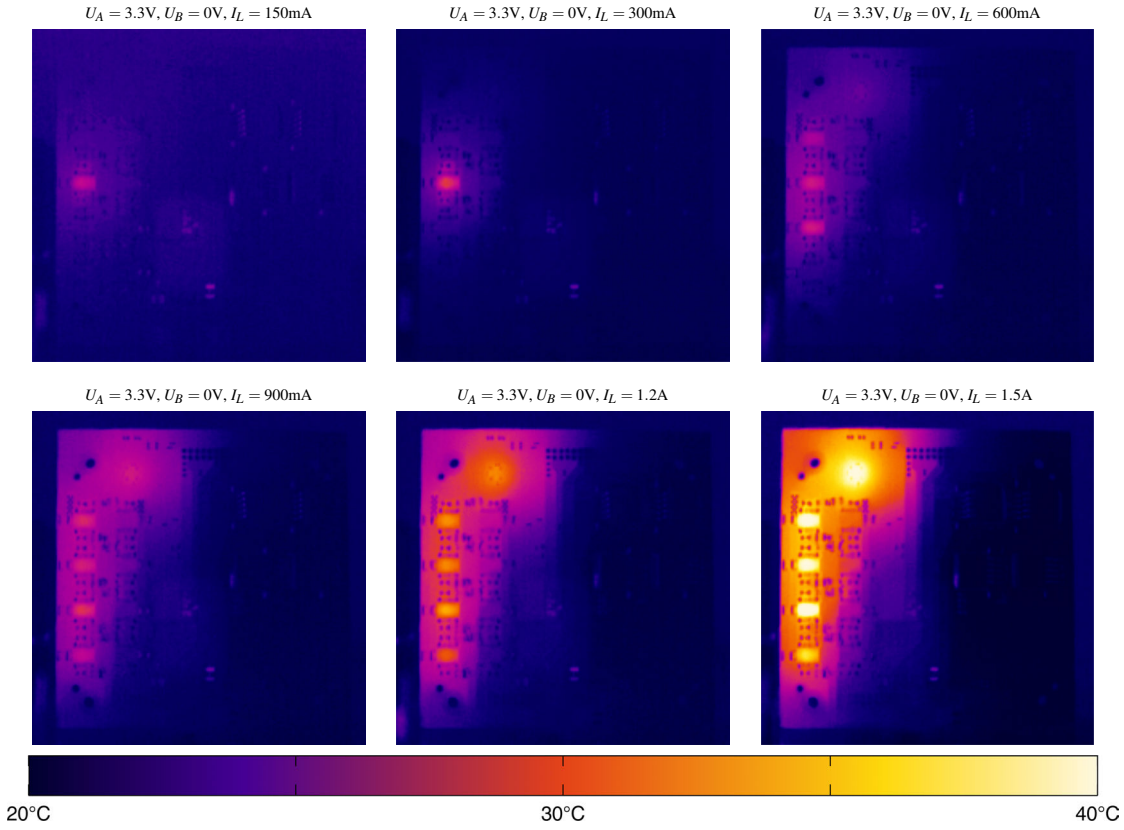


Figure 3.18: Thermal distribution performance of 5.0 V charge pump cluster chain A with constant input voltage $U_A = 3.3\,\text{V}$ and varying load I_L.

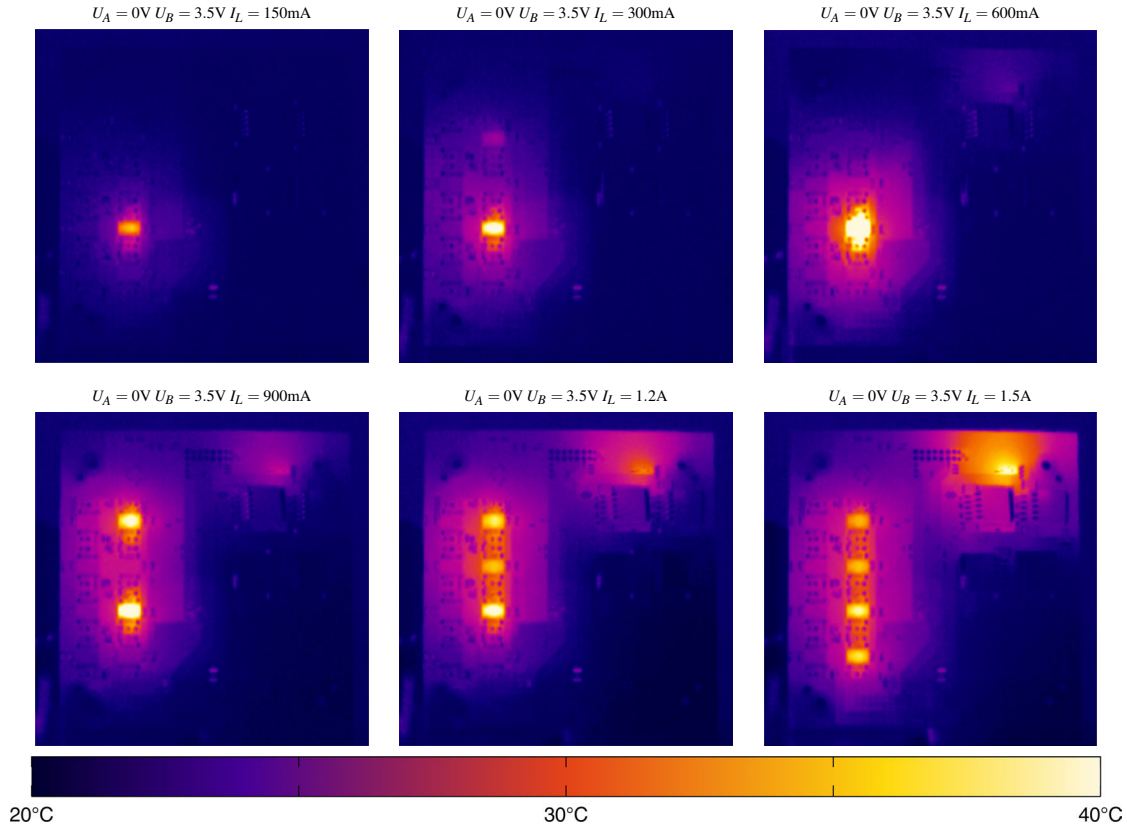


Figure 3.19: Thermal distribution performance of 5.0 V charge pump cluster chain B with constant input voltage $U_B = 3.5\,\text{V}$ and varying load I_L.

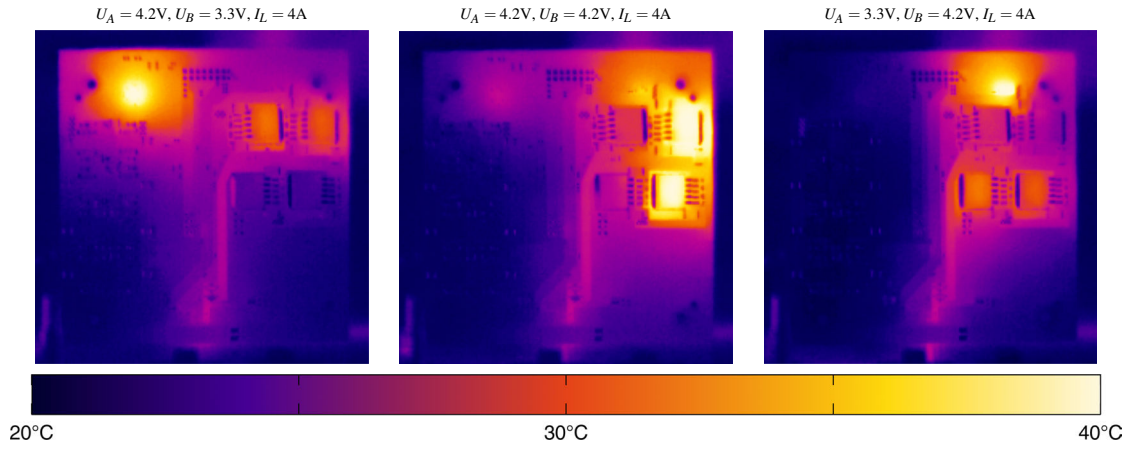


Figure 3.20: Thermal distribution performance of 3.3 V low dropout regulator cluster for varying input voltages U_A and U_B with constant load I_L.

before part of the load is transferred to the secondary device for higher loads, thus reducing the thermal dissipation of the first device.

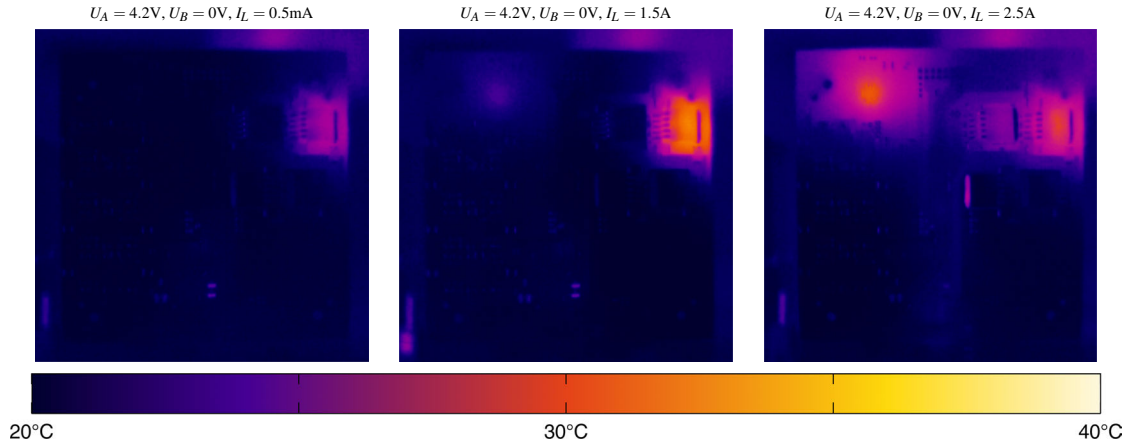


Figure 3.21: Thermal distribution performance of 3.3 V low dropout regulator cluster chain A with constant input voltage $U_A = 4.2\,\text{V}$ and varying load I_L

3.4.3 Power Budget Verification

Power budgets of very small satellites are usually constrained by the satellite's dimension as they do not possess large solar panels and active attitude control for continuous sun pointing. In order to efficiently utilize the limited energy available, sophisticated power strategies have to be developed. However, a robust power budget estimation is usually very difficult. Efficiencies of peak power trackers might degrade with higher spinning rates of the satellite while efficiencies of power converters and high power paths might vary significantly with higher currents for the comparatively small bus voltages. Testing the power budget in a hardware-in-the-loop configuration can help to verify the power strategy despite mentioned uncertainties.

For the hardware-in-the-loop evaluation of peak power tracking efficiency and long-term power management strategy, realistic conditions regarding varying temperature and irradiance of each solar panel have to be emulated physically. Fortunately, the low power nature of pico-satellites allow to use compact and cost-efficient hardware setups. The UWE Solar Cell Emulator (see figure 3.22, right) has been developed to mimic the characteristic behavior of small photovoltaic arrays under realistic time varying conditions of typical pico-satellite operation scenarios.

The emulator's hardware design is straight forward as it can be seen in the block diagram shown in figure 3.22 (left). The setup is designed around a linear power operational

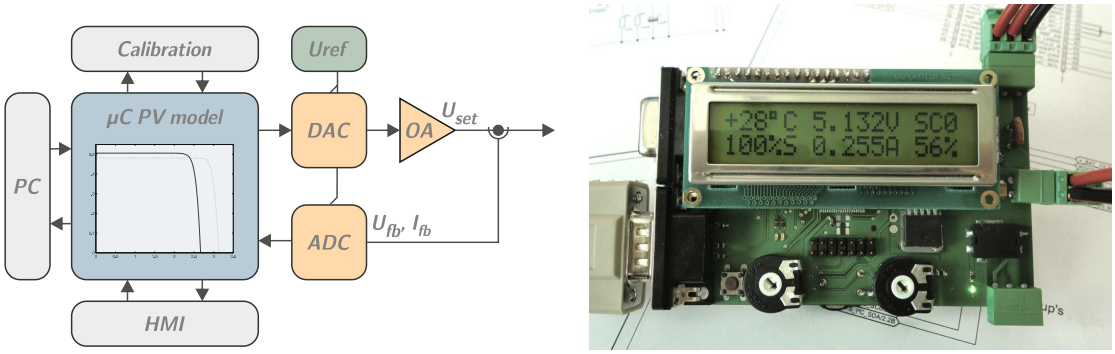


Figure 3.22: Block diagram of the photovoltaic emulator (left) including PC interface, persistent calibration memory (Calibration), interface for stand-alone operation (HMI), reference voltage source (U_{ref}), analog-digital converters (DAC, ADC), power operation amplifier (OA) and the sense circuit which generates the current and voltage feedback U_{fb} and I_{fb}. Emulator hardware in a functional configuration (right).

amplifier configured in a simple non-inverting amplifier configuration. A low-pass filter with designed cut-off frequency of about 1 KHz stabilizes the output signal by suppressing higher frequency noise. The input signal of the amplifier is provided by a precise digital-to-analog converter with temperature compensated reference voltage U_{ref}. The same voltage reference is used by a fast analog-to-digital converter measuring the instantaneous load current I_{fb} and voltage U_{fb} as a feedback to a microcontroller.

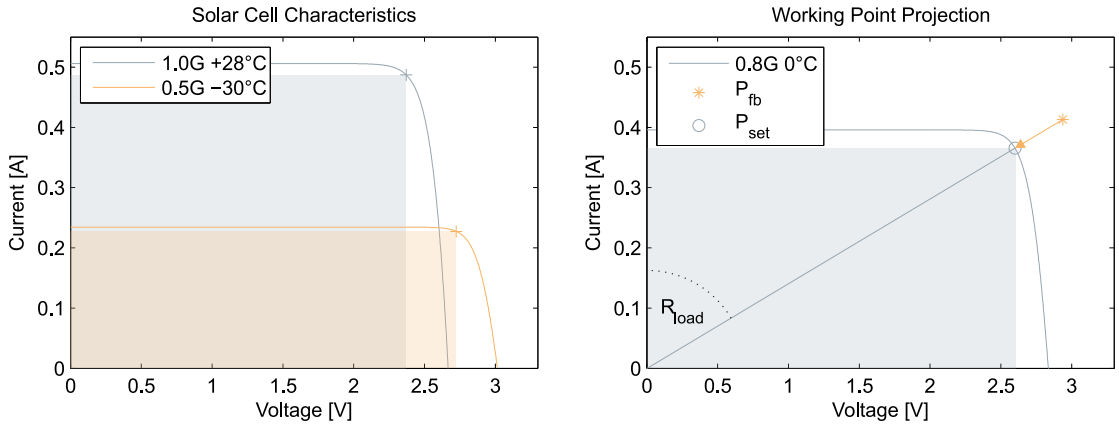


Figure 3.23: Characteristic curves of a single solar cell with maximum power points for different temperatures T and irradiations G (left). Deriving the emulators output voltage U_{set} by projecting the instantaneous working point P_{fb} onto the cells UI characteristic curve according to the equivalent load resistance R_{load} (right).

The digitalized signals are used by a software model on the microcontroller which closes the control loop. The software model can represent any function which generates a desired

output voltage U_{set} from the load measurement (U_{fb}, I_{fb}). The embedded photovoltaic model implemented bases on a single exponential photovoltaic model introduced by Walker (2001). The model incorporates cell temperature T and solar irradiation G as well as cell specific parameters from the manufacturers datasheet to calculate the UI characteristic curve.

The model implementation is optimized to enable on-the-fly calculation of the load equivalent working point (U_{set}, I_{set}) from the measured load. First, the instantaneous load measurement (U_{fb}, I_{fb}) is projected onto the characteristic curve using the equivalent load resistance $R_{load} = U_{fb}/I_{fb} = U_{set}/I_{set}$ as illustrated in figure 3.23 (right). The corresponding operating voltage U_{set} can then be calculated using a re-parameterized form of Walker's single exponential photovoltaic model.

A control and configuration interface allows simultaneous access to multiple emulators in a daisy-chain configuration via a MATLAB interface. Thus, arbitrary dynamic scenarios can be simulated to perform hardware-in-the-loop verifications of pico-satellite power management systems.

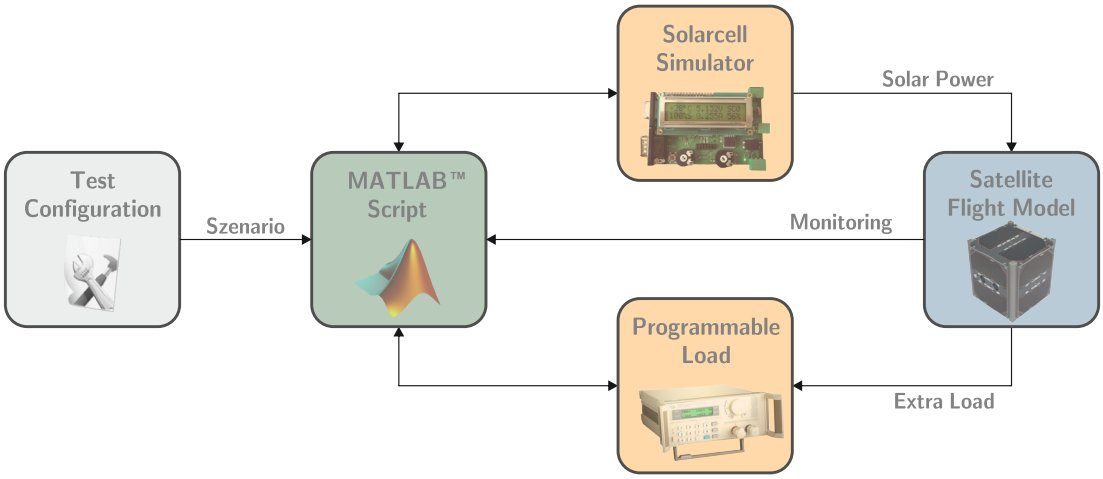


Figure 3.24: Test setup for long term power budget verification.

The photovoltaic emulator has been used frequently throughout the development of UWE-3 in various automated tests in order to verify the PPT operation and to determine and verify the effective power budget on the satellite. The principle test setup for power budget verification is depicted in figure 3.24. The satellite's peak power tracking circuits are supplied by photovoltaic emulators which are controlled by a MATLAB script to simulate typical orbit scenarios of a spinning pico-satellite defined in a test configuration file. A programmable load connected to the individual power buses on the satellite can simulate extra power consumption on the bus. During test execution the script monitors the

PPT performance indicated by the emulator, the power bus voltages and battery parameters provided by the satellite itself, and further measurements obtained by the programmable load.

During several long term tests, each lasting several days, the setup could automatically determine the maximum extra load on the individual buses such that the total power budget remains positive for specific worst-case scenarios. As example, one scenario simulated a single axis spin at 3.6 deg s^{-1} about a body axis orthogonal to the Sun vector such that only two panels are exposed to the Sun on the same time. Nevertheless, the engineering model could demonstrate to be capable of providing about $700 - 1000$ mW extra power[3] additional to the nominal power consumption of the bus. As these values naturally include all uncertain efficiency parameters including PPT, power path, batteries, converters etc., they allow a robust determination of adequate safety margins in the power budget calculation. Similar tests have been later conducted in orbit as further described in chapter 5.1.2.

3.5 Summary

This chapter addressed relevant aspects regarding the motivation, design, implementation, and test of the flexible and redundant electrical power system employed on UWE-3. Specific challenges connected to electrical power systems of miniature spacecrafts have been discussed and the current state-of-the-art has been presented in terms of a representative selection of available power systems for pico- and nano-satellites. The fundamental concepts and specific implementation aspects of the UWE-3 electrical power system have been elaborated in detail. Finally, various verification and performance test setups and results have been discussed.

Experiences and performance measurements of several experiments conducted in the context of satellite commissioning and experimental operation during its first year in orbit are further presented in chapter 5.1.2. Final conclusions regarding design, test, and operation of the electrical power system are consolidated in chapter 6.2.

[3] orbit average, exact value depends on type of regulated bus and the battery charge state

4

Robust and Efficient Core Module

Control and data management systems play a central role in any spacecraft as they control all other devices and further collect, manage and distribute the acquired data among the spacecraft and to the ground segment. Besides all tasks related to platform control and surveillance, the data management system takes care of payload monitoring and control. In particular its tasks include housekeeping and supervision, telemetry and telecommanding, onboard time management, attitude and orbit determination and control, as well as onboard autonomy. The individual functions might be implemented on a single dependable onboard computer system or distributed on additional dedicated payload computers. (Montenegro, 2009)

Similar to terrestrial embedded computers, spacecraft onboard computers are typically composed of blocks implementing a data processing unit, data storage and data communication in terms of input/output devices. However, as outlined by Montenegro (2009), space borne computer systems have to comply with specific requirements in order to provide dependability despite typical threats inherent to the space environment. All components of a spacecraft are exposed to extreme mechanical and thermal stress due to strong vibrations during launch and high temperature variations in the absence of any atmosphere during regular operations. The most critical challenges for onboard computer systems are imposed by typical limited resources such as limited space, energy and mass as well as potential hazards due to radiation effects in analog and digital electronics.

For mentioned reasons traditional onboard computer architectures employ expensive radiation tolerant or radiation hardened components to ensure reliability of the system. This approach is not always feasible due to cost constraints or performance requirements. Increased complexity of modern space missions demands adequate onboard computers providing energy efficient and performant processing capabilities. According to Czajkowski and McCartha (2003) the performance evolution of commercial and hardened processor

technologies shows that hardened technology typically lags 2-3 generations behind commercial devices. Effectively, standard components can provide an order of magnitude enhanced performance in terms of processing power, energy efficiency and integration density compared to qualified radiation immune components (Behr et al., 2003).

In the last decade, the trend towards commercial technology has become significant for small satellite missions and is particularly an enabling factor for the pico- and nano-satellite class. However, as processing power, energy efficiency and radiation tolerance can usually not be maximized simultaneously by component selection only (Czajkowski and McCartha, 2003), fault tolerance has to be achieved on system design level instead. In the past, various small satellite missions could demonstrate the power of commercial processing technologies such as the ARGOS project (Lovellette et al., 2002), the BIRD mission (Brieß et al., 2005) or the X-Sat micro satellite launched in 2011. However, still little progress has been made for the utilization of commercial technologies in mission critical areas (McLoughlin and Bretschneider, 2010), especially in the context of miniature satellites.

This chapter describes design, implementation, test-results and in-orbit performance of a robust ultra-low power onboard data handling core module developed for UWE-3. In order to provide a better understanding of the design drivers and the measures taken to achieve robustness in the commercial technology design, first, an introduction about space radiation, effects and mitigation techniques is given, followed by a more detailed overview of available onboard computer architectures for miniature satellites.

4.1 Space Radiation Effects and Mitigation

Potential threats for space systems due to ionizing radiation have been discussed since the discovery of the Earth's radiation belts in 1958. Since the beginning of space age spacecraft engineers have been faced with the challenge of designing radiation tolerant hard- and software. Nevertheless, in the last decades about 1-2 satellites per year suffered total or partial mission loss induced by space weather effects. (National Research Council, 2000)

The topic has recently become popular again when the Operation of the Mars rover Curiosity was affected due to a glitch in the flash memory of its active board computer on 28th of February 2013. In this case the main computer could be swapped to a redundant onboard computer (B-side) to resume operation and to allow for further investigation of the problem in order to restore the A-side computer again as a viable backup (Webster, 2013). Even though the corresponding hardware of Curiosity is radiation tolerant it is likely that

the root cause for the failure is related to radiation effects (Moskowitz, 2013).

The typical space environment for Earth orbiting satellites mainly comprises three sources of ionizing radiation: galactic, solar and terrestrial. A good overview about the Earth's radiation environment is given by National Research Council (2000) and Edmonds et al. (2000) and is outlined in the following section.

4.1.1 Space Environment for Earth Orbiting Satellites

Galactic Cosmic Rays (GCR) originate from the outside of the solar system and consist mainly of a relative low but continuous flux of energetic protons and a few heavy ions. Even though the protons make up the majority in the GCR composition, the heavy ions constitute the most important source of GCR induced radiation effects on spacecrafts. Further, secondary neutrons might be generated due to collisions of high energetic particles with matter inside the spacecraft itself.

The second source of ionizing radiation is given by energetic particles emitted by the sun during Solar Particle Events (SPEs) such as Solar Flares or Coronal Mass Ejections. The probability of these events is not constant but modulates with the eleven year solar cycle. Unlike GCR protons, solar event protons contribute significantly to radiation effects on spacecrafts due to their relative abundance compared to heavy ions among SPE particles.

The most important radiation source for Earth orbiting satellites are trapped particles in the geomagnetic field. Particles captured by the Earth's magnetosphere travel around the planet while bouncing between the geomagnetic poles. They form the so-called inner and outer radiation belts whose impacts are most significant between 1.000 and 32.000 km altitude.

However, most of the interplanetary radiation is shielded by the geomagnetic field so that the amount of radiation received by a spacecraft significantly depends on its orbit. The Earth's magnetic field can be approximated as a dipole[1] with its main axis slightly tilted with respect to the planetary rotation axis and its origin displaced by more then 500 km from the Earth's geometric center. Hence, besides the magnetic poles, the radiation belts come closest to Earth over the South Atlantic, a region which is referred to as the South Atlantic Anomaly (SAA).

Ionizing radiation can effectively not be avoided by Earth orbiting satellites, especially for higher inclinations. This fact, together with the continuously decreasing feature geometry of integrated circuit designs, their decreasing operating voltages and their ever increasing clock speeds, render modern semiconductor components extremely sensitive

[1] good approximation for altitudes below 4-5 Earth radii (Petersen, 2011)

to radiation effects (Santarini, 2005). Forcing traditional spacecraft designers to trade-off reliability versus performance by utilizing radiation-hardened parts, this is not an option for educational small satellite projects due to limited component accessibility at typically high prices and further due to extreme size, mass and power limitations imposed by the nature of miniature satellites. For this reason other mitigation techniques such as error detection and correction have to be employed in order to achieve robust designs.

In order to understand the concepts of typical mitigation techniques, the following section outlines the basic principles of radiation effects in semiconductors and bases on detailed information provided by Edmonds et al. (2000), Maurer et al. (2008), and Micheloni et al. (2010).

4.1.2 Radiation Effects in Semiconductors

When energetic particles penetrate matter such as semiconductors, they deposit energy in the target material. The causal interaction can be either ionizing, causing the creation of electron-hole pairs, or non-ionizing, such as nuclear interactions resulting in atomic lattice destruction which is usually referred to as Displacement Damage (DD). For CMOS devices the most significant effects are related to ionization.

Ionizing radiation can be characterized by its Linear Energy Transfer (LET), which describes the ionizing energy per travelled distance of the impinging particle in the target material. It depends on the particle type and its kinetic energy. The product of the LET, normalized by the density of the target material, with the radiating particle fluence provides the amount of collected ionizing energy per unit mass, which is referred to as Total Ionizing Dose (TID).

The expected annual dose absorbed by semiconductor components inside a satellite like UWE-3 is in the order of 10 kRad assuming an aluminium shield of 1 mm which corresponds to the shield thickness of the UWE-3 side panels. Figure 4.1 shows the absorbed ionizing dose in a silicon probe surrounded by an aluminium sphere with varying shield thickness. The corresponding simulation has been performed with SPENVIS[2] for a 700 km Sun-Synchronous LEO during solar Maximum.

Radiation can cause immediate or cumulative effects on semiconductors or insulators. Cumulative effects are mostly related to TID or DD resulting in gradual changes of the circuit functionality. When a single ionization event causes abrupt changes or transient effects one speaks of Single Event Effects (SEEs).

[2] Space Environment, Effects, and Education System (www.spenvis.oma.be)

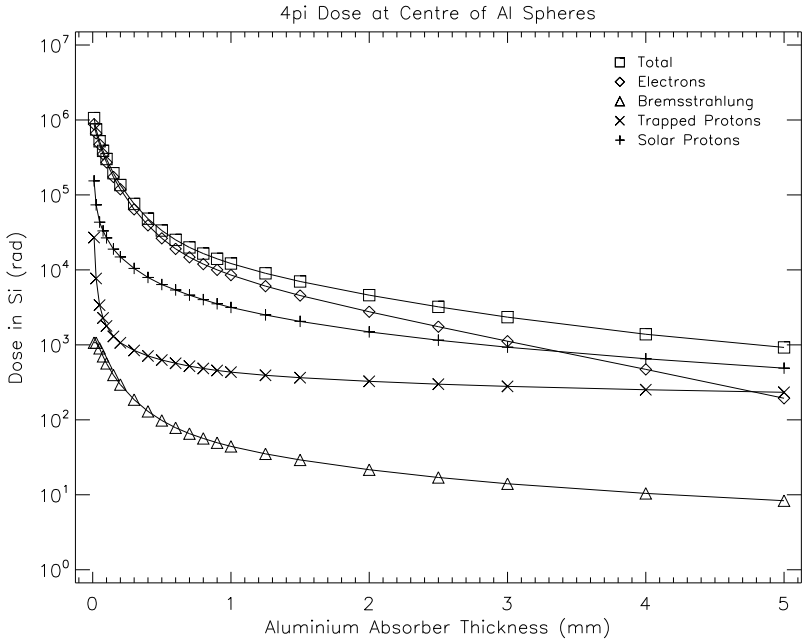


Figure 4.1: Estimated annual Total Ionizing Dose absorbed by a shielded silicon probe in the expected UWE-3 orbit as simulated with SPENVIS.

Total Ionizing Dose Effects

Depending on the LET and the electric field strength present in the target, a large fraction of generated electron-hole pairs undergo immediate recombination. The remaining fraction of carriers, the so called charge yield, is mainly responsible for cumulative malfunctions due to charge trapping and defect generation in dielectric layers. While generated free electrons quickly drift away driven by the local electric field, the less mobile holes might be trapped by oxide layers, thus slowly building up charges which in turn affect the functionality of the semiconductor circuit. However, over the course of time trapped charges can be neutralized again due to annealing effects, e.g. promoted by thermal excitation.

Induced charge buildup can affect the functionality of MOS transistors due to charges trapped in the gate oxide, thus shifting the threshold voltage towards lower gate voltages as the additional potential has to be compensated. In complex circuits, this can result in increased leakage currents, reduced driving strengths, degraded timing margins and even state locks such that a transistor circuit can not be turned off anymore. Unhardened commercial components withstand doses up to several kRad. Radiation tolerant devices can sustain doses in the range of 20 to 100 kRad while hardened components might fail only after several hundred kRad.

Digital bipolar transistor circuits are in general more robust regarding TID but not completely immune when they employ oxide isolation techniques. In contrast, linear

circuits exposed to more than several tens of kRad might suffer significantly from changed input bias currents, offsets, and drifts as well as voltage offsets and drifts due to transistor degradations. Leakage currents of linear circuits can further increase significantly with TID.

Single Event Effects

When the energy deposited to a sensitive circuit by a single ionizing particle exceeds a device specific threshold, an immediate response can be triggered. The so-called Single Event Effect can be either destructive, resulting in permanent physical damage, or non-destructive, in case the effect only causes loss of data or control. In contrast to TID effects, SEE are not cumulative.

The number of observed SEEs in a device exposed to ionizing radiation depends on the LET of the penetrating particles and the sensitivity of the device to respond to charge depositions. The latter can be expressed by the device specific cross section which describes the probability of an event as response to a penetrating particle. The cross section can be expressed by $\sigma_{SEE} = NF^{-1}$. Here, N describes the number of events observed in a device exposed to a particle fluence F with a specific LET. The cross section effectively depends on the LET, typically fading in with increasing LET after a threshold L_0 is exceeded and converging towards a saturation cross section σ_s. The threshold L_0 is related to the minimum (or critical) charge necessary to cause an effect in a circuit node. The relation of the cross section for a specific SEE type and the LET is usually determined experimentally by fitting observed event numbers for various LETs to a Weibull function. Combining LET spectra estimated for a specific spacecraft trajectory with the determined cross section allows rough estimations of SEE rates in orbit.

However, various types of SEEs in CMOS circuits are possible. A potentially destructive effect is the Single Event Latchup (SEL). A latchup is generated by the activation of parasitic bipolar junction transistors due to small currents injected into a sensitive region, resulting in a self-sustained shortcut between the supply pins which in most cases remains until the circuit is made potential free. When the supply current is not limited a latchup might end up in permanent damages which is the case for Single Event Burnouts (SEBs) in power MOSFETs. Other destructive effects can occur due to dielectric breakdowns in gate oxides caused by sudden charge buildups which is referred to as Single Event Gate Ruptures (SEGRs).

The most prominent non-destructive effect is the Single Event Upset (SEU) which describes the corruption of information due to a radiation induced logical state change of

a memory cell or a flip flop. Decreasing feature sizes of sensitive circuits increases the vulnerability to SEUs so that even Multiple Bit Upsets (MBUs) became recently more significant. However, no physical damage is caused by upsets such that these effects might be corrected by reprogramming the cell. Observed SEU rates in Low Earth Orbits for COTS components are in the order of 10^{-5} to $10^{-6}\,\mathrm{bit}^{-1}\mathrm{day}^{-1}$ (Underwood and Oldfield, 1999).

With increasing clock speeds of modern technologies also Single Event Transients (SETs) became recently more significant. SETs are transient signal fluctuations caused by induced currents in semiconductor circuits. These transients are harmless unless the false signal is propagating through the circuit and eventually captured by a memory element. Higher clock speeds significantly increase the probability of capturing a transient signal. SETs might further affect the function of linear regulators and DC/DC converters.

When SEUs or SETs occur in complex devices like flash memory control logics or microcontrollers they might trigger undesired behavior such as illegal instruction executions. These so called Single Event Functional Interrupts (SEFIs) can result in loss of control or even loss of data in case of undesired memory write access.

4.1.3 Radiation Effects in Flash Memories and Floating Gates

With rising popularity of non-volatile flash memories for personal computers this technology becomes also more attractive for space industry, especially for the utilization in solid state recorders. Flash memories are indeed very beneficial as they provide high capacity non-volatile data storage at high densities. The technology is further shock resistant, power-economic, and can be procured at reasonable prices. Thus, it contributes only insignificantly to power, mass and volume requirements. (Caramia et al., 2009)

Especially small satellite implementations such as the BIRD satellite use flash based data storage for program memory of processors and microcontrollers as well as for mass storage (Brieß et al., 2002). However, the benefits come at a price since the technology is also quite sensitive to Total Ionizing Dose and Single Event Effects as described by Micheloni et al. (2010) and Gerardin et al. (2013).

Flash memory devices are complex circuits, such that numerous potential failure modes are possible. For a long time, the periphery circuits build around the floating gate array were considered to play the most significant role in radiation induced failures of flash memories. As an example, the charge pump which is used to generate the programming voltage was found to degrade significantly after 10 to 30 kRad such that floating gate cells can not be erased reliably any more. SEEs have been observed in the periphery as upsets

in page buffer latches or functional interrupts in control logics, causing errors especially during read or write operations. (Micheloni et al., 2010)

Recently, the radiation sensitivity of floating gate cells itself has gained more attention. Especially the advancements in memory density brought along an increased vulnerability of floating gates to both, TID and SEEs. These errors usually affect the charge state of the floating gate directly, thus changing the information stored in the cell permanently until it is reprogrammed.

A floating gate cell can be described as a transistor with an additional isolated gate underneath the control gate (see figure 4.2). Any electrons stored in the so-called floating gate affect the threshold voltage V_{th} of the transistor. The actual V_{th} constitutes the information stored in the cell, determining whether a cell is read as logical one or zero when a defined read-out potential which adds to the floating gate potential is applied to the control gate. The application of high negative voltages between control gate and source terminal erases the cell by moving the charge off the floating gate through the oxide. For programming, a high source-drain current enables energetic electrons to pass the oxide layer and remain trapped in the floating gate. The charge state of the floating gate usually remains stable for several years and might only change slowly due to temperature dependent leakage effects. (Forstner, 2008)

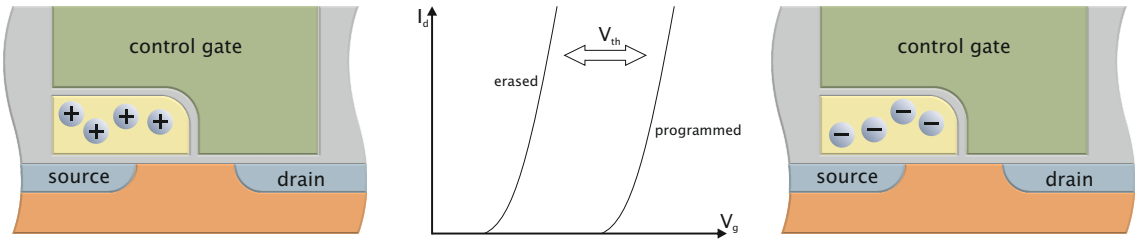


Figure 4.2: Simplified schematic of a floating gate cell as used in MSP430 microcontrollers (based on Forstner, 2008). The transistors threshold voltage V_{th} is decreased when the cell is erased (left) and rises when the floating gate is programmed (right).

Recent studies on modern flash devices revealed that ionizing radiation causes progressive discharge of the floating gates with accumulating ionizing dose. Charges generated in the oxide layers surrounding the floating gates progressively affect the charge state of the floating gate, thus altering the threshold voltage V_{th} towards a common mean voltage. The effect has been observed to become significant after 55 kRad TID (Micheloni et al., 2010). The dose threshold changes from device to device. Some devices show upsets already after 25 kRad TID (Gerardin et al., 2013).

Single Event Effects in floating gate cells have been observed as sudden threshold voltage drops due to prompt discharge of individual floating gates hit by an impinging

ion. The V_{th} shift linearly depends on the LET and becomes more significant for smaller scale cell structures, resulting in continuously decreasing threshold LETs of newer device generations. Depending on the angle of incidence the ionization strike can even affect a row of adjacent cells and corrupt the information stored. (Micheloni et al., 2010)

Effective cross sections of modern flash memories are still some orders of magnitude smaller compared to typical volatile COTS memories (Gerardin et al., 2013). Depending on technology and solar activity the SEU rate of modern flash memories in LEO can vary between $10^{-7}\,\text{bit}^{-1}\text{day}^{-1}$ (Bagatin et al., 2013b) to $10^{-11}\,\text{bit}^{-1}\text{day}^{-1}$ (Bagatin et al., 2013a). However, continuously decreasing threshold LETs of modern device technologies makes radiation induced data corruption in flash memories more and more significant, not only for harsh environments but also for terrestrial applications (Micheloni et al., 2010).

4.1.4 Mitigation Techniques

Ionizing radiation can affect the operation of spacecraft systems significantly, ranging from temporary disturbances like data corruption to fatal failures resulting in total mission loss. Modern device technologies can be quite sensitive to radiation effects due to feature miniaturization and power optimized semiconductor designs. The utilization of radiation-hardened devices can increase robustness but is often no option due to cost, availability, efficiency or capability. For this reason, the utilization of Commercial Off-The-Shelf (COTS) technologies in space has been under investigation for more than a decade such as reported by Lovellette et al. (2002) who describe first direct comparison of a radiation hardened processor with a similar COTS processor onboard the ARGOS satellite. Recent activities related to small and cost-efficient spacecraft underline the importance of mitigation techniques apart from hardened technologies in order to realize miniaturized systems which are powerful, energy-efficient and robust at the same time.

However, special care has to be taken in both, hardware and software design, in order to mitigate severe effects despite the sensitivity of standard components. In general, mitigation can be realized by protection, conservative design, redundancy and recovery (Tribble, 2003). The most important mitigation techniques are outlined in the following, based on a more comprehensive overview by Maurer et al. (2008).

Hardware Mitigation Techniques

Selective shielding of dose sensitive components with high electron number materials like tantalum or tungsten can effectively reduce ionizing doses induced by electron and low-energy proton radiation. However, shielding is generally not effective regarding SEEs and

might even reduce robustness against high-energy radiation due to generation of secondary particles caused by interactions with the shielding material.

Another approach for minimizing radiation effects in some devices can be to simply minimize the target by limiting their operation during times or regions exposing excessive radiation doses (e.g. SAA passage). Partially powering down unnecessary circuits can effectively protect them from TID effects depending on electrical potentials or destructive SEE effects such as latchups.

Besides relying on radiation-hardened technologies, lifetime of sensitive components might also be increased by de-rating. The technique refers to a conservative design and component selection which assures that relevant specification parameters significantly exceed the circuit operation requirements. For example, the component selection might already take into account future increased power consumption or changing bias currents caused by TID effects.

As critical effects due to SETs are closely related to the operating frequency, the design of digital circuits operating at moderate clock frequencies increases the systems tolerance against transients.

Robustness against latchups is usually achieved by a combination of damage protection and recovery mechanisms. In order to prevent high currents flowing during a latchup condition to cause permanent damages in the device, the supply current of the relevant circuit has to be limited. This can be achieved by a series resistor in the supply path of low power devices or a more sophisticated circuit breaker design in case of high power applications. However, a controlled potential free power cycle has to be applied on the latched device in order to suspend the latchup condition.

One of the most important mitigation techniques related to SEUs, SETs or SEFIs in microprocessors are watchdog timers. These are independent timer circuits which, when not being triggered for a specified timeout period, perform a reset on the unresponsive device.

Whenever extra space and power consumption are not a limiting factor, the introduction of hardware redundancy can mitigate severe failures on system level. In the easiest case redundancy can be applied by simply duplicating a component in a parallel or serial connection which is effective for diodes or switches, for example.

Logical circuits can be triplicated whereas a robust voting unit is used to determine the corrected output, a mature technique which is usually referred to as Triple Modular Redundancy (TMR) and goes back to Lyons and Vanderkulk (1962). In more advanced configurations a set of multiple microprocessors running in lockstep have been realized such as described by Angilly (2004). However, special care has to be taken to minimize

single point of failures in the voting circuits itself. The triplication of the processing unit significantly increases power consumption and imposes performance degradation due to the complexity of re-synchronization in case an error was detected (Czajkowski and McCartha, 2003).

Software Mitigation Techniques

Besides mitigation on hardware level many SEU or SET induced memory corruptions can be identified and corrected in software. Software based mitigation techniques do not require any custom or redundant hardware components and are therefore adaptable and cost-efficient. However, they might introduce memory overhead and performance degradation due to software and processing redundancies.

In the easiest case software protection mechanisms can be implemented by simple state verification where the contents of critical control registers are monitored and corrected if necessary. More sophisticated software based memory protection techniques rely on Error Detection And Correction (EDAC) codes which can effectively enhance the availability of COTS in space applications. In software implemented EDAC routines make use of redundancies in order to detect and correct corrupted memory blocks. Commonly used coding schemes are simple parity checks, Cyclic Redundancy Checks (CRCs), Hamming codes or Reed-Solomon codes. The checks are typically executed periodically (scrubbing) in order to avoid accumulation of errors (Shirvani et al., 2000).

An analog approach to TMR on hardware level is time redundancy on software level. Instead of duplicating a processing unit multiple times redundancy can be carried out in time by performing redundant calculations on a single processor only. So-called source-to-source compilers can be used to generate hardened code automatically by adding redundant instructions to an implementation according to some transformation rules (Oh, 2001). Nevertheless, additional protection mechanisms are required to assure robust operation and the code transformation typically adds significant overhead in memory requirements and execution time (Azambuja et al., 2011).

4.2 Onboard Computers for Small Satellites

Various hardware and software mitigation techniques which can enhance robustness of space borne electronics on system design level have been presented. The increasing complexity of forthcoming satellite missions together with the growing demand for smaller and more cost-efficient satellite systems for commercial applications emphasize the importance

of modern off-the-shelf components for space applications as they promise increased system performance at lower mass, power consumption and cost. Especially small scale satellite missions can benefit significantly from these technologies as they often demand high computational performance at small power budgets and limited financial resources.

A good example for the successful utilization of commercial standard components in order to increase efficiency in many aspects is given by the X-SAT project which had been launched in 2011 (Kwoh et al., 2012). Carrying a multispectral camera as a primary payload, one of the experimental satellite's main objectives was to develop a low cost micro satellite bus for near real-time remote sensing applications. McLoughlin and Bretschneider (2010) describe the design of a COTS based parallel computer architecture which has been designed as a capable Parallel Processing Unit (PPU) for X-Sat to be used for processing large amounts of image data captured onboard the spacecraft.

The X-Sat PPU architecture combines 20 low power COTS processors operating in parallel to resemble a powerful embedded Beowulf cluster. Two antifuse FPGAs act as interconnecting backbone which controls the data flow between the individual nodes. A set of triple redundant serial flash memory devices connected to each FPGA stores the configuration data and program code to be loaded to the attached processing nodes on activation. Separate power switches and failure protection circuits allow to power cycle the nodes independently in control of the FPGAs or an independent power fault monitor. Thus, the system provides high computational performance at relatively low power consumption while still providing an acceptable level of reliability in terms of increased redundancy and graceful degradation.

As McLoughlin and Bretschneider (2010) report the performance requirements defined for the X-Sat PPU would not have been feasible relying on radiation hardened technology only. This paradigm becomes even more relevant when looking at typical subminiature satellite projects in the nano and especially pico class where the main design drivers are not seldomly dominated by energy and cost efficiency.

4.2.1 Commercial Onboard Computers for Pico-Satellites

In the last years a number of miniature onboard computers for pico- and nano-satellites became available on the market. Many of the available systems have been developed in the context of former university projects or are derived from such developments. They cover a relative wide range of processing capabilities and power requirements such that not all systems might be suitable for all missions. Some quite powerful onboard computers like the *Q6* (Xiphos Technologies, 2013), the *OBC lite*™ (AAC Microtec, 2012) or the

CORTEX 160 (Andrews Space, 2013) might be good candidates for nano-satellite missions, but exceed the power budget of typical pico-satellite architectures. The most prominent commercial devices suitable for pico-satellites are depicted in the following sections.

CubeSat Kit™ FM430 Flight Module

One of the first commercial onboard computers for pico- and nano-satellites is the *CubeSat Kit™ FM430 Flight Module* (Pumpkin, Inc., 2008) which has been available on the market for more than 6 years and has recently been replaced by the *CubeSat Kit™ FM430 Motherboard*. The *FM430* has been used in different hardware revisions in various missions such as on the Delfi-C^3 nano-satellite (Brouwer et al., 2008) or the pico-satellite ITUpSAT1 (Kurtulus et al., 2007) which have been launched in 2008 and 2009 respectively. The system is designed around a single low power 16-bit MSP430 RISC microcontroller with 60 kB Flash memory and 10 kB RAM and operates at 7.4 MHz maximum. It provides most common digital interfaces such as UART, SPI, and I^2C together with several general purpose I/O lines. An SD card socket provides up to 2 GB optional mass storage.

The PCB with typical CubeSat form factor weights about 74 g. The plain hardware design comprises an onboard low-dropout regulator as power supply combined with undervoltage and overvoltage protection as well as overcurrent protection circuits for individual components. Depending on its configuration the device consumes about $10-100$ mW which can be comfortably accommodated within a typical power budget of both, pico- and nano-satellites.

NanoMind A712C

A similar architecture compared to the *FM430* but equipped with a more capable onboard processor is the *NanoMind A712C* (GOMSpace, 2014a). The straight-forward design is centered on a single 32-bit ARM7 RISC CPU operating at $8-40$ MHz. It comes with 4 MB program flash memory and 2 MB RAM which makes it suitable for more advanced conventional operating systems. The onboard 4 MB Flash memory for data storage can be extended with a MicroSD card providing up to 2 GB extra mass storage. Besides UART and I^2C the board provides a CAN interface for subsystem communication.

The mechanical design follows the *CubeSat Kit™* subsystem interface definition and weights about 55 g. With a nominal power consumption of $120-300$ mW the onboard computer could still be accommodated in the power budget of a typical pico-satellite. The *NanoMind* has been used in several missions. Among others it has been used in the STRaND-1 nano-satellite which has been launched in first quarter of 2013 (Bridges

et al., 2013). Recently, the *NanoMind* has been successfully operated in the nano-satellite GomX-1 (Alminde et al., 2012) which has been launched together with UWE-3 in late 2013.

Cube Computer

The *Cube Computer* (Stellenbosch University ESL, 2014) is comparable in architecture and processing capabilities but provides increased fault tolerance. The design bases on a single 32-bit ARM Cortex-M3 which operates at $4-48$ MHz and provides 4 MB program flash memory. With its standard CubeSat form factor, a total mass of $50-70$ g and a specified total power consumption of less than 200 mW the system can be used as an capable onboard computer for typical pico- and nano-satellite missions.

As described by Botma et al. (2012) the *Cube Computer* achieves memory SEU tolerance by a flow-through error detection and correction mechanism implemented in an FPGA. Further, an anti-latchup circuit monitors the current consumption of the SRAM modules which can be isolated or power cycled by the processing unit in case of a malfunction. An additional external watchdog adds reliability by automatically performing a power cycle in case of latchups in the processor itself. The *Cube Computer* has been developed in the context of the ZACube-2 nano-satellite and has no flight experience yet.

Intrepid System Board

Increased processing capabilities at reasonable power consumption is provided by the *Intrepid System Board* (Tyvak, 2012) which is available on the market since early 2012. A single ARM926-based Atmel AT91SAM9G20 32-bit processor is operated at 400 MHz with 128 MB SDRAM and 512 MB program flash memory. An extra 32 MB serial flash memory and an external MicroSD card can be used for data storage. The embedded Linux operating system has access to various digital interfaces such as UART and I^2C as well as a set of general purpose IO lines for optional daughter boards and inter-board communication. The total power consumption of the *Intrepid System Board* varies between $200-300$ mW.

The hardware architecture combines a processing unit together with basic power regulation circuits on a lightweight 55 g PCB with typical CubeSat form factor. The design further includes several fault tolerance mechanisms such as a latchup protection for memory and processor, an external hardware watchdog and a separate programmable hard reboot timer. The *Intrepid System Board* has been used on a CubeSat mission launched in November 2013. It is further planned to be employed as high power processing unit

for onboard science data processing on the INSPIRE nano-satellite mission (Klesh et al., 2013).

ISIS On Board Computer

Recently, the *ISIS On Board Computer* (ISIS, 2014) became available on the market. With its single 400 MHz ARM9 processor the high performance processing unit is comparable with the *Intrepid* architecture. The *ISIS* unit is equipped with 32 MB RAM and 1 MB program flash memory. Further, 256 kB additional FRAM can be used as non-volatile data storage while two redundant SD card sockets provide up to 4 GB optional mass storage.

Besides several general purpose IO lines the *ISIS On Board Computer* provides most common digital interfaces such as UART, SPI, and I^2C. An external watchdog and power controller contribute to the reliability of the design. The *CubeSat Kit*™ compatible onboard computer has a total mass of 96 g when equipped with an additional daughter board providing additional interfaces. With its 400 mW average power consumption the design might already reach the limits of practicability in the power budget of many pico-satellites. The technology is based on the design of the payload data processing unit for the Triton-1 nano-satellite which has been launched together with UWE-3 in late 2013.

Mission Interface Computer

With the *Mission Interface Computer* (Clyde Space, 2012c) (Clark et al., 2012) a hybrid solution regarding the trade-off between power consumption and processing capabilities of miniature onboard computers became available on the pico- and nano-satellite market. The *Mission Interface Computer* combines a low power 16-bit RISC MSP430 operating at 20 MHz with a more capable Actel FPGA implementing an additional 32-bit RISC ARM Cortex M1 softcore which operates as initial primary processor at $20-40$ MHz. The standard configuration of the primary processor comes with 8 MB EDAC protected RAM, 128 kB ROM and 2 GB mass storage. The secondary processor provides 16 kB RAM and 8 MB configuration storage. Both processors have access to several digital communication buses such as I^2C and UART or SPI.

As both processor units have control over the subsystem interfaces one can act as the main onboard computer while the other unit might provide assistance in terms of background data processing or mutual reconfiguration. The roles can be swapped in case of a malfunction which provides increased robustness in terms of asymmetric redundancy. The *Mission Interface Computer* has originally been developed for the UKube-1 nano-satellite (Greenland, 2012) which has been launched in mid 2014. However, the architecture's

increased power consumption of $500 - 1250\,\text{mW}$ limits its usability for typical pico-satellite platforms.

4.2.2 Redundant Onboard Computers

Various commercial miniature onboard computers suitable for a variety of mission requirements became available in the last years. All devices presented rely on COTS technology to increase efficiency for a viable application on small satellite platforms. Some of them could already demonstrate successful operation in orbit, others are still pending in-situ verification. In order to increase dependability, several hardware architectures employ extra latchup protection circuits and external watchdog units.

However, beside power and communication, the onboard computer is one of the most crucial subsystems of a satellite bus and should therefore have redundancy in order to provide a reasonable level of reliability (Shirasaka and Nakasuka, 2011). This is not a trivial task when it comes to miniature satellite platforms. In fact, one of the main challenges for small satellite engineering concerns the careful design of redundancies in order to cope with the limited resources available (Burlacu and Lorenz, 2010).

The majority of onboard computers presented provide only little in-system redundancy. Hence, duplication on system level would be required in order to minimize single point of failures on the satellite itself. Some nano-satellite architectures such as Delfi-Next (Bouwmeester et al., 2010) might allow to duplicate a low power onboard computer within its budgets. On the other hand most onboard computers presented would already use up a significant amount of the power, mass and space available on a typical pico-satellite. Thus, redundancy, replication or diversity on system level would not be feasible on miniature platforms.

Nevertheless, a few developments of redundant onboard computers for pico-satellites have been realized. Providing a certain level of redundancy on sub-system level, these designs achieve to minimize the impact on power, mass and space contribution while avoiding single point of failures on critical components.

Baumann et al. (2009) describe the fault-tolerant design approach for the pico-satellite BEESAT-1 which has been successfully launched in late 2009. The satellite's onboard computer hosts two independent processing units on a single subsystem PCB (see figure 4.3, left). Each unit comprises a 16/32-bit ARM7 core with 2 MB SRAM and 20 MB flash memory. Additional current limiters and watchdog controlled circuit breakers implement latchup protection. A redundant pair of CAN buses connects both units with the subsystems such that each unit is capable of controlling the entire satellite platform. The processing

units are operating in a cold-redundant manner. Thus, only one instance is active at a time and can be switched over to the redundant device in case a malfunction is detected. This limits the typical power consumption of the BEESAT onboard computer to about 150 mW.

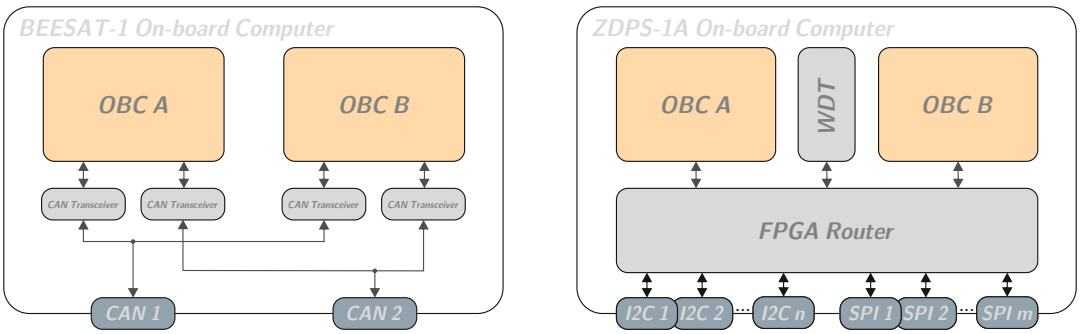


Figure 4.3: Examples for redundant miniature onboard computer architectures of BEESAT-1 (Baumann et al., 2009, left) and ZDPS-1A (Zhang et al., 2012, right).

A different approach has been realized for the ZDPS-1A satellite launched in late 2010 (Yang et al., 2012). The architecture, as described in more detail by Zhang et al. (2012), comprises two redundant processing units which are embedded on a single miniature subsystem board (see figure 4.3, right). As processing units two identical low-power microcontrollers with 2 kB on-chip RAM, 62 kB on-chip program flash memory and 4 MHz clock frequency are employed (Yang et al., 2013). The ZDPS-1A architecture comprises a central FPGA based router which connects the active processing unit with a large set of dedicated data interfaces for each individual subsystem. The processing units are used in a warm-redundant operation scheme which is controlled by the central FPGA. While one unit is always running in stand-by, a separate watchdog circuit connected to the FPGA continuously monitors the active unit in order to initiate an automatic failover to the redundant one in case of a malfunction. Despite the utilization of low-power controllers the onboard computer consumes up to 200 mW which might be mainly caused by the FPGA router.

Both redundant onboard computers presented could demonstrate successful operation in orbit for more than a year. However, their architectures differ significantly. The BEESAT onboard computer effectively uses the CAN interfaces for access arbitration to a compact data bus such that no further electronics is necessary to combine the redundant processing units. The ZDPS-1A relies on a single centralized FPGA for flexible digital signal routing in order to support a wide and in-homogenous data bus. Besides overhead in power consumption this solution might introduce additional single point of failures. On the other side this architecture allows to support a diversity of digital interfaces. This way each different subsystem might be controlled by a dedicated specific data connection whereas

the BEESAT system requires each subsystem to add extra overhead for the implementation of one or two CAN interfaces.

Another difference results from the implementation of the onboard computer's backup schemes. While the BEESAT system relies on a cold-backup strategy, the ZDPS-1A architecture adds a bit more autonomy implementing warm-backup by an automatic fail-over logic. The systems further deviate in processing capabilities. In contrast to the BEESAT system which employs capable ARM cores as a general data handling resource for a variety of applications, the utilization of low power microcontrollers has been found to be sufficient for the basic operation of ZDPS-1A.

However, with $150 - 200\,\mathrm{mW}$ power consumption of both single board designs, their impact on power and mass budgets is acceptable for typical pico-satellite applications.

4.3 Onboard Computer Design for UWE-3

The onboard data handling (OBDH) core module as shown in figure 4.4 plays a central role in the design philosophy of the UWE-3 bus. It can be seen as the fundamental core dedicated to satellite housekeeping operation. It is the only system continuously operating from the very first instant after activation until the satellite ceases operation. Other subsystems might carry their own processing units as required. They might be powered down, power cycled or even re-programmed under the control of the core module in order to ensure proper operation considering the extremely limited power budget on pico-satellites and enhanced threats due to radiation effects. Thus, the design of the core module is optimized with respect to energy efficiency and robustness.

4.3.1 Design Concept

The utilization of radiation-hardened devices can increase robustness but is often no option due to cost, availability, efficiency or capability. Instead, the design strategy for achieving robustness of the UWE-3 satellite bus is mainly failure tolerant design using modern commercial standard components. Relying on Fault-Detection, Fault-Isolation and Recovery (FDIR) techniques, short failure periods are accepted as long as the system protects itself from permanent damages, detects the failure state and recovers in a timely manner.

Due to its central role the design of the UWE-3 onboard computer enhances reliability by implementing two redundant processing units on a single subsystem board. As the core module is optimized for housekeeping and basic operations the design can employ ultra-

Figure 4.4: OBDH Core Module with two redundant microcontroller units measuring only $9x9\,\mathrm{cm}^2$ with an average power consumption of less than 10 mW.

low power microcontrollers as processing units. Besides advances in energy efficiency, the utilization of microcontrollers with task-optimized processing capabilities and clock frequency naturally reduces the target for radiation induced SEUs or SETs as compared to more complex soft- and hardware setups. As microcontrollers usually allow code execution from flash memory the design further avoids the need for bootloading and code execution from RAM which provides enhanced robustness regarding critical SEUs in the code section.

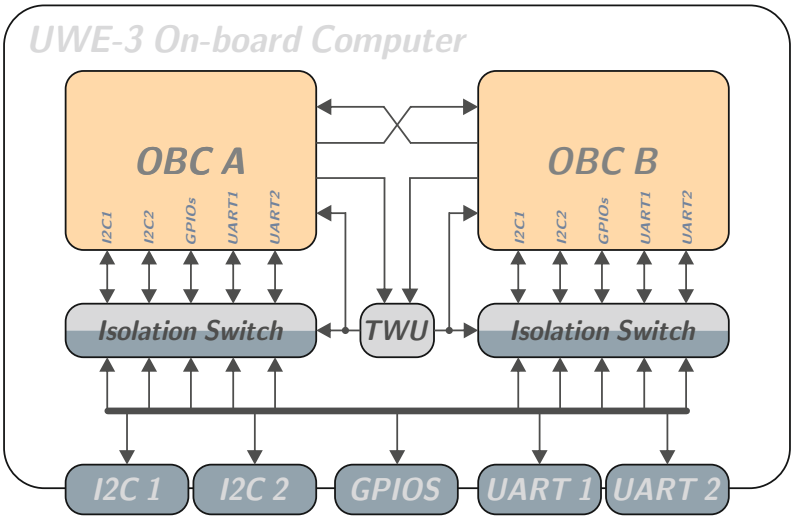


Figure 4.5: Redundancy Design of the UWE-3 Core Module.

As shown in figure 4.5 the core module realizes a warm-backup scheme to be able to

automatically recover from failure conditions by initiating a fail-over to the redundant unit without the need for manual interaction. This procedure is controlled by an independent toggle watchdog unit (TWU) being responsible for proper reset and activation of the redundant hardware. A data cross-connection between the redundant devices further enables mutual aid, up to complete mutual re-configuration. Thus, software based EDAC algorithms on the active unit could identify the fault and re-initialize the inactive device if required.

Two clusters of isolating analog switches implement signal routing and bus arbitration whereas the TWU ensures that the active microcontroller is automatically connected to the bus. At the same time the inactive controller is electrically isolated from the satellite's periphery. This way, a diversity of digital and analog signals can be multiplexed in an simple, energy efficient, and robust way without introducing single point of failures.

The onboard computer supports a compact data interface mainly basing on a redundant set of I^2C buses for general subsystem control (I2C-1 and I2C-2). However, for the control of the UWE-3 bus the design provides additional dedicated communication lines for crucial subsystems such as the redundant communication system (UART-1 and UART-2) and the redundant power path control (two GPIOs). An additional set of general purpose inputs and outputs allows to monitor and control further specific signal lines to be used for example for analog voltage observation or interrupt notification.

In order to ensure autonomous recovery from unresponsive states the design of the core module employs several independent timeout-cascaded watchdog implementations. Besides the TWU which implements the first stage, a redundant power cycling unit (PCU) automatically performs a power cycle on the core module in case the TWU fails to recover the system in time. The third watchdog stage is implemented in software. Monitoring the communication link to the ground segment the software stage might initiate high level recovery procedures such as redundancy selection or soft-reset in order to ensure the satellite's accessibility from ground.

4.3.2 Hardware Implementation

The core module hardware is build around two redundant ultra-low power microcontroller units (MCUs) in a master-slave configuration which is dynamically decided by a separate watchdog controlled arbitration unit, the TWU (see figure 4.6). Beside several cross connections, such as for DMA supported bi-directional high speed communication, the active controller (master) can access the inactive unit (slave) via its Embedded Emulation Module (EEM) using a JTAG interface implementation. This gives full control of the

remote hardware, independent of the current state of its programmed software. Thus, the slave can be accessed, controlled, and even completely re-programmed by the current master MCU for memory scrubbing or secure software updates after launch.

The system further provides a temperature compensated high precision real-time clock for time synchronization between the MCUs, two redundant flash memory based mass storage devices (2×32 Mbit), and several housekeeping sensors for monitoring currents, voltages and temperatures. Two Spy-By-Wire interfaces and a serial debug communication link are routed to the backplane to allow comfortable access to the system for software flashing and in-system debugging via the umbilical line, even when the satellite is completely integrated.

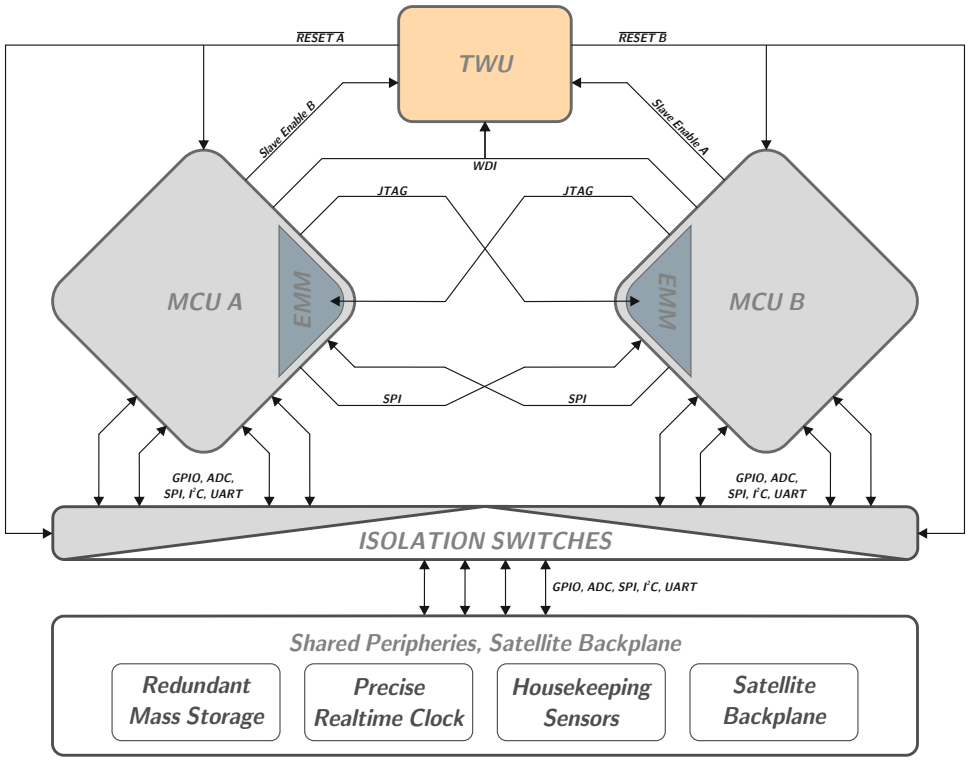


Figure 4.6: Block diagram of the core modules architecture including TWU for dynamic master slave configuration arbitration.

Besides robustness, the OBDH core module is optimized for very low power requirements. In nominal operation, the complete subsystem consumes less than 10 mW (16 MHz). This ensures operability of the housekeeping system at all times, even in severe failure situations, e.g. when the satellite runs into low energy. A redundant power converter, directly supplied from the unregulated power bus, circumvents the main power path in case of a malfunction in the electrical power system. This ensures continuity of proper

satellite control to deal adequately with an emergency situation and recover the system for example by initiating a controlled power cycle of specific subsystems or even of the whole satellite bus (except the core module). The very low power requirement further allows to bridge temporary supply voltage drops for several seconds by using high density backup capacitors. This may be important to compensate for transient current peaks associated with peripheral latchups.

Toggle Watchdog Unit

In normal operation, the current master periodically triggers the so-called toggle watchdog unit (TWU). In case the master fails to serve the watchdog within a specified timeout, i.e. due to MCU hangs, the TWU would perform a reset on both MCUs and subsequently swap the master-slave configuration by asserting the $\overline{RESET}$ signal of the former slave, leaving the former master in reset state. The same logic would control the isolation switches in order to connect analoge and digital signal lines to the satellite bus. However, the slave controller might be enabled afterwards by the master if necessary, e.g. for processing assistance, software checks or re-programming.

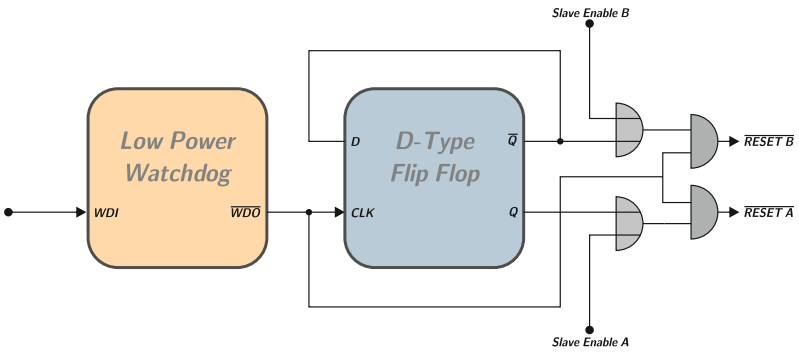


Figure 4.7: Block diagram of the toggle watchdog unit implementation.

The TWU itself is implemented using an external low power watchdog circuit which is connected to the *CLK* input of a D-Type flip flop (see figure 4.7). Feeding back the latch output to its data input, the generated reset impulse is translated to a state toggle of the flip flops opposing output signals. A subsequent combination of OR gates includes the *Slave Enable* inputs which allow the master to additionally wakeup the slave unit. The final AND gates reflect the reset impulse on both outputs to ensure that, besides state toggling, both MCUs are reset before the master is activated. This is especially important if the former slave unit was activated by assertion of the *Slave Enable* signal.

Figure 4.8 illustrates the operation of the TWU. Starting with MCU A as active master,

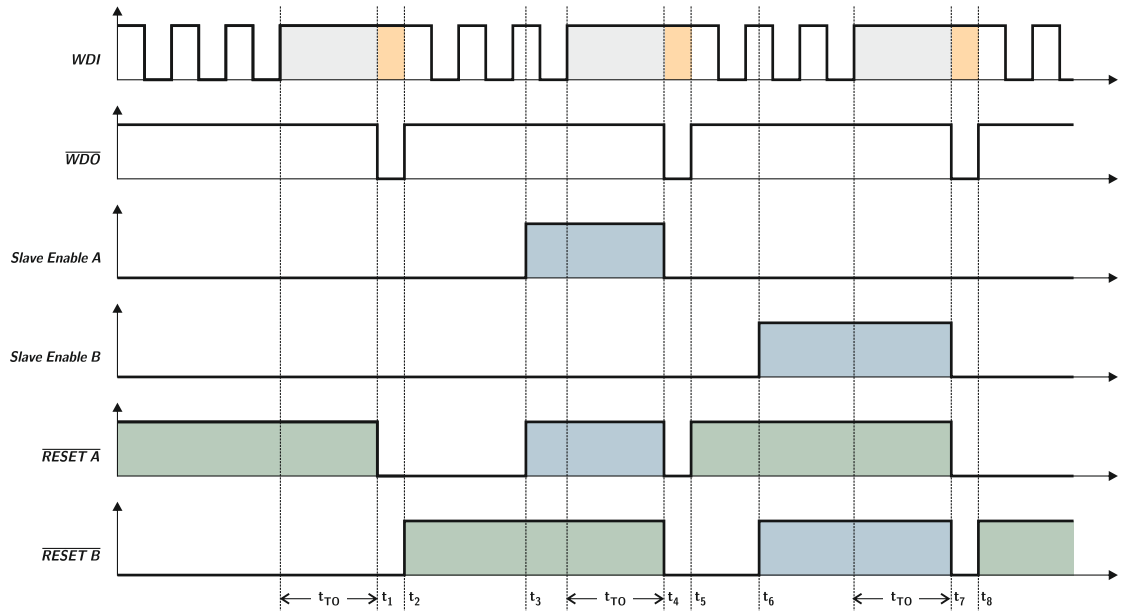


Figure 4.8: Timing diagram of the toggle watchdog unit operation.

at time t_1 the circuit performs a reset due to an elapsed timeout period t_{TO} without activity on the *WDI* signal. The reset pulse generated on $\overline{WDO}$ toggles the state of the latch, resulting in the activation of MCU B as master on the rising edge of $\overline{WDO}$ at time t_2. At time t_3, MCU B asserts the *Slave Enable A* signal. This activates MCU A as slave such that both controllers are operating on the same time, e.g. for mutual assistance. Following a timeout on *WDI* at time t_4 the TWU issues another state toggle, causing both MCUs to perform a reset before MCU A wakes up again as master at time t_5. MCU B remains inactive until the master asserts the *Slave Enable B* signal at time t_6. After the next *WDI* timeout at time t_7 the TWU re-initializes MCU B as master again while leaving MCU A in reset state.

This configuration enables the OBDH core module to monitor itself, recover from failure conditions like system hangs, identify responsible faults in the hardware like SEU induced memory corruptions, and perform recovery mechanisms on software level. However, not all malfunctions can be resolved by pure resets. Especially latch-up conditions or so-called functional interrupts might end up in failures on semiconductor level which usually require a power cycle to recover in case the fault is non-destructive.

Quad-Redundant Power Cycling Unit

In order to autonomously recover from latchup states which could not be recovered by a controlled TWU reset, the core module provides an independent quad-redundant power

cycling unit (PCU) with implicit majority voting arbitrator. The watchdog controlled circuit is able to perform autonomous power cycles of the core module by disconnecting it completely from the backplane using clusters of analog bus isolators. This way, complete voltage isolation of the low power circuits is ensured to recover from non-destructive faults in the semiconductor circuits.

The PCU can be seen as a watchdog operated switch which would perform a controlled power cycle in case its *WDI* signal is not triggered by the master MCU for a specified timeout. As the PCU itself is a critical system, not being monitored by any further instance, its design comprises redundancy without requiring a central arbitration unit to avoid single point of failures. This is achieved by the utilization of four individual watchdog controlled high-side switches in series-parallel configuration (see figure 4.9, left). Thus, the PCU output reflects an implicit majority decision, conducting power when most of the individual switches are closed, and isolating when most of the switches are open. In other words, the circuit at least allows one switch to fail in any mode without affecting the overall PCU operation.

The individual watchdog switches are implemented in a similar way as done for the TWU unit. A single switch is realized using a D-Type flip flop in toggle configuration (see figure 4.9, right). A low power watchdog would swap the state of the flip flop in case its *WDI* signal is not triggered for a specified timeout. The connected high-side switch turns off until the subsequent $\overline{WDO}$ pulse, following another timeout period, would toggle the latch again. An inverter connecting the *WDI* signal to the flip flops pre-set input ensures that a signal change on *WDI* also synchronizes all latches to achieve a defined default-on state and ensures proper bootstrapping of the circuit.

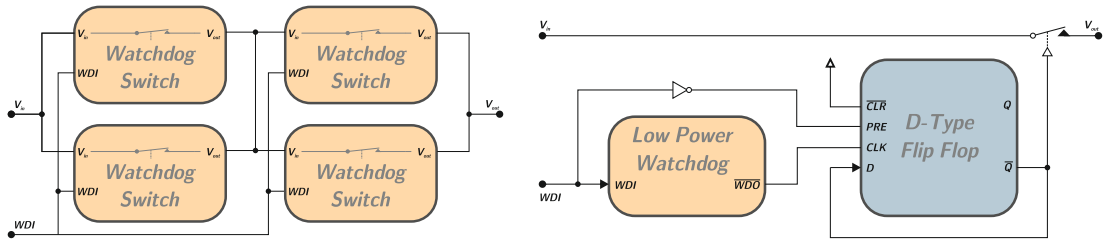


Figure 4.9: Block diagram of the quad-redundant power cycling unit with implicit majority voting (left). Block diagram of a single PCU watchdog switch (right).

The high side switches itself further provide over current protection which is tuned to the expected maximum current consumption of the core module. In case of a severe malfunction caused by a latchup in the core module, the switches would limit the current by dropping the supply voltage, hence protecting the semiconductors from permanent

damages due to burnouts. After a while, the PCU watchdogs would shut down one after another until the core module is completely potential-free. After about one minute the PCU automatically continues operation of the core module again.

For proper recovery from non-destructive latchups it is essential that the corresponding circuit is completely potential free. In the case of the ultra-low power microcontrollers in the present design, this is not a trivial task as the controllers can operate with extremely low current consumption, which implies that the off-resistance in the power path has to be sufficiently high in order to drop the supply voltage completely.

Standard CMOS devices typically provide electrostatic discharge protection in terms of clamping diodes connecting to the supply rails on each input. Powering off the device by disconnecting *VDD* without isolating its signal inputs from parts of the circuit which are not powered down might result in undesired power supply paths to the device as can be seen in figure 4.10.

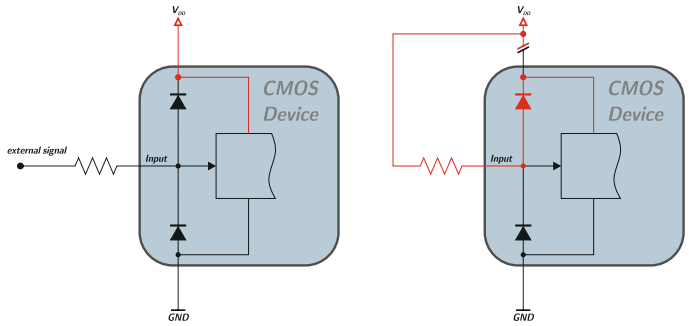


Figure 4.10: CMOS device with clamping diodes connecting to the supply rails can provide undesired power supply paths in partial power down operation (right).

Due to the minimal current drain of the utilized ultra-low power microcontrollers, the parasitic power path would be sufficient to prevent *VDD* from dropping sufficiently as it would be sustained by the input signal via the protection diode. In the design of the core module the isolator switches shown in figure 4.5 and 4.6 isolate the MCUs from the periphery during internal power cycles. This way, it is assured that the semiconductors are made potential free in order to recover from latch-up states.

4.3.3 Software Implementation

The combination of multiple cascaded hardware and software implemented watchdog stages helps to ensure continuous operability of the satellite. In most failure cases sufficient functionality of crucial subsystems can be achieved by automatic initiation of hard-resets,

power cycles, and hardware redundancy selection in order to allow extensive analysis and maintenance to be commanded from ground.

Besides hardware controlled warm-backup, the core module's hardware implementation is capable of supporting more complex redundancy schemes. Due to the architecture's master-slave topology with high-speed data cross-connection even hot-redundant MCU operations in terms of runtime state synchronization and verification could be implemented in software. However, for typical housekeeping operations momentary intermissions of software execution can be accepted as a complete state recovery during soft- and hardware re-initialization can be performed within fractions of a second.

Nevertheless, a crucial requirement for reliable operations recovery is the integrity of the code section in the microcontroller's persistent memory. The sensitivity to radiation effects of the flash memory's floating gate cells might be small compared to typical SRAM cells. However, its relative abundance and comparably high hazard rate (see section 4.4) increases the effective failure cross section of the instruction memory.

In order to protect the flash memory's floating gate cells from corruption due to single event effects or total ionizing dose induced prompt or anneal effects, check and recovery algorithms can be executed periodically. Many error detection and correction methods for memory protection can be found in literature, most of them focus on minimizing the necessary memory overhead. In case of the ultra-low power core module the limiting factor is mainly execution time. Thus, a simple runtime-optimized procedure for mutual protection and recovery operation via the JTAG cross connection has been implemented.

For this purpose, the entire software image is maintained in redundant copies on both MCUs. As can be seen in figure 4.11, the flash memories of both MCUs are partitioned into three regions. The first region of the master LP (local program) stores the executable program memory, which is actively used by the microcontroller for operation. A second region LR (local replication) stores a clone of the program memory. A third smaller region LC (local checksums) stores two bytes pseudo signature analysis[3] (PSA) checksums for each segment of the program memory. This setup allows a single MCU to verify its own flash memory locally and recover corrupted segments if necessary. In normal operation, when both MCUs are physically operational, also the redundant information on the slave (remote) device is used. Using the remote microcontroller's Embedded Emulation Module via the JTAG cross-connection a complete pseudo signature analysis checksum of the entire flash memory of the remote device can be calculated within less than 3 seconds to be compared with the local checksum on the current master device. The advantage of the PSA is that it is part of the EEM hardware implementation and can therefore be calculated

[3] see Texas Instruments - MSP-GANG430 User's Guide

remotely without the need for transmitting the entire memory content.

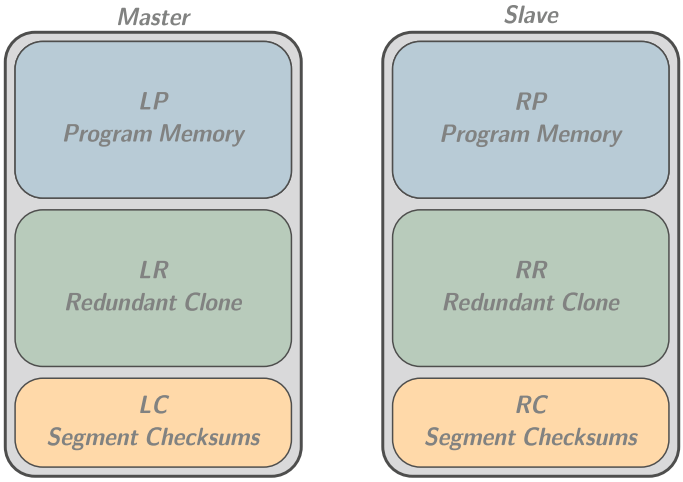


Figure 4.11: Flash memory organization storing redundant copies and checksum tables on each microcontroller unit.

If the quick checksum comparison of the entire remote flash fails, corrupted segments are quickly identified by fast segment wise checksum comparisons. Erroneous segments are recovered by using quick bitwise majority voting incorporating local and remote redundancies.

Let *LP* be a bit in LP, *LR* be a bit in LR and so on. Then, Table 4.12 represents the quadrivalent majority voting (*QMV*) incorporating all four redundant copies of the program memory image.

QMV		$\overline{RP}$		*RP*	
		$\overline{RR}$	*RR*	$\overline{RR}$	*RR*
$\overline{LP}$	$\overline{LR}$	0	0	0	x
	LR	0	x	x	1
LP	$\overline{LR}$	0	x	x	1
	LR	x	1	1	1

Figure 4.12: Karnaugh diagram representing bitwise majority voting with four redundancies.

The red marked x-values denote the combinations of *LP*, *LR*, *RP*, and *RR*, which are not unambiguously decidable as no clear majority emerges. The quadrivalent majority voting function can be quickly calculated by evaluating the following two expressions:

$$C1 = (LP \wedge LR) \vee (RP \wedge RR) \tag{4.1}$$

$$C2 = (LP \vee LR) \wedge (RP \vee RR) \tag{4.2}$$

Regarding the Karnaugh diagrams for $C1$ and $C2$ (see figure 4.13) it can bee seen, that the quadrivalent majority voting is decidable if and only if $C1 = C2$ whereas its result is then simply defined by $QMV := C1\ (= C2)$.

$C1$		$\overline{RP}$		RP	
		$\overline{RR}$	RR	$\overline{RR}$	RR
$\overline{LP}$	$\overline{LR}$	0	0	0	1
	LR	0	0	0	1
LP	$\overline{LR}$	0	0	0	1
	LR	1	1	1	1

$C2$		$\overline{RP}$		RP	
		$\overline{RR}$	RR	$\overline{RR}$	RR
$\overline{LP}$	$\overline{LR}$	0	0	0	0
	LR	0	1	1	1
LP	$\overline{LR}$	0	1	1	1
	LR	0	1	1	1

Figure 4.13: Karnaugh diagram for $C1$ (left) and for $C2$ (right).

The advantage of this approach is that it can be calculated rapidly on large data arrays as the expressions can be evaluated just using AND and OR operations on whole data words. Thus, the bitwise majority decision can be calculated simultaneously for 16 bits on the used architecture with only 6 assembly instructions.

The utilized microcontroller architecture further allows reading memory content in so-called marginal read mode (Quiring, 2008). This refers to a technique where the floating gate cells of the flash memory can be read with adjustable charge thresholds. The technique allows to reveal bit-corruptions in terms of insufficiently charged or insufficiently erased memory cells even when the corruption does not yet take effect in normal read mode.

4.4 Verification Tests

Testing described hardware and software recovery mechanisms by exposing the system to sources of ionizing radiation such as produced by particle accelerators is a complex and expensive undertaking. Fortunately, meaningful testing can often be accomplished by Software Implemented Fault Injection (SWIFI). It is clear that these techniques might not achieve the same target reachability as radiation tests because not all potential fault targets might be accessible by software (Ziade et al., 2004). Nevertheless, SWIFI techniques can constitute a simple and cost-efficient alternative to hardware based testing approaches such as heavy ion radiation.

4.4.1 Software Implemented Fault Injection

Various Software Implemented Fault Injection approaches for specific platforms and operating systems are available and some have been especially developed and used for space applications such as JIFI from JPL[4] which focusses on various Power PC architectures (Some et al., 2001).

In order to enable SWIFI analysis of the embedded core module a lightweight fault injector service has been implemented. The service basically runs in the background and receives commands via the core module's debug interface. Upon request, the service modifies either the remote or the local memory content at any specified address location in flash memory or RAM. For this purpose the current program execution is paused for a moment while the modification is performed. The injector allows to alter each addressable memory location on bit-level by flipping the information or by overwriting it with a specified value. In case the fault injection addresses code segments of currently executed instructions, the byte code being responsible for injecting the modifications is copied and executed from RAM in order to enable erasure and re-programming of the corresponding memory segment.

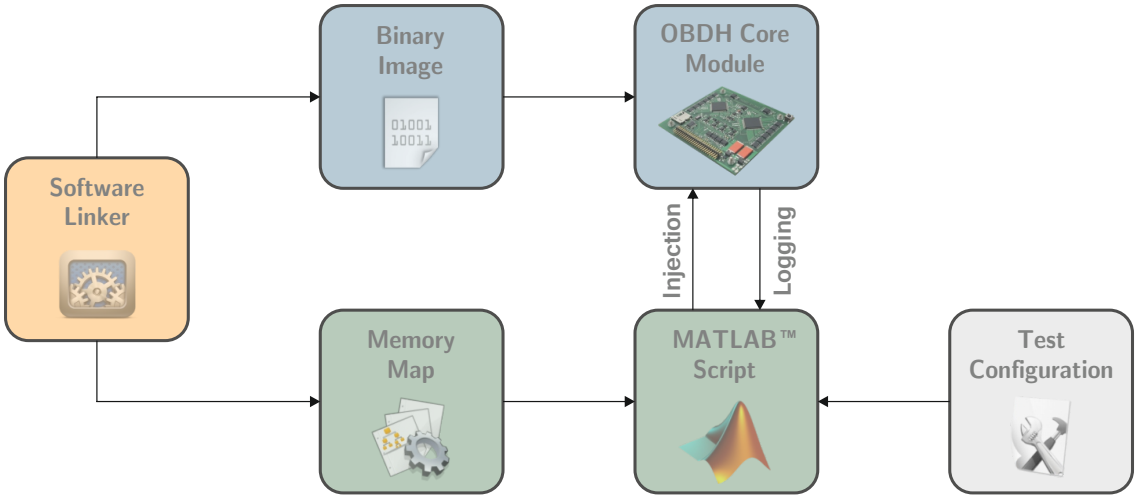


Figure 4.14: Software implemented fault injection and fault logging test setup.

The embedded SWIFI service is controlled via a PC which coordinates the fault injections and logs the system's response. The complete test setup is depicted in figure 4.14. After compilation of the core module software, the linker generates the corresponding binary image and a memory map file with the memory linking information. Once the

[4] Jet Propulsion Laboratory

binary image is flashed to the core module it is automatically replicated locally according to the mentioned redundancy scheme and further cloned to the remote device via the JTAG interface cross-link.

A MATLAB script automatically scans the memory map file including the symbol addresses of all linked variables and functions. An additional configuration file stores relevant parameters of a test campaign. According to the configuration, the script requests bit error injections at individual rates for different regions in the entire address range of both microcontrollers via the debug communication link. With the help of the memory map information, specific regions like RAM, TEXT, or even individual modules, functions or variables can be exposed to systematic fault injections whereas other memory regions such as the link location of the fault injection service can be excluded. The script further monitors the core module and logs events like prompt resets, system hangs, TWU recovery, PCU recovery, etc. during test execution.

4.4.2 Bit-Error Injection Test Campaign

Depending on the target memory location, a bit error might induce different effects on program execution. These can range from negligible modifications in unused memory regions to severe hardware misconfigurations or critical modifications in state or program memory, resulting in total unresponsiveness of the system. Some fault injections might result in prompt device resets caused by security violations or vacant memory access. Thus, direct resets would interrupt the current program execution but would not endanger mission operations in general. The role of the employed hard- and software based recovery mechanisms is to identify harmful failure states and recover the system in a timely manner to ensure accessibility from ground segment.

In an extensive long term test campaign more than one million bit errors have been injected in the entire memory address space of the running core module during normal operation. In order to reveal deviations in failure sensitivity to bit errors, injection tests have been conducted separately for individual memory regions like periphery registers (PER), statical allocated RAM (BSS), stack (STACK), and local program area (LP) in the microcontroller's flash memory. Besides observation of induced direct resets, the effective initiation of TWU and PCU recovery procedures has been monitored to verify robust operation of the system.

An overview of the test campaign is given in table 4.1. The entire test series has been conducted within 19 days, whereas each memory region has been exposed to continuous bit error injections for several days. The SRAM based target regions PER, BSS and

STACK have been exposed to an injection rate of one bit error per second. As the injection procedure is more complex in flash memory, a reduced injection rate of one bit error every 20 seconds has been chosen for the program memory LP to ensure that a significant majority of CPU time is available for regular task execution.

Target:	PER	BSS	STACK	LP
Size (bytes)	4096	4332	4096	131072
Runtime (hrs)	93	138	141	71
Injections	299741	290580	436947	10801
Unrecoverable	0	0	0	5
Reset Recoveries	3443	1583	650	859
PCU	11	34	4	39
TWU	576	1334	509	343
Direct	2856	215	137	477

Table 4.1: SWIFI test campaign overview.

After about one million error injections a little bit more than 6.5 thousand recovery procedures and prompt resets have been observed. As the most important result the system could demonstrate to recover from virtually all provoked failure states. In about 56 % of the cases the injection sequence resulted in a prompt reset of the active microcontroller while 43 % of the injection sequences had to be recovered by either hard- or software based watchdog monitors, finally observed as TWU resets. In about 1 % of the cases an automatic power cycle has been initiated by the PCU hardware in order to recover the system.

In five cases during error injection in flash based program memory the test run had to be aborted. In these cases the system could not be recovered automatically anymore as the erroneous device prohibited accessed to its EEM via JTAG interface. However, performing flash erasure with significantly reduced supply voltage of the target microcontroller allowed manual recovery in all cases. It is assumed that the execution of infected code segments results in a severe hardware misconfiguration which prevents the physical JTAG interface from being accessed by external devices. Representing flash images could be recovered but no further investigations to reveal the causal effects for this rare cases have been conducted yet.

Despite essential verification of the system's robustness against bit error induced failure states in general, a more detailed evaluation of the individual failure sensitivities has been conducted by means of statistical survival analysis. As a basis for detailed survival analysis figure 4.15 depicts the relative frequencies of target specific injections resulting in different failure modes. While the detailed analysis can be found in appendix B.1, the most relevant

results are outlined in the following to complete this chapter.

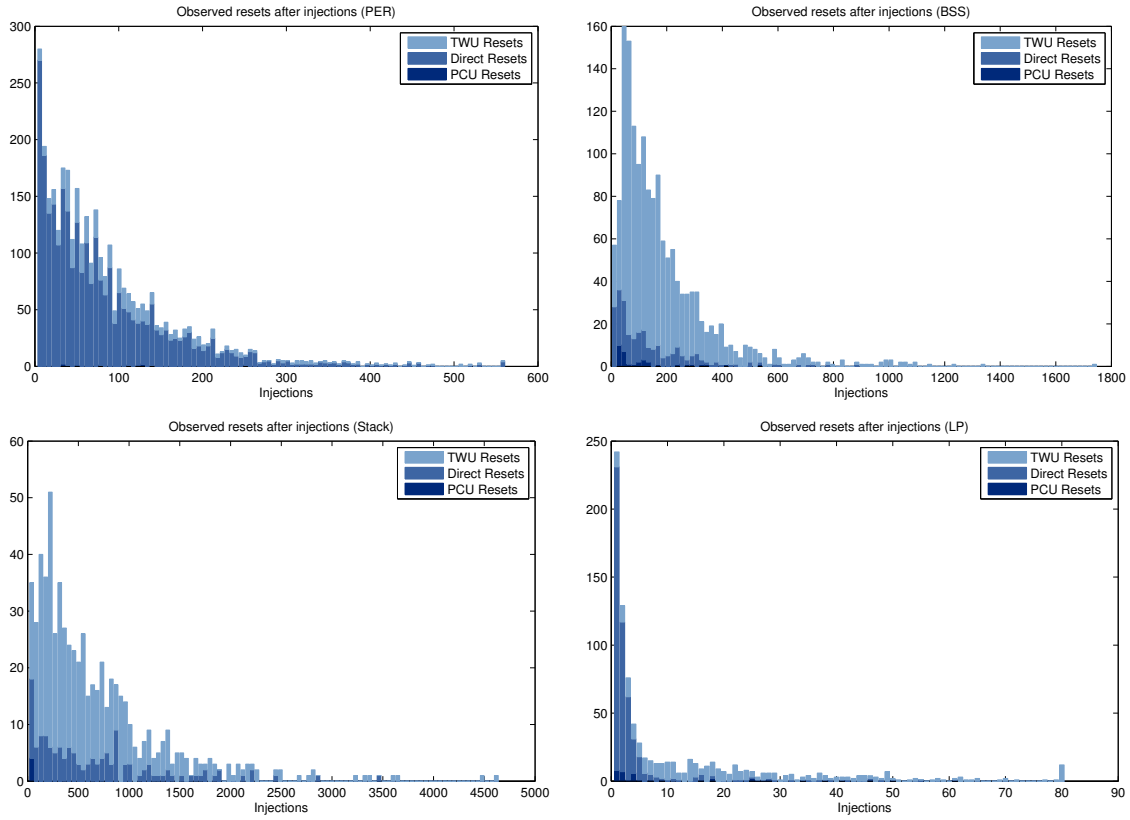


Figure 4.15: The number of bit-error injections until power cycle, toggle recovery or prompt reset occurred, displayed as stacked histograms.

As can be seen in figure 4.16, the sensitivity to different failure modes varies significantly for the individual target regions of the tested configuration. As expected, the most bit error sensitive region is the active program memory, showing both, direct resets and software hangs already after few injections. The PER region is significantly more sensitive to direct resets, mainly caused by register password violations. Injecting the BSS region predominantly results in system hangs, probably caused by information corruptions in the schedulers statically allocated memory. The most robust region with a median survival time of 477 injections seems to be the stack. However, this number might be misleading as the average stack size used at runtime is only about 20 % of the reserved memory space. Thus, it can be assumed that many injections hit a currently unused address.

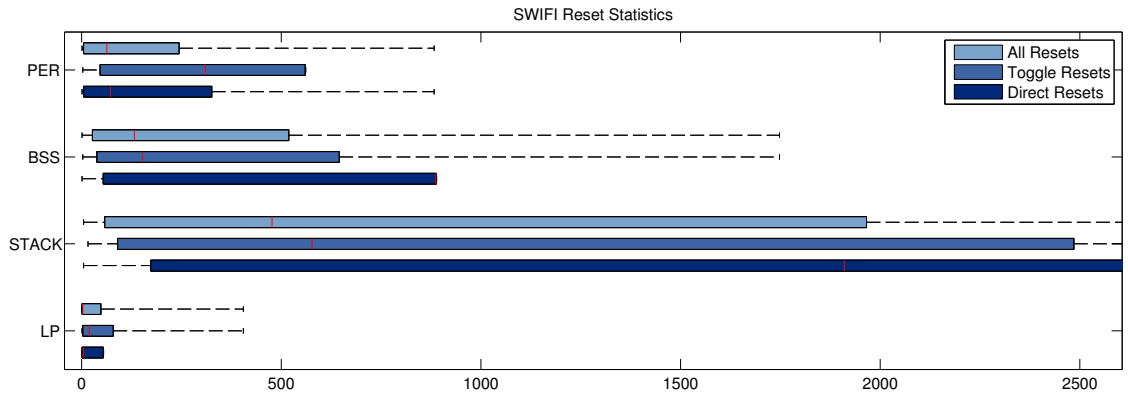


Figure 4.16: SWIFI survival analysis summary for different memory regions. The box plots indicate 5 % quantile ($Q_{0.05}$), median ($Q_{0.50}$), and 95 % quantile ($Q_{0.95}$) of estimated survival functions for the observed distributions shown in figure 4.15. The whiskers indicate observed minima and maxima. The complete analysis can be found in B.1.

4.5 Summary

This chapter addressed relevant aspects regarding the motivation, design, implementation, and test of the robust and energy-efficient onboard computer employed on UWE-3. A comprehensive overview of radiation effects and common mitigation techniques for customary microelectronics in space environment has been given. The current state-of-the-art regarding onboard computers for pico- and nano-satellites has been presented. The fundamental concepts of relevant soft- and hardware design aspects of the UWE-3 onboard computer have been elaborated in detail. Finally, experimental results from software implemented fault injection tests carried out for verification prior to launch have been discussed.

Operation experiences regarding the system's performance during the satellite's first year in orbit are further presented in chapter 5.1.3. Final conclusions regarding design, test, and operation of the onboard computer are consolidated in chapter 6.3.

5

UWE-3 Mission Operations

With successful launcher separation, automatic activation, and reception of first signals the UWE-3 mission operation phase has been initiated in late November 2013. As part of the mission commissioning phase, elaborate checkout and performance verification tests have been carried out during the first weeks of operation. The main objectives for commissioning of UWE-3 were to establish a reliable communication link with the ground segment, to assure stable orbital operating conditions, and to verify specific performance requirements of relevant subsystems as preparation for future payload operations. After presenting most important results regarding in-orbit operation performance of crucial subsystems, the remainder of this chapter provides an overview of general UWE-3 mission operations during the satellite's first year in orbit. In particular, experiments targeting communication link optimization and the evaluation of the experimental attitude determination and control system are addressed in the following sections.

5.1 General In-Orbit Operation Performance

In preparation for later experimental operations, intensive system checkouts and performance analysis tests have been carried out on the individual subsystems. The following sections present the most important results regarding thermal environment analysis, power budget verification, and first in-orbit operation experiences with the satellite's redundant onboard computer.

5.1.1 Thermal Measurements

After orbit injection, following 15 minutes after lift-off, UWE-3 quickly converged to its nominal thermal balance. As expected, the outer structure is subject to most significant

thermal variations. With a mean orbital temperature of $+4\,°C$ the satellite's side panels remain stable within $-25\,°C$ and $+29\,°C$ during 99 percent of the time. After active detumbling the temperature distribution of the panels changed slightly, now showing higher gradients due to the significantly reduced spinning rate of about $1\,\text{deg}\,\text{s}^{-1}$. Figure 5.1 shows a 24 hours temperature recording (after detumbling) from 25th January.

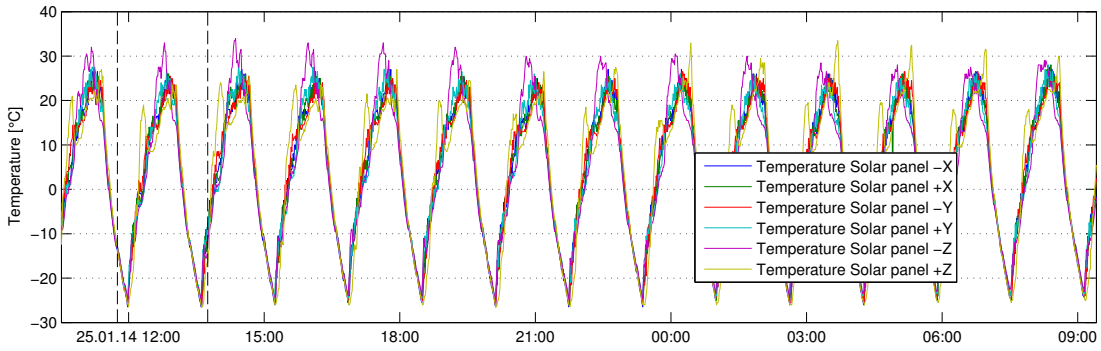


Figure 5.1: A 24 hour in-orbit temperature recording.

Figure 5.2 (left) depicts the temperature distribution of all side panels during a representative orbital period selected from figure 5.1. The maximum temperature gradient on the outer structure is limited by approximately 20 K, indicating a good thermal coupling between the individual panels. The maximum gradient typically occurs between the sun-facing Z-panel and its opposite while the satellite is slowly spinning about the Z-axis. The distribution of the orbital heat rate is depicted in figure 5.2 (right), showing an average temperature change of about $\pm 2\,K$ per minute. This peak rate usually occurs directly after transition from Eclipse to sun light end vice versa. However, due to directed energy transfer from sun the temperature rate during heat-up can be slightly higher on individual panels than for general passive cool down.

5.1.2 Electrical Power Performance

In the first weeks of operations special focus was put on the verification of the satellite's power management. Various measurement recordings have been downloaded in order to ensure proper power generation of the tumbling satellite and to verify proper battery management in the course of several days. Further, all subsystems have been tested for their principle function and legal power consumption. Several high power operation tests have been conducted as preparation for more power demanding experiments while the system has been carefully monitored in order to reveal unexpected performance degradations.

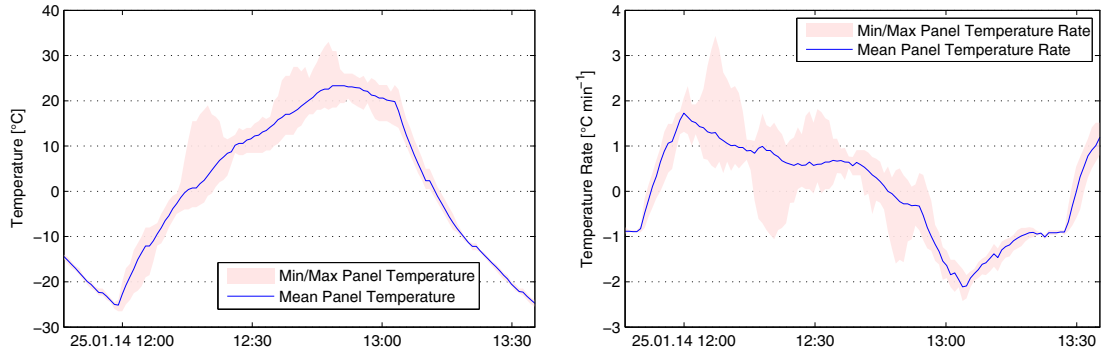


Figure 5.2: Temperature distribution in outer structure during a representative orbit (left). Temperature rate distribution in outer structure during the same orbit (right).

As it can be seen in figure 5.3, the temperature inside the interior battery case varies only slightly within an orbital period. The MLI shield effectively kept the temperature sensitive Lithium-Ion batteries between +9.5 °C and +4.5 °C in January 2014. Besides a residual orbital temperature cycle of about 4 K an additional daily variation around 2 K can be measured inside the battery case.

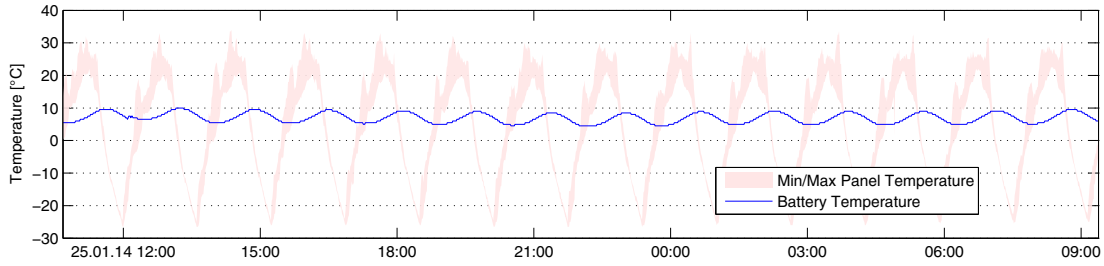


Figure 5.3: A 24 hour in-orbit temperature recording of battery temperatures related to maximum and minimum satellite temperatures in outer structure.

Further, an additional seasonal variation in the order of 5 K can be observed along with temporal temperature peaks due to increased power consumption of the satellite during power demanding experiments (figure 5.4). However, as the temperatures stay robustly above 0 °C no extra heating is required.

Being launched with fully charged batteries UWE-3 converged to its expected power balance within several hours after orbit insertion. During normal operations the satellite consumes about 320 mW in total. This allows to maintain a stable charge state well above 90 percent of the battery capacity. Figure 5.5 shows a recording of the batteries charge state over time. The data also shows a regular redundancy switch over from power path A to power path B which is performed periodically for battery maintenance reasons. While

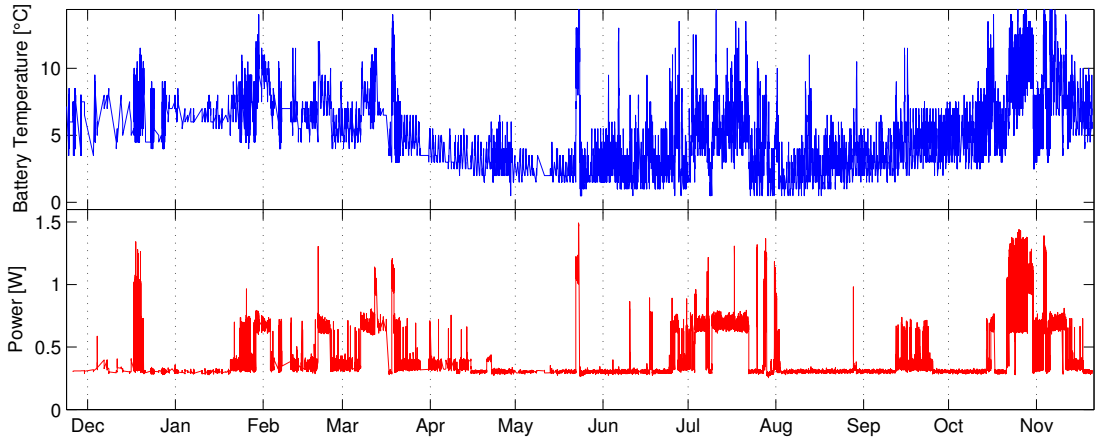


Figure 5.4: Seasonal temperature variation in thermally insulated battery case and total power consumption.

battery B takes over the full load, battery A is able to recharge completely within a few hours.

With 320 mW nominal power consumption the UWE pico-satellite bus provides a comfortable power margin to be used for payload operations. In case of UWE-3 the average power consumption adds up to 365 mW when attitude determination is operating in nominal mode while high precision attitude determination with continuous gyro sampling dissipates 675 mW in total. In preparation for the commissioning of the reaction wheel a power budget test has been performed to ensure proper operation of the reaction wheel and the wheel drive electronics which itself consumes about 400 mW in standby operation.

Figure 5.6 shows a similar recording of power, charge-state and battery temperatures of a long-term high power test during early operations. The graph depicts the activation of the high power mode continuously consuming about 1.1 W. After 16 hours the mean charge state stabilized at 70 % whereas the mean battery temperature can be observed to increase by 5 K. The reason for the drop in mean charge state is that the utilized Lithium-Ion batteries limit the charging rate when operating in constant voltage charge mode, which is the case between 80 % and 100 % state-of-charge. After reduction of the power consumption by activation of normal operation mode (with attitude determination) both, charge state and battery temperature converge to initial values again within several hours.

Similar performance could be achieved during a high precision and high duty cycle magnetic control experiment where the system could demonstrate robust provision of $1.1 - 1.2$ W orbit average power for several days (see figure 5.7). However, a further power demanding experiment with more than $1.5 - 1.7$ W orbit average power consumption had

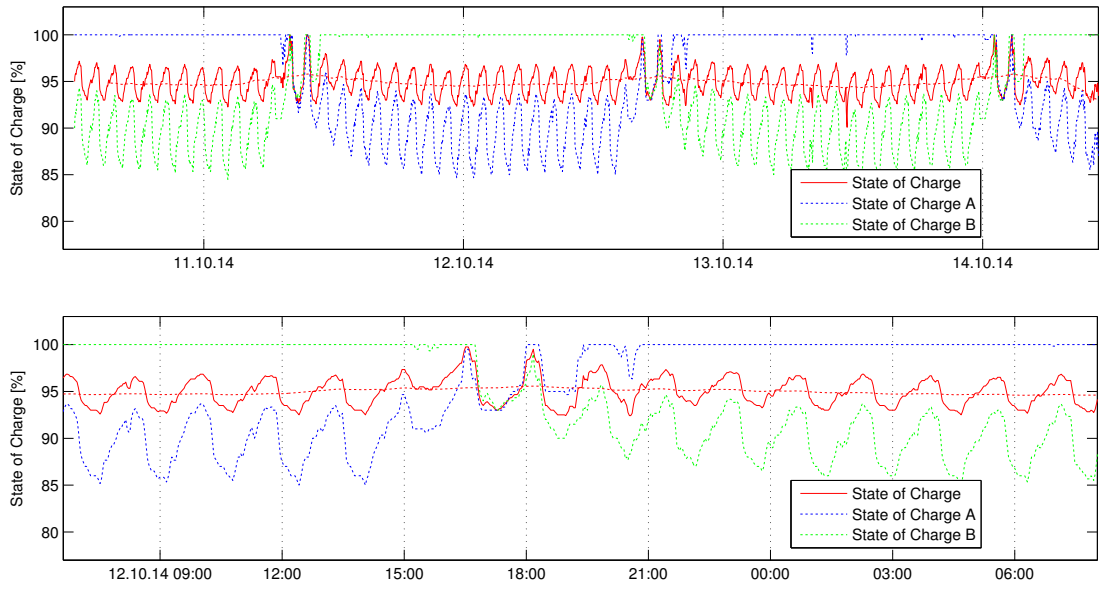


Figure 5.5: Charge state recordings during normal in-orbit operations (top) and regular power path switch over (bottom).

been aborted after eight hours by the satellite's safe mode when both batteries eventually dropped below 30 % state of charge.

5.1.3 Onboard Computer Operations

Since launch on November 21st the redundant low power onboard data handling core module is operating without interruptions. As expected the system's power consumption stays well below 10 mW while its temperature remains within −12 °C and +22 °C. On satellite activation the core module started operation with microcontroller unit (MCU) A as master, and MCU B as slave in sleep mode. After 17 days of operation on December 8th the autonomous toggle watchdog unit (TWU) switched over to the B unit as the A unit failed to trigger the TWU in time. No corruption in the flash-based program memory of MCU A could be identified by the B unit. Several similar events have been observed in the following months.

In order to investigate the impact of radiation on the system, a region of 8 kB unused RAM has been monitored starting from mid of January 2014. In order to identify single event upsets in both, the active master MCU and the slave MCU in sleep mode, PSA checksums of the target memory regions have been requested manually as part of regular satellite operations. With a total number of five upsets observed in about four months of operation the SEU rate of the employed technology can be roughly estimated to be

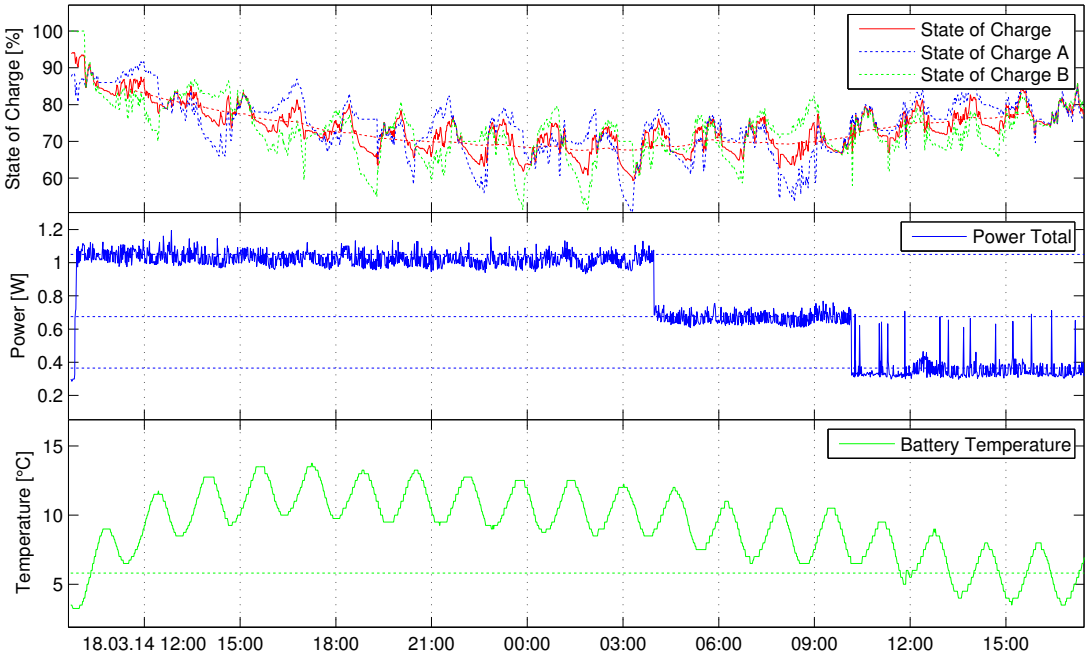


Figure 5.6: Power, charge state and battery temperature recordings during in-orbit power budget verification tests.

in the order of $10^{-6}\,\mathrm{bit}^{-1}\mathrm{day}^{-1}$ (see equation 5.1) which reflects a typical error rate for commercial CMOS components in LEO.

$$SEU_{MCU} = \frac{5}{120\,\mathrm{days} \times 16384\,\mathrm{bits}} \approx 2.5 \cdot 10^{-6}\,\mathrm{bit}^{-1}\mathrm{day}^{-1} \tag{5.1}$$

On the 20th of April 2014 a latchup has been identified on the satellite, indicated by a minor increase of nominal power consumption in the order of 50 mW. However, the fault did not cause any noticeable interference and has been resolved autonomously by a subsequent toggle to the redundant processing unit.

Figure 5.8 indicates the observed events during the first six months of mission operations. The event times are correlated with measures for solar activity such as solar proton flux and compression of the Earth's magnetosphere as measured by the geostationary GOES-13 satellite. The solar proton flux for energies greater than 10 MeV indicates solar proton events whereas a flux exceeding $10\,\mathrm{p\ cm}^{-2}\mathrm{s}^{-1}\mathrm{sr}^{-1}$ constitutes a typical threshold where ionization starts to occur (Feynmann and Gabriel, 2000). Further, GOES-13 Hp measurements represent the Earth magnetic field component parallel to the Earth's rotation axis (Singer et al., 1996). Here, significantly reduced values near zero or less can indicate a compression of the magnetosphere or strong currents associated with magnetic substorms.

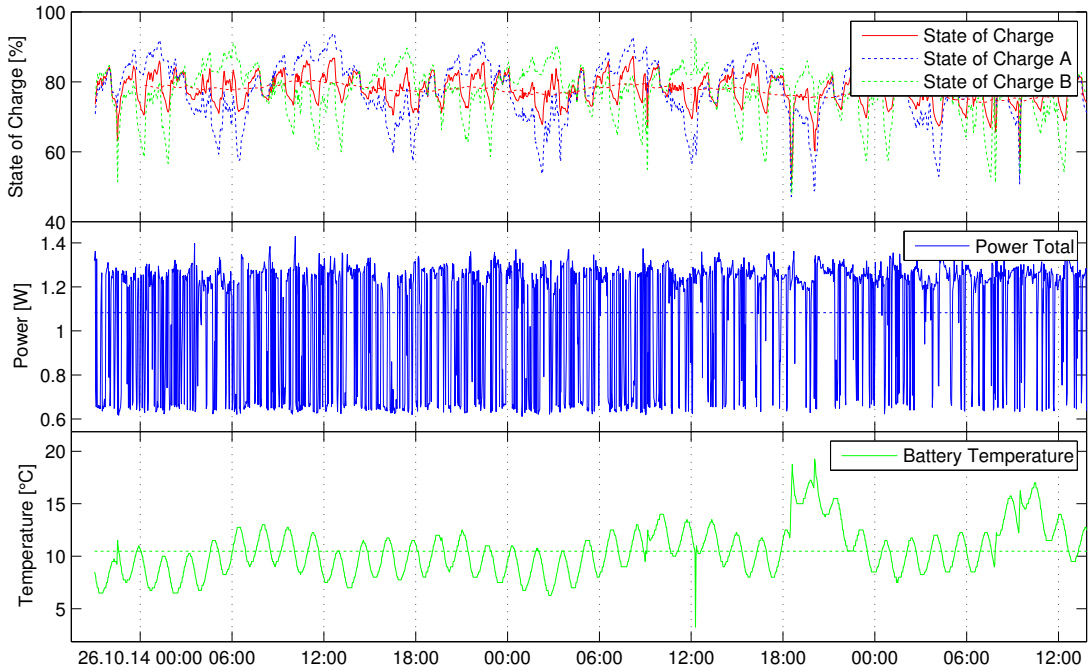


Figure 5.7: Power, charge state and battery temperature recordings during attitude control experiment in high precision mode.

However, due to the small number of events observed and the missing capability for automated onboard event time logging no clear correlation between observed anomalies and solar events can be identified.

Besides automated warm-backup, the onboard computer's redundancy scheme supports fail-safe in-orbit software updates which has been successfully demonstrated after the first six months of operation. In mid of June 2014, a binary image of an extended onboard software has been uploaded to the satellite's file system and subsequently flashed to the redundant MCU by the current active device. After updating the remote flash memory via the microcontroller's JTAG/EEM cross connection, the remote code section has been verified before manual switch-over to the upgraded system. In the case of an unexpected malfunction, the TWU would have initiated a fail-over to the intact device and the initial configuration of the updated device could have been recovered easily.

Among several new features and experiments mainly targeting link quality optimization, an experiment for automated single event upset observation and recording has been installed onboard the satellite in the context of the software update. Besides exact event time identification in order to be able to correlate individual events with the instantaneous orbital position the experiment allows to identify multi-bit-errors by bitwise content verification.

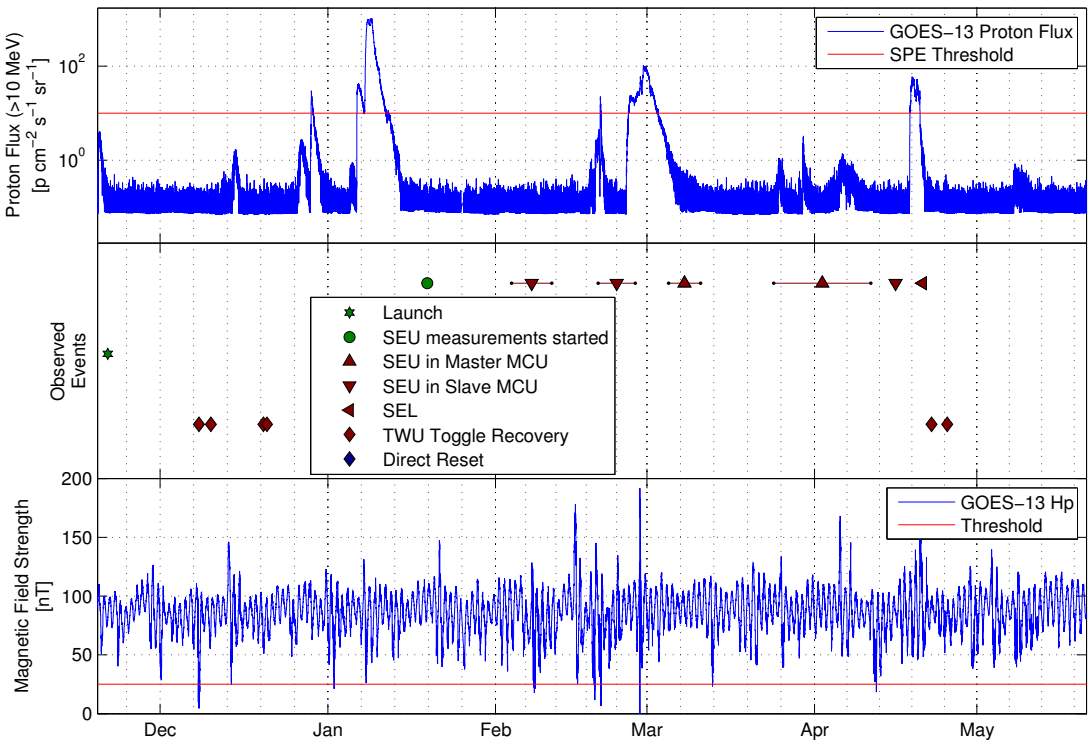


Figure 5.8: Observed events in the satellite's onboard data handling core module during the first six months of operation correlated with geostationary solar proton flux and geomagnetic field measurements from GOES-13. Event times for memory upsets before June 2014 are annotated with whisker plots indicating the related measurement interval.

Since June 2014 four upsets could be identified in the observed target regions of the active master unit as well as on the inactive slave unit in stand-by mode. None of the identified events produced multi-bit errors in adjacent memory regions. Figure 5.9 indicates the observed event times without any significant direct correlation with solar activity. However, the knowledge of exact event times allows to correlate the satellite's instantaneous location with the estimated radiation environment in low Earth orbit as depicted in figure 5.10. The presented plots show the individual event locations overlaid on the estimated orbital proton and electron environment in the satellite's orbit. Thus, it can be seen that the majority of the observed events might be related to radiation effects within polar regions of the radiation belts as well as within the south atlantic anomaly.

Even though the majority of observed TWU recoveries are located within orbital regions of increased radiation, their relative abundance compared to observed upsets in RAM is noticeable. Taking into account that only a comparably small fraction of bit-errors result in TWU recoveries not all events might be explained by radiation effects

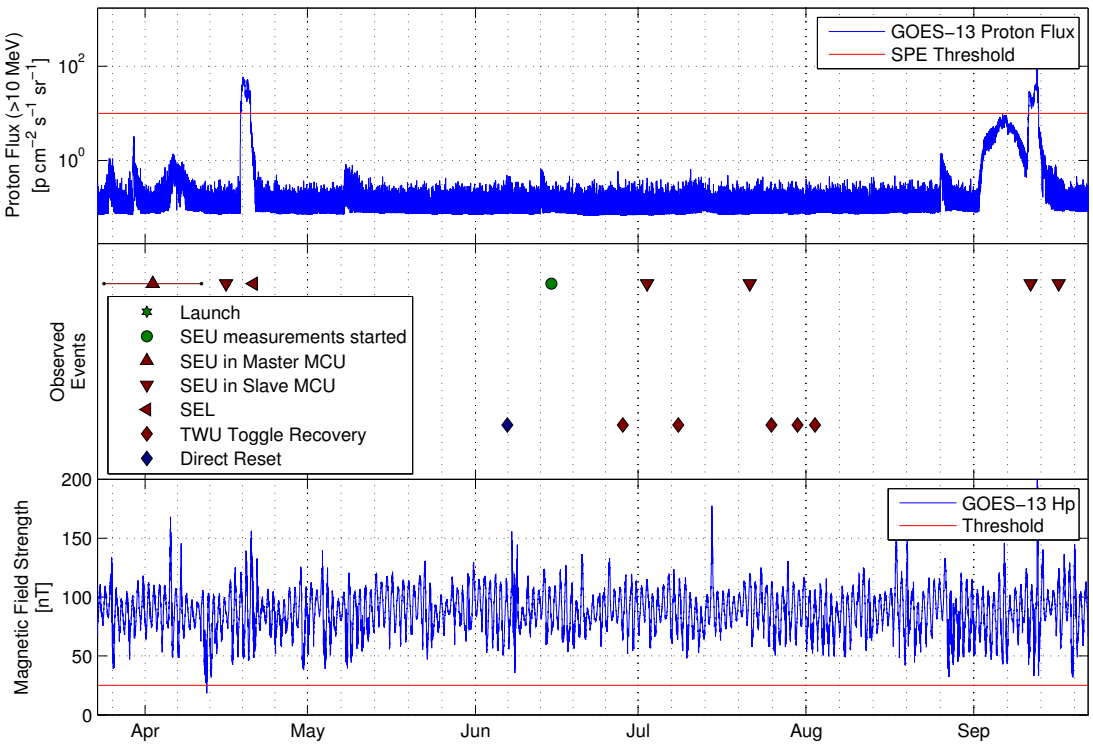


Figure 5.9: Observed events in the satellite's onboard data handling core module after installation of enhanced monitoring capabilities in June 2014. Events are correlated with geostationary solar proton flux and geomagnetic field measurements from GOES-13.

in addressable memory regions alone. Potential reasons for unexpected failures include remaining software bugs which could not be revealed during long term testing on ground, or transient radiation effects in logic gates of the mircocontrollers processing core and periphery.

However, no significant intermissions of the core module's operation has been observed since launch in late 2013. Further, no data corruption in flash memory could be identified before and after software update in June 2014.

5.2 Uplink Interference Analysis

UWE-3 employs two fully redundant UHF transceivers with separate omnidirectional monopole antennas operating in the 70 cm amateur radio band (435.000 MHz - 438.000 MHz). While the satellite's transceivers provide about 1 Watt transmit power the university's groundstation operates at 70 W on a 3 m cross-yagi antenna with 14 dB gain.

From beginning of satellite operations the downlink quality from the satellite to ground

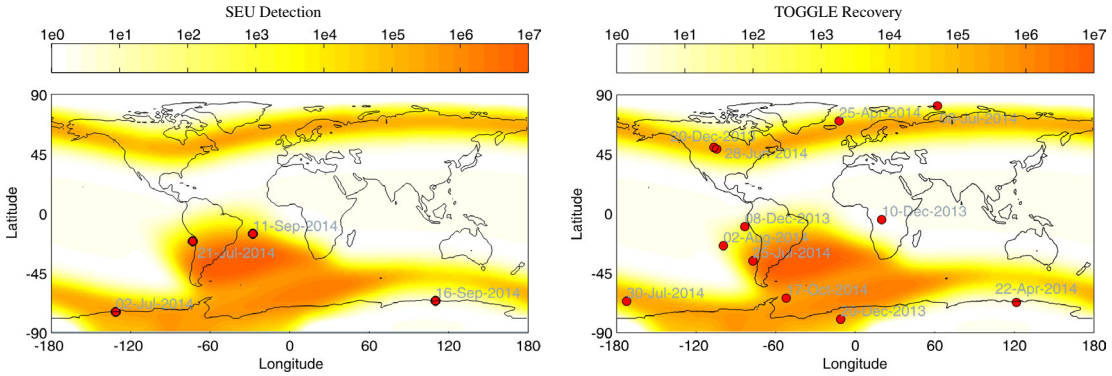


Figure 5.10: SEE locations for SEU detection and TWU recoveries with two minute scan interval. Overlay on Electron ($> 0.04\,\text{MeV}$) and Proton ($> 0.1\,\text{MeV}$) MAX Integral Flux ($\text{cm}^{-2}\text{s}^{-1}$) according to AE-8/AP-8 models as simulated with SPENVIS for the UWE-3 orbit.

was excellent, showing high signal strengths even at low elevations. However, the telecommand uplink was initially difficult with transmission failure rates between 80 % and 90 %. From beginning of 2014 the uplink quality degraded further, resulting in average failure rates between $90-95\,\%$ which could sporadically extend to $98-100\,\%$ for several passes while still providing excellent downlink quality.

Both, ground and space borne hardware defects could be excluded from potential failure sources as the problems remained when operating on the redundant devices. The problem has been further analyzed by performing various automated uplink tests. In order to efficiently identify the uplink success rate short data frames containing a unique id have been frequently uplinked directly to a file in the satellite's flash memory without acknowledgement requests. In the course of the test, parameters such as offsets in antenna pointing or uplink frequency have been altered randomly. After downloading the file, the received frame ids could be directly compared with the uplinked frame ids to correlate the success rate with instantaneous frequency offset, satellite position, etc. As it can be seen in figure 5.11 (left) a potential frequency drift, e.g. caused by temperature variations at the satellite's receiver, could also be excluded as failure source as the success rate is not affected by slight frequency deviations. However, it could be identified that the uplink quality significantly changes in general within the amateur frequency band and further slightly varies with the satellite's relative location.

Following a trial-and-error search on different frequencies a good candidate has been found such that the uplink quality could be improved significantly and the satellite operations and experiments could be conducted more efficiently again.

With the software update in June 2014 several new experiments targeting the analyzation

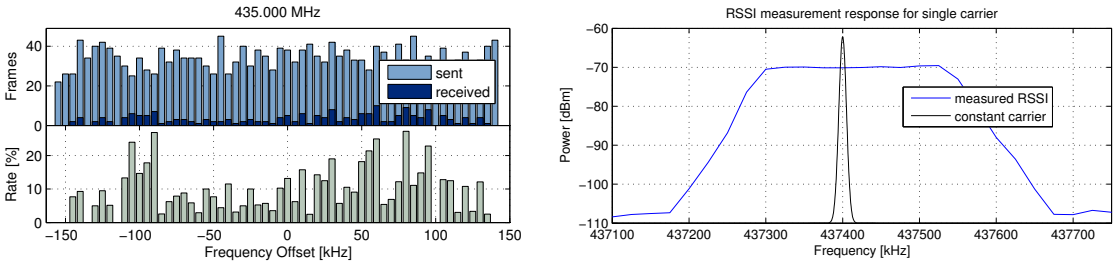


Figure 5.11: Exemplary uplink quality analysis based on a ground based frequency sweep around 435.000 MHz ± 150 kHz from 15/16 April 2014 (left). RSSI frequency sweep with $C_f = (437.100\,\text{MHz}, 437.800\,\text{MHz}, 20\,\text{kHz})$ and $C_a = (1000\,\text{ms}, 1, 3)$, showing the receivers response to a constant carrier signal at 437.400 MHz (right).

of the link quality have been installed on the satellite. In order to further analyze the spatial distribution of in-situ interference levels for the whole amateur radio spectrum, an RSSI frequency sweep experiment has been implemented. The experiment allows to monitor and log measured RSSI noise levels while automatically scanning over a specified frequency range. Beside start and stop time the experiment allows to configure target frequency range and scan interval $C_f = (f_{start}, f_{stop}, \Delta f_{step})$. Further, the data acquisition can be controlled with parameters for RSSI sampling rate, number of averaged samples in a measurement and number of repeated measurements for a single frequency $C_a = (t_s, n_b, n_m)$.

As the onboard radio itself is used for the RSSI sampling first the device response to a single carrier has been determined on the engineering model on ground. As can be seen in figure 5.11 (right) the RSSI measurement is sensitive to a range of $f_{base} \pm 110\,\text{kHz}$ when the radio is configured to a specific receive frequency f_{base}.

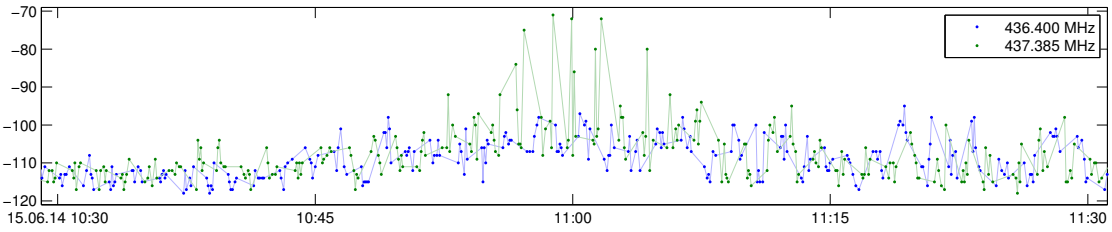


Figure 5.12: RSSI noise levels [dBm] measured onboard UWE-3 during a pass over central Europe without groundstation operations in Wuerzburg. $C_f = (436.400\,\text{MHz}, 437.385\,\text{MHz}, 985\,\text{kHz})$, $C_a = (5000\,\text{ms}, 1, 6)$.

Figure 5.12 shows an in-orbit frequency sweep recording from 15th of June when UWE-3 had a high elevation pass-over in the west of Wuerzburg. Throughout the entire measurement the signal emission from our groundstation has been deactivated. It can be seen that the background noise level increases about 5-10 dB on both observed frequencies

when the satellite passes Europe. Further, it can be noticed that the 437.385 MHz is exposed to severe interferences over central Europe with RSSI peak levels ranging up to −70 dBm while the 436.400 MHz is not affected by this source. These measurements could be repeated several times and are representative for the observed time frame in third quarter of 2014.

Described observations lead to further experiments targeting the global spatial distribution of interferences on the entire UHF amateur radio band used for satellite operations. Several frequency sweeps have been recorded in third quarter of 2014, each lasting several days to ensure global coverage. The results discussed in the following base on measurements recorded between 06.08.2014 and 11.08.2014 and are representative for the observations made. The recording comprises more than 100.000 data points downloaded from the satellite in a 1.5 MB compressed data file. The measurements have been recorded with configuration parameters $C_f = (435.000\,\text{MHz}, 438.000\,\text{MHz}, 200\,\text{kHz})$ and $C_a = (250\,\text{ms}, 10, 2)$. In order to ensure the observation of sporadic short interference peaks a high sampling rate of 250 ms has been chosen. Each recorded measurement represents the average of 10 samples, thus reducing the amount of data produced. Figure 5.13 shows the recorded mean RSSI level from an exemplary data set versus base frequency f_{base} and time.

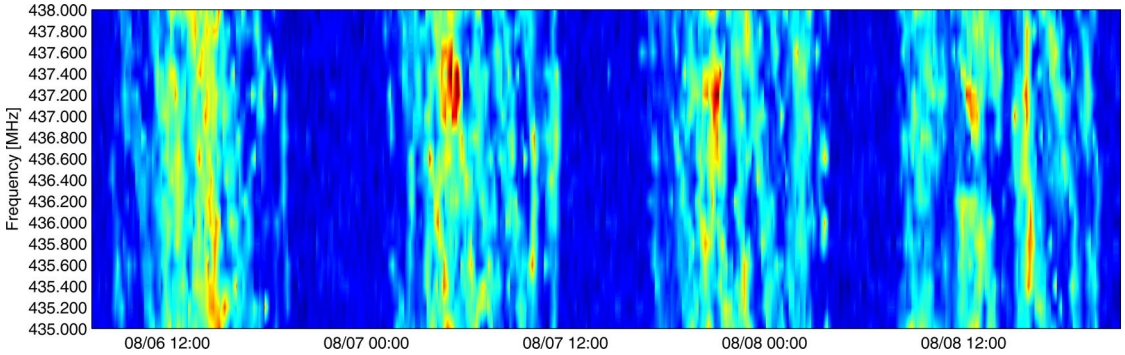


Figure 5.13: Extract of frequency sweep recording showing RSSI measurements [dBm] plotted against frequency [MHz] and time [UTC]. $C_f = (435.000\,\text{MHz}, 438.000\,\text{MHz}, 200\,\text{kHz})$, $C_a = (250\,\text{ms}, 10, 2)$.

The downloaded measurements have been mapped to their instantaneous sub-satellite points as visualized in figure 5.14. The recorded data points show sufficient coverage of the entire globe and can be properly used as a grid for spatial interpolation to generate a global interference map for each frequency under investigation.

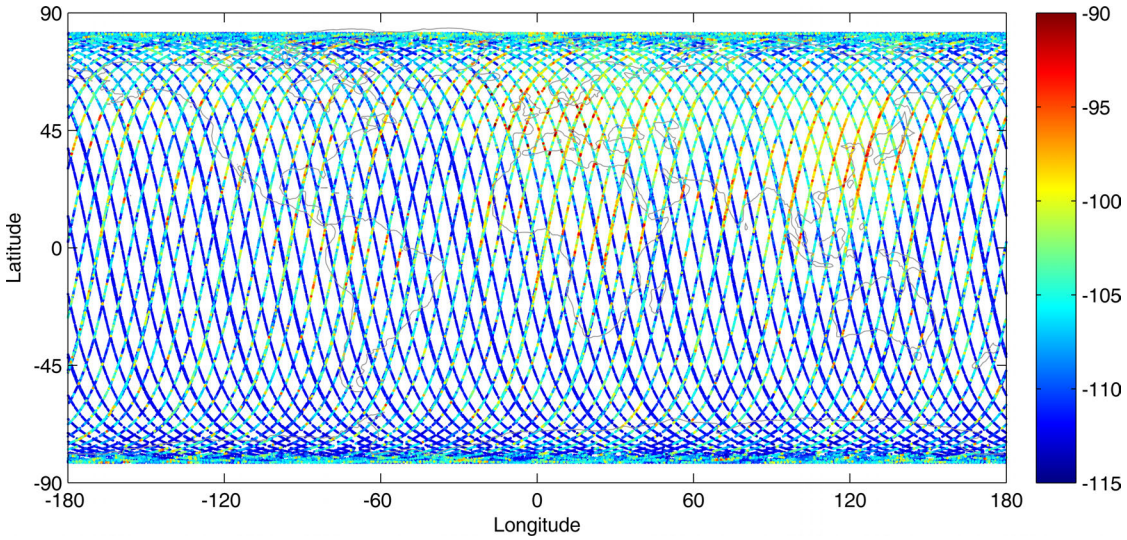


Figure 5.14: Recording showing RSSI measurement [dBm] plotted against satellite position.

The map interpolation results are shown in figure 5.15. It can be seen that the average interference levels vary significantly with location and observed frequency. Especially orbital regions connected to central Europe seem to be affected significantly on a wider frequency band between 437.000 MHz and 437.600 MHz.

In order to express these observation with concrete numbers a local statistical analysis has been made. For this purpose the measurements have been filtered for specific locations and frequencies in oder to calculate statistical measures such as median and quartiles of the underlying distribution of observed averaged RSSI levels. Figure 5.17 depicts the statistical analysis for two different regions. The first region is centered around the sphere of influence around our groundstation in Wuerzburg (see figure 5.16, left). The second region serves as an undisturbed reference with a selected region of similar size located somewhere in the south pacific (see figure 5.16, right).

Again, the plots clearly show the dependency in location and especially frequency, but it has to be pointed out that the underlying data points represent an average of 10 RSSI samples already. Therefore, the extreme interference levels as present in figure 5.12 are not directly visible anymore in terms of their real outlying value. However, it is ensured that these peaks contribute to the statistics such that the different frequencies can be compared with each other for frequency selection.

The results reflect our experiences when operating UWE-3 during the first six month after launch. They further underline the importance of proper frequency selection for satellites using the radio amateur bands. Moreover, the results emphasize the requirement

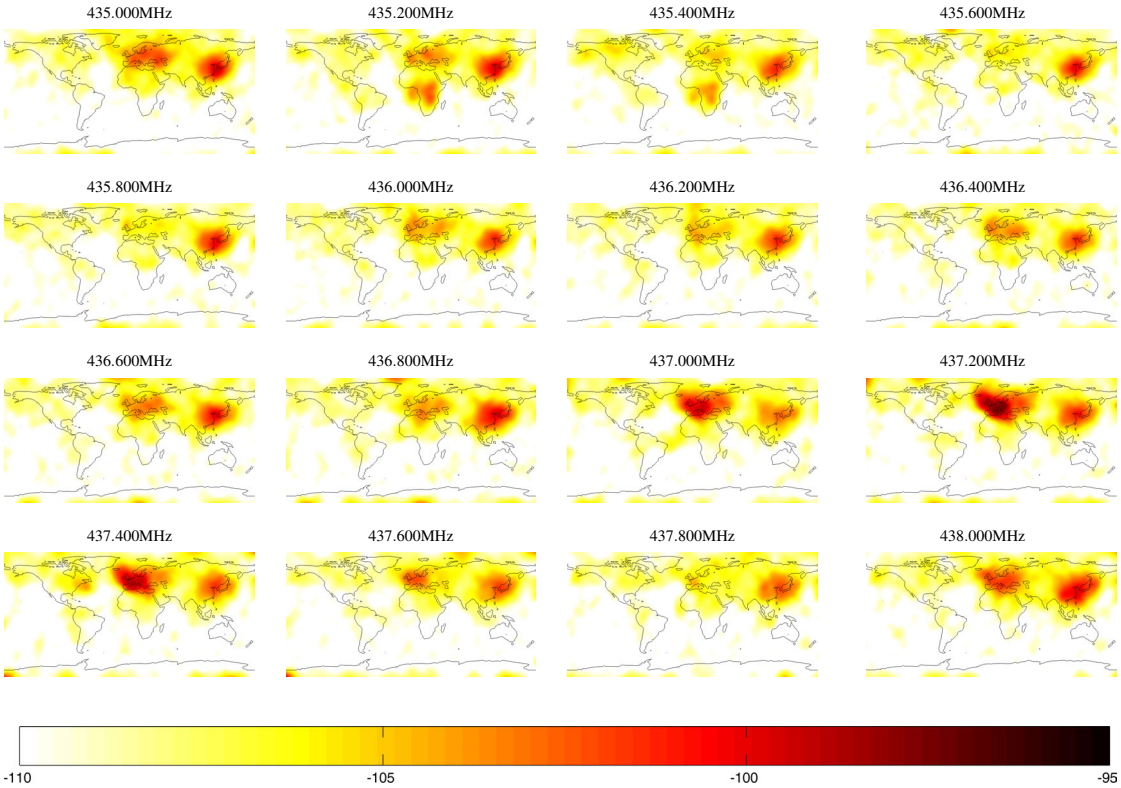


Figure 5.15: RSSI [dBm] average interference world plot between 06.08.2014 and 11.08.2014.

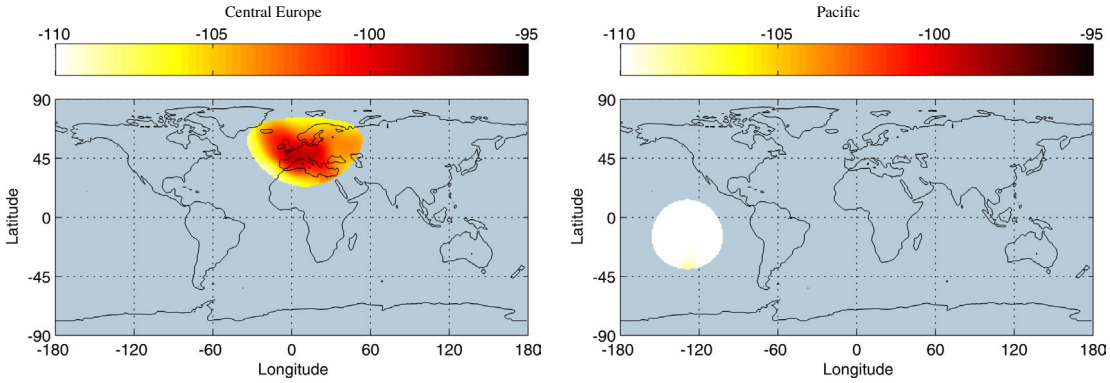


Figure 5.16: Reference world plots showing RSSI levels [dBm] for 437.400 MHz.

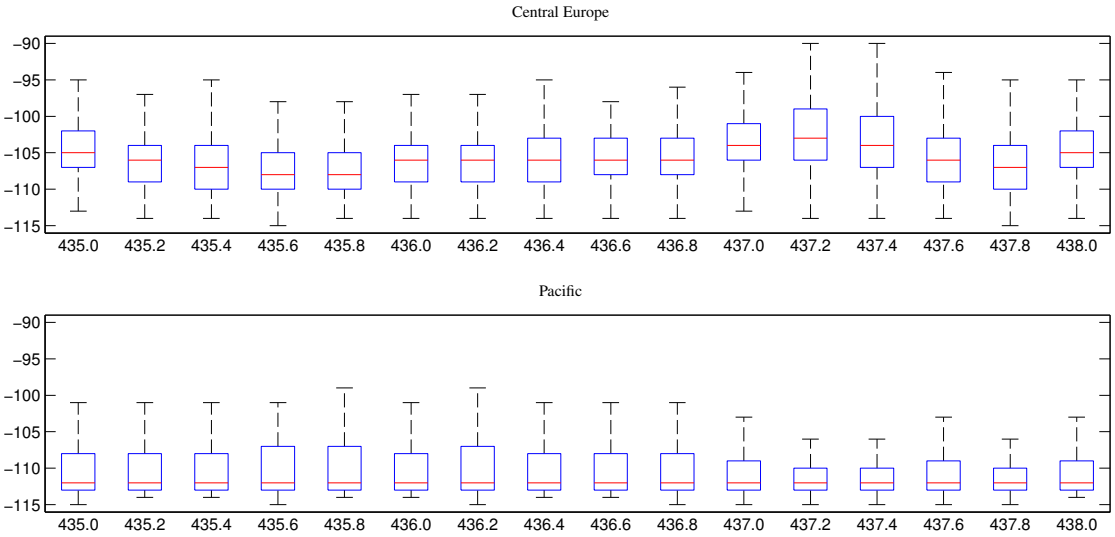


Figure 5.17: Average interference statistics for each frequency for Europe centered at groundstation in Würzburg (top) and for a reference without interferences over the pacific (bottom). (Box: first and third quartiles, median of RSSI [dBm] (10 samples averaged every 2.5 s); Whiskers: data in 1.5 interquartile range)

for in-orbit frequency re-configuration to be able to react to changes of inevitable global interferences caused for example by military space surveillance radars.

5.3 Experimental ADCS Operations

One of the UWE-3 mission objectives has been the demonstration and in-orbit performance characterization of its low-power coarse attitude determination and control system. Details on hardware design and related control concepts of the attitude determination and control system have been widely excluded from the content of this thesis documentation. Nevertheless, most important experimental results obtained during the first months of operations are summarized in the following to complete this chapter. Detailed information regarding experimental ADCS operations with UWE-3 can be found in (Bangert et al., 2014), (Busch et al., 2014b), (Busch et al., 2014a), (Bangert et al., 2015), and (Busch et al., 2015).

The experimental attitude determination and control system has been activated first on 3rd of December 2013, following two weeks of general satellite commissioning after launch of UWE-3. During the first two weeks of operation the system has been configured to perform continuous coarse attitude determination in low-power mode which adds about 60 mW to the total power budget of the pico-satellite. During this time various data sets

comprising raw sensor measurements and onboard attitude estimations have been recorded for detailed analysis. As can be seen in figure 5.18 (top, left) an initial tumbling rate in the order of 24 deg s^{-1} has been measured whereas the satellite was spinning predominantly about its x-axis which had been aligned perpendicular to the ejection direction from the launch adapter. In the absence of any active attitude control a natural rate damping in the order of 0.5 deg s^{-1} day^{-1} could be observed, together with periodic spin axis deviations correlating with the satellite's orbital rate (see figure 5.18, top, right).

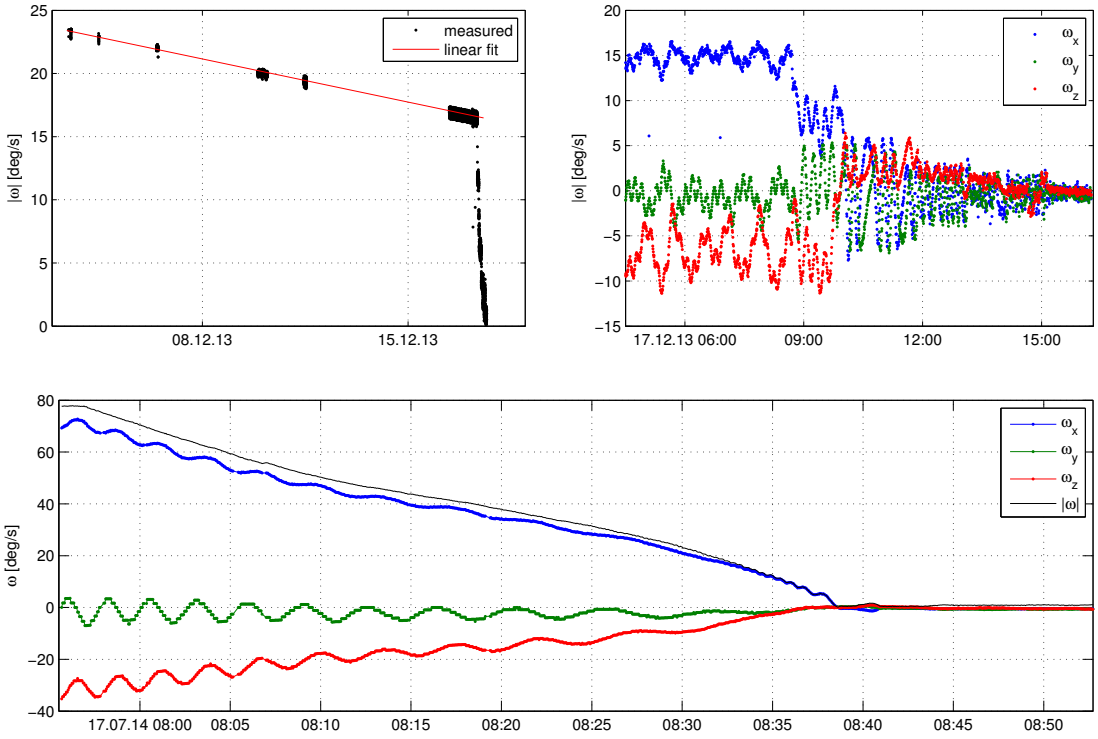


Figure 5.18: Initial tumbling rate, natural decay, and low duty cycle detumbling after launch (top). Performance test of B-dot control, despinning the satellite from 80 deg/s in about 40 minutes with 50 % duty cycle (bottom).

On 17th of December the onboard magnetic detumbling mechanism has been activated with a comparatively small duty cycle of the B-dot controller in the order of 2 % in order to maintain a conservative power budget. In the following hours the system could demonstrate the effective rate damping from about 16.5 deg s^{-1} to less than 1 deg s^{-1} during several minutes of active torquer operations (see figure 5.18, top). A similar experiment has been conducted on 17th of July 2014 after the satellite had been actively spun up to about 80 deg s^{-1}. As depicted in figure 5.18 (bottom) the satellite could be stabilized again within 40 minutes at about 0.7353 deg s^{-1} (RMS) while operating with 50 % duty cycle of the magnetic controller.

In order to assess the system's performance in terms of attitude determination accuracy a consistency analysis has been performed. Thus, large data sets comprising onboard attitude estimations and raw sensor measurements have been used to compare the individual raw sensor measurements in body frame with the corresponding reference models for sun position and Earth magnetic field in inertial frame. First results revealed a systematic deviation of the measurements correlating with the instantaneous attitude of the satellite, thus indicating a miscalibration of the underlying sensors despite preceding ground based calibration.

In-orbit calibration of the sensor kit has been performed in two steps. First, the orientation invariance of the magnetic field strength has been exploited in order to determine orientation, gain, and offset of the magnetometers in an arbitrary sensor frame. This has been accomplished by minimizing the summed deviation of the measured magnetic field from the corresponding IGRF-11 reference value (see figure 5.19). In a second step the summed deviation of the attitude invariant angle between sun direction and magnetic field vector has been minimized in order to derive the mounting matrices of the individual sun sensors. After calibration the attitude determination system showed expected performance with a consistency deviation close to the individual sensor noise which indicates an absolute attitude determination accuracy in the order of a few degrees. Similar performance could be identified also during fast spin experiments with spin rates up to 80 deg s^{-1}.

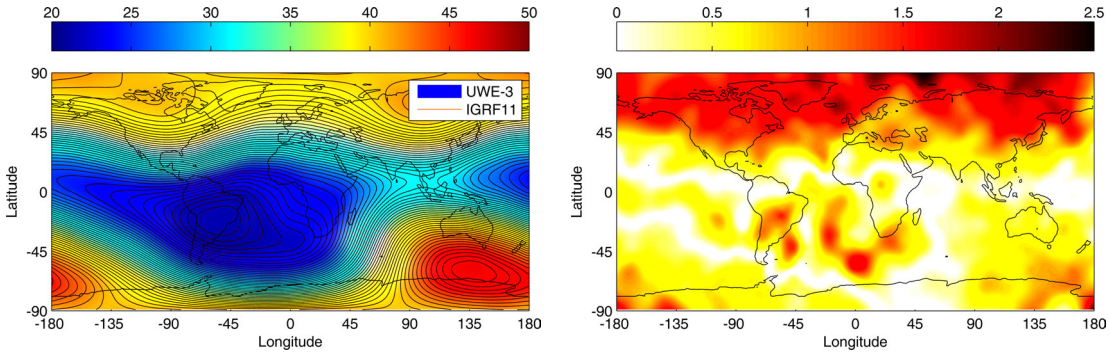


Figure 5.19: Calibrated magnetic field strength $[\mu T]$ as measured during several orbits compared to the reference model IGRF-11 as overlay (left). Relative deviation $[\%]$ of measured field strength to IGRF-11 reference.

Further investigation of the satellite's natural motion in the absence of any active attitude control revealed that the satellite's dynamics is significantly influenced by the Earth magnetic field. Figure 5.20 (left) depicts the trace of the measured magnetic field direction in body frame over several orbits. The data indicates that the satellite swings about an inherent residual magnetic dipole aligned with the satellite's negative z-axis.

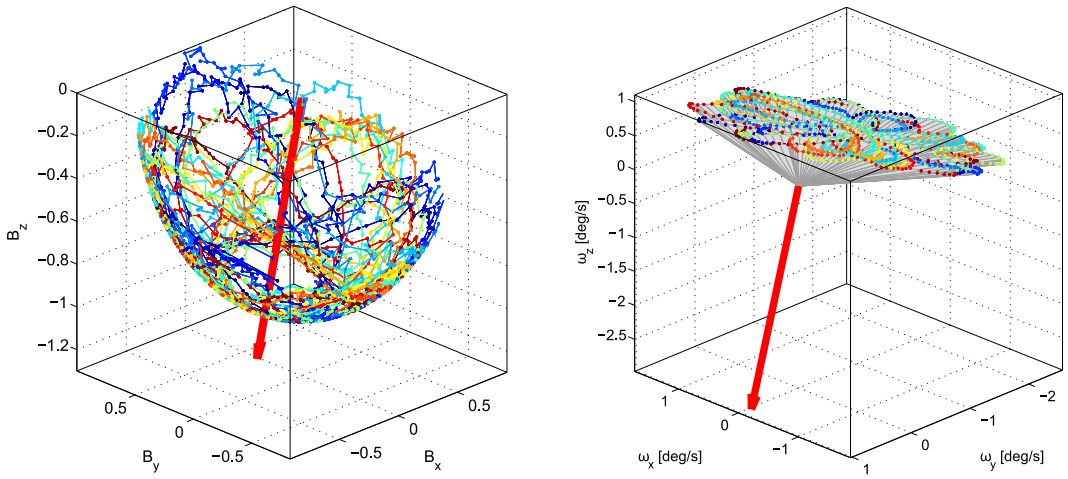


Figure 5.20: 3D trace of measured magnetic field vector (left) and rate vector (right) in body frame during several orbits, in the absence of any active attitude control. Direction of estimated residual magnetic dipole is overlaid as red arrow.

For a more detailed analysis of the satellite's natural motion a high resolution recording of the onboard rate measurements has been used to derive a numerical estimation of the external torques affecting the satellite's motion. Looking at the trace of measured rate vectors as depicted in figure 5.20 (right) it can be seen that the apparent angular acceleration is mostly aligned within a plane such that underlying torques can be well explained by a magnetic dipole aligned perpendicular to that plane. The exact orientation and strength of the residual dipole μ have been derived numerically by fitting a magnetic torque $\mu \times B$ to the Euler equations such that a large data set of rate measurements ω and magnetic field measurements B satisfies $\mu \times B \stackrel{!}{=} I\dot{\omega} + \omega \times I\omega + e$ with minimal errors e. The result describes a dipole being predominately aligned along the satellite's negative z-axis with a magnitude in the order of $0.05\,\mathrm{Am}^2$.

It could be shown that the estimated dipole can explain the major contribution of experienced torques in the absence of active control while being independent of time, instantaneous power consumption, battery charge state, and satellite illumination. In particular, extensive operations of onboard magneto-torquers could not permanently affect the measurable residual dipole. It has been concluded that magnetization of one of the satellite's redundant monopole antennas would be the most probable source of the magnetic dipole observed. However, it could be demonstrated that the onboard torquers are just capable of compensating the disturbance torque induced by the residual dipole.

In the following months work has been focusing on various magnetic control algorithms taking into account large magnetic disturbance torques such as magnetic spin control

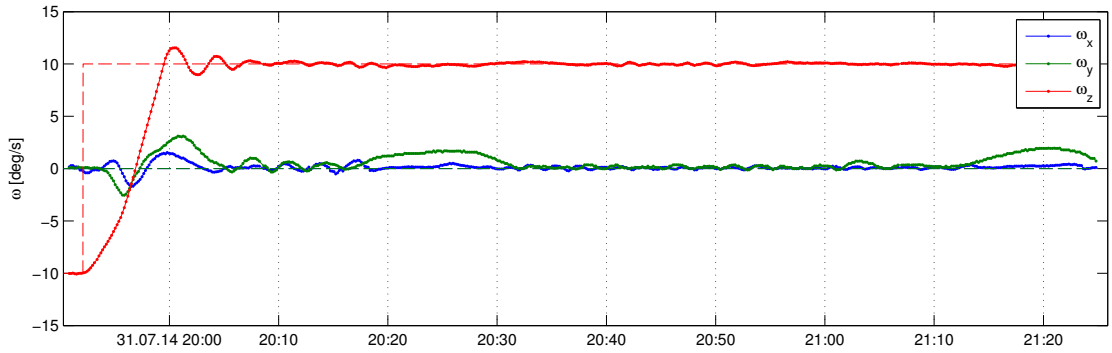


Figure 5.21: Magnetic spin control experiment demonstrating in-orbit spin axis control during a set-point transition from $-10\,\mathrm{deg\,s^{-1}}$ to $+10\,\mathrm{deg\,s^{-1}}$ about the satellite's z-axis.

experiments (see figure 5.21). In this context several software updates have been uploaded to the satellite in order to provide more flexibility for the experimental usage of the attitude control system. In particular, an efficient script interpreter has been installed on the ADCS which allows to activate arbitrary control laws which can be uplinked and executed on-the-fly in a secure sandbox environment. Thus, UWE-3 can be effectively used as a valuable testbed for experimental attitude determination and control operations which will be used in preparation for the upcoming UWE missions targeting advanced orbit and formation control.

6

Conclusions

In the last decade a clear trend towards increased utilization of miniaturized satellites could be observed. Especially the flexible and cost-efficient access to space promoted by the CubeSat standard paved the way for a magnitude of valuable educational, technical, and scientific missions. Promising concepts targeting to exploit the advantages of distributed space systems based on miniature satellites are already on the horizon. Nevertheless, limitations connected to their extremely limited resources still pose substantial challenges regarding performance and durability of single miniaturized spacecraft designs, not to mention special demands arising with the need for efficient batch manufacturing to realize larger formations.

With the goal to provide a solid base for future pico-satellite formations, this work addresses these challenges at the example of the University of Wuerzburg next generation experimental pico-satellite UWE-3. Three elementary design drivers have been identified as general approach. *Flexibility* of a modular architecture ensures that the platform can be easily reused, modified, or extended to suit future requirements. *Robustness* guarantees reliable and fault-tolerant operation by systematic design for testability together with inherent redundancy for critical subsystems. *Efficiency* promotes advanced miniaturization and can support flexibility and robustness on one hand, but often demands a thoughtful trade-off in this respect on the other hand.

The UWE-3 pico-satellite realizes a consequent implementation of envisaged aspects for the general bus architecture as well as for all subsystems designed in the context of this project. UWE-3 has been launched in late 2013 and has by now been successfully operating for more than two years in orbit. This thesis addresses the pico-satellite's modular platform in general and elaborates on the design and operational performance of the satellite's electrical power system and its onboard computer as crucial key components.

6.1 Modular Satellite Bus

Taking up the challenge to realize a modular structure for a miniaturized pico-satellite platform, the introduced satellite bus defines a generic electrical and mechanical subsystem interface in form of a pluggable backplane architecture. As a main innovation compared to related systems complying with the single unit CubeSat standard, the design avoids the need for any wired harnessing. Instead, it allows to rapidly assemble either a compact or exposed functional satellite configuration by plugging the individual modules to the satellite's backplane or a prototyper board, respectively.

The completely integrated flight demonstrator UWE-3 comfortably meets the CubeSat Design Specification with respect to geometry, weight, and mass distribution constraints. Despite its minimalistic structure, finite element analysis could prove good performance of the structural setup when exposed to launch equivalent static loads. The flight model was further successfully qualified for launch during extensive thermal-vacuum, acceleration, and vibration tests.

The design achieves efficiency in several aspects. Besides cost-efficient manufacturing of the small number of mechanical components involved, the backplane architecture allows optimized utilization of limited space available. In fact, compared to its predecessors, the UWE-3 setup comprises increased functionality, performance, and redundancy at significantly reduced consumption of mass and internal space. Thus, UWE-3 reserves more than 20 % of available mass and space, which renders the platform reusable for future extensions. Flexibility could further be demonstrated during the design process, when individual subsystems were concurrently developed and re-designed in several iterations over the course of the project, whereas the standardized interface could significantly reduce dependencies and incompatibilities. In particular, the concept could demonstrate to enhance testability for several reasons. On one hand, introduced electrical and mechanical interface definitions facilitated debugging of electronics and embedded software. In this regard, the platform effectively promoted early integration functional testing due to simple and rapid assembly of test configurations which allow comfortable access to relevant test signals. On the other hand, defined software libraries and protocols proved beneficial for rapid implementation and execution of automated test procedures and could effectively reduce the engineer's workload during elaborate long term functional tests and costly qualification test campaigns.

Overall, the modular and flexible bus architecture is seen as one of the major key components responsible for the success of the UWE-3 mission regarding the satellite's reliable operation in orbit, but also in terms of the project's educational value. However,

it has to be clear that qualities such as flexibility and robustness are difficult to measure and can hardly be assessed in a single mission only. Instead, these qualities have to prove themselves in the future when successor projects can benefit from re-usage and support for extension. Despite specific advantages addressed in the context of the UWE mission, the platform might not be optimal for all kind of missions and applications of small satellites. Some designs might require different signals on the backplane such as higher voltages or high speed data buses. Other concepts might require mechanical and electrical support for commercial subsystems. Thus, being optimized for specific requirements targeting the UWE project series, the presented platform can clearly not fulfill all requirements for a comprehensive standard for small satellites.

Nevertheless, some aspects regarding flexibility and robustness might contribute to an ongoing standardization processes for miniature satellite buses. In this respect the bus definition already convinced UNISEC Europe and entered the definition process of future ISO and IAA standards.

6.2 Electrical Power System

As a major challenge for an electrical power system, targeting the UWE-3 platform, the implementation has to provide performant and robust power generation, storage, conversion, and distribution within the framework of the modular and flexible design paradigm of the miniature satellite bus. In contrast to available power systems for pico- and nano-satellites presented, this work introduced a partially distributed modular and redundant design. In this way, the concept enables the power system to suit different satellite configurations and future mission scenarios while providing a reasonable level of robustness for its crucial service.

Flexibility of the proposed concept could be achieved by spatial separation of functional blocks, relocating the implementation for peak power tracking close to the solar cells on the multifunctional side panels whereas the power distribution circuitry became a part of the corresponding subsystem module. As a result, the system's performance can scale with quantity and requirements of power generators and consumers, while keeping the number of power lines on the backplane constant. Robustness was addressed by the systematic implementation of two redundant power paths allowing both, parallel and exclusive operation. Further fault-tolerance arises from the parallel implementation of power generators and converters in each path, providing combined performance with graceful degradation.

Comprehensive load tests have been carried out on the engineering model to charac-

terize the system's performance within its specified operating range. In particular, the redundant power paths could be verified in single chain and combined operation for up to 10 W load, which represents more than 5 times the orbit average power of a typical pico-satellite mission. Effective path efficiencies and natural load distribution could be characterized experimentally, showing reliable operation of the redundancy concept at acceptable performance within the entire operating range. Thermal imaging experiments could further demonstrate the converter cluster's effectiveness regarding load sharing and spatial distribution of heat dissipation.

The flight-model implementation proved expected performance during extensive thermal and mechanical qualification tests. In particular, the results could indicate that the mechanical assembly provides sufficient fixation of the batteries while its excellent thermal insulation avoids the need for heater activation during operation in orbit. This could also be confirmed in the course of UWE-3 operations as observed battery temperatures remained securely positive despite minor seasonal variations. Further long-term in-orbit performance tests could demonstrate stable provision of 1.1 W orbit average power, which leaves more than 70 % verified margin in the satellite's nominal power budget for energy demanding experiments. Nevertheless, provision of higher orbit average power might be possible in low Earth orbit such that further experiments and optimizations are expedient.

Despite particular advantages coming along with the electrical power system's distributed architecture, these benefits are clearly limited to the utilization on the UWE platform as the design is strongly connected to the modular satellite bus definition. The independent utilization on a different platform would require to implement a fixed number of peak power trackers and power distribution units on a separate central board, thus giving up flexibility and adding electrical harness. Another limitation of the presented implementation arises from its comparatively low unregulated bus voltage. Being optimized for the requirements of a single unit pico-satellite, larger platforms such as triple unit CubeSats might benefit from higher bus voltages which would require slight modifications on power generation, storage and conversion hardware.

However, the electrical power system could demonstrate very good performance on the UWE-3 satellite from the first day of operations. No significant degradations or malfunctions could be observed after more than 5000 orbital cycles during the satellite's first year in orbit and beyond.

6.3 Onboard Computer

Urging robustness and efficiency in the presence of significant threats for microelectronics operated in the hazardous space environment, the UWE-3 design paradigm assigns a challenging role to the satellite's onboard computer. As one of its essential services, the central module has to identify severe fault states within the spacecraft, in order to re-establish operations by automatic initiation of adequate recovery procedures for particular subsystems, including itself. With the unique characteristic to combine low power processing performance in a warm-backup scheme, the UWE-3 onboard data handling core module fills a gap in the list of existing onboard computers for pico-satellites.

Being optimized for housekeeping and basic data management on the pico-satellite platform the core module design relies solely on energy-efficient state-of-the-art technology. Thus, with less than 10 mW nominal power consumption the hardware implementation requires ten times less energy than the majority of available onboard computers for small satellites. Despite advances in energy-efficiency, the core module realizes hardware and software supported fault-tolerance mechanisms. In particular, a redundant processing unit architecture with hardware controlled master-slave topology enables automatic redundancy selection with special support for mutual assistance. Thus, the design allows runtime-efficient error detection and recovery for mutual program memory protection up to complete mutual reconfiguration in the context of fail-save in-orbit software updates.

Software implemented fault injection tests have been conducted on the engineering model as a cost-efficient alternative to extensive radiation tests in order to verify the system's fault-tolerance to memory upsets. The core module could demonstrate robustness against more than one million bit errors injected to its addressable memory space during long-term validation tests prior to launch. During its first year of operation in low Earth orbit several fault events such as prompt resets, system hangs, or latchups were observed and automatically recovered on the UWE-3 flight model. An acceptable SEU rate in the order of $10^{-6}\,\mathrm{bit}^{-1}\mathrm{day}^{-1}$ was determined experimentally for the processing unit's RAM. No data corruption in 512 kB flash ROM could be identified within one year in orbit. The majority of observed events were triggered inside orbital regions exposed to trapped particle radiation whereas no significance for a time correlation with solar activity is seen in general.

Despite robustness in terms of hardware controlled recovery from severe fault states to guarantee basic operation and stable accessibility from the ground segment, prompt resets and momentary system hangs can never be avoided in non-hardened hardware. Advances in FRAM technology can provide further mitigation for the new generation

of commercial low power microcontrollers. Nevertheless, critical software tasks need to implement appropriate measures such as redundant calculations or rapid state recovery in order to ensure data integrity and task continuity after automatic fail-over events. Further limitations of the discussed system come along with the requirements for extreme energy efficiency, which in turn limits processing power and memory capacity due to ultra low power microcontrollers used. The present implementation provides sufficient performance for UWE-3 operations and basic data management. Nevertheless, future applications might require high frequency data sampling or complex preprocessing algorithms such as image processing payloads. Such demanding subsystems have to implement dedicated processing units to be operated when required and powered off when idle to save energy.

Overall, the UWE-3 onboard computer proved excellent performance in general from the first day of satellite operations in orbit. It could significantly contribute to mission success, not least because of its support for fail-safe software updates which allowed to extend operations by evaluation of continuative experiments and in-orbit validation of novel software concepts for future missions.

6.4 Future Work

Flexible and cost-efficient miniature satellite platforms are advancing fast in the field of educational, technical and scientific space missions. In this progress, continuing miniaturization will remain inevitable to continue performance and functionality enhancement while adhering to specific constraints connected to miniature spacecraft designs. Besides promising mission concepts targeting pico-satellite formations in low Earth orbit, future mission scenarios already envisage small satellites to leave Earth orbits. Being a pioneer in this field, the INSPIRE project funded by NASA intends to launch a nano-satellite in Earth-escape orbit in the next few years. As a precursor to future inclusion on interplanetary missions the project has the primary objective to demonstrate the fundamental functionality of small satellite technology in deep space. Similarly, in 2020 the ESA Asteroid Impact Mission (AIM) intends to transport several pico- or nano-satellites to the paired Didymos asteroids with the aim to complement the main spacecraft's scientific return.

This trend makes clear that especially energy-efficiency and robustness of miniature spacecraft technology will remain crucial factors for future research. In particular, topics related to fault-tolerant commercial of-the-shelf designs, long range and inter-satellite communication, advanced onboard autonomy, miniature propulsion systems and low thrust control, high precision attitude determination and control as well as miniaturized scientific instrumentation will drive future advances in the field of small satellites. Apart

from specific enabling technologies also further standardization of electrical and protocol interfaces for small satellite components and subsystems will constitute a significant endeavor for the industrial and academic community in the upcoming years.

In the context of the UWE project series future work will address enabling technologies for the realization of small satellite formations. In particular, efforts will focus on inter-satellite communications and low thrust orbit control for autonomous formation management as well as on precise attitude determination and control to support coordinated observations. In this regard, ongoing research investigates the integration of low thrust propulsion systems in the modular and flexible satellite platform. The demonstrator mission UWE-4 is planned to be launched in the next two years.

Beside general optimizations regarding energy, mass and space efficiency, several advancements are envisaged for the UWE satellite bus itself. In particular, continuative standardization for inter-subsystem communication should further enhance generic data access and generic testing. A design iteration on the standard subsystem interface might include additional redundant high speed communication, for example driven by multipoint low voltage differential signaling, to support future applications.

Particular innovation potential is seen in the extension of the platform's multifunctional side panels. Current studies address the possibilities for compact integration of state-of-the-art miniature imaging sensors and adequate low power processing units to replace the sun sensors for onboard navigation and visual verification. In addition, the integration of phase controlled small scale high frequency antennas on all side panels promises great potential for efficient inter-satellite communication in larger formations.

Further intended innovations will solely concern software of space and ground segment and can easily be tested in operation onboard UWE-3. As an example in the field of advanced onboard autonomy, an efficient binary code interpreter has been recently installed on the satellite's onboard computer in the course of a planned onboard software update. Providing generic data and control access to compact precompiled operation scripts running in a secure sandbox environment the system aims to support flexible and robust onboard autonomy for future satellite operations. In this regard, UWE-3 will remain a valuable tool for robust, flexible and efficient in-orbit validation in the context of future research and development for small satellite missions.

Appendix

A

Modular Satellite Bus

A.1 Subsystem Interface

This section presents relevant details of the electrical interface definition for the modular platform described in section 2.4.1. The modular interface design is centered on a backplane interfacing individual modules to a generic power and data bus via different connector types.

The mechanical layout of the backplane is typically adapted to the specific satellite configuration in order to allow desired spatial distribution and especially very compact placement of the subsystems inside the satellite. In addition, the backplane implements a redundant set of deployment switches (kill switches) according to CDS 2.3.2 while the front access board implements a backplane extension to provide umbilical line connectors (CDS 2.3.3) and redundant remove-before-flight switches (CDS 2.3.4). The umbilical line is divided in an analog interface for test activation and battery maintenance and a digital interface for software flashing, test and in-system debugging of the onboard computer.

The power bus incorporates redundant unregulated battery buses and several controlled regulated power buses for different voltages and functions. Dedicated redundant control signals allow to manage global high and low side switches in the power path for satellite (de-)activation before launch (CDS 2.3.2 and 2.3.4) and controlled power cycles after activation in orbit.

The data bus provides various signal lines for general subsystem control and communication such as redundant bidirectional communication buses, a subsystem programming interface, global reset and time synchronization. Crucial subsystems such as radio communication and electrical power have dedicated control and communication lines. Further dedicated signal lines allow programming, in-system-debugging, test and checkout of the onboard computer after integration via the satellite's umbilical line.

An overview of the individual interface connectors is provided in figure A.1 whereas detailed pin layouts for the subsystem board interface, the panel interface, and the umbilical line are depicted in figure A.2, A.3, A.4, and A.5 respectively. Individual signal descriptions of the power and data bus are provided in figure A.6 and A.7.

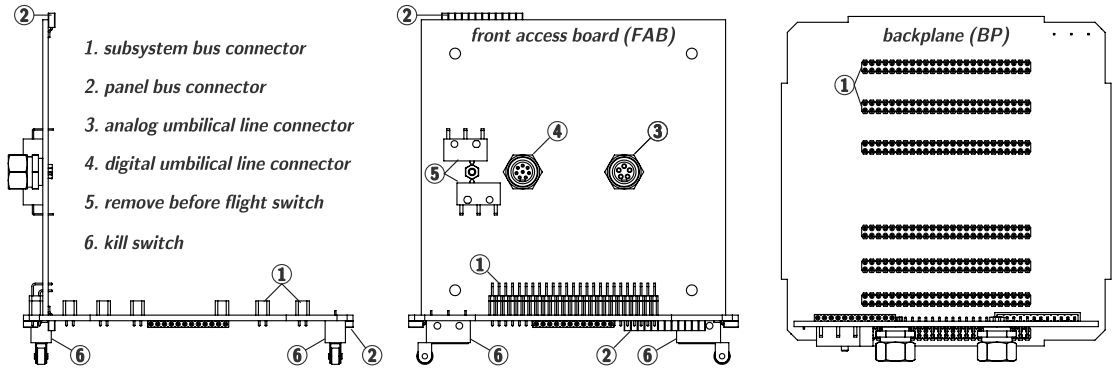


Figure A.1: Interface connectors of the power and data bus on the satellites backplane.

UML_UART (RXD)	1	2	UML_UART (TXD)
UML_SBW-1 (TDIO)	3	4	UML_SBW-1 (TCK)
UML_SBW-2 (TDIO)	5	6	UML_SBW-2 (TCK)
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
BUS_JTAG (TDI)	9	10	BUS_JTAG (TCK)
BUS_JTAG (TDO)	11	12	BUS_JTAG (TMS)
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
CTL_RESET	17	18	CTL_RESET
COM_UART-1 (RXD)	19	20	BUS_I2C-2 (SDA)
COM_UART-1 (TXD)	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-2	27	28	PWR_BAT-2
PWR_BAT-1	29	30	PWR_BAT-1
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	CTL_SYNC
GND_ROOT	35	36	GND_ROOT
GND_CTL-1	37	38	GND_CTL-2
SUP_BACKUP	39	40	SUP_BACKUP
SUP_CTL-1	41	42	SUP_CTL-2
General Purpose Input/Output	43	44	COM_IRQ
General Purpose Input/Output	45	46	General Purpose Input/Output
COM_UART-2 (TXD)	47	48	General Purpose Input/Output
COM_UART-2 (RXD)	49	50	General Purpose Input/Output

Figure A.2: Subsystem bus connector (1).

GND_SYSTEM	1
SUP_5V0	2
CTL_RESET	3
BUS_I2C-2 (SDA)	4
BUS_I2C-2 (SCL)	5
SUP_UNREG	6
SUP_3V3	7
PWR_BAT-2	8
PWR_BAT-1	9
reserved (PWR_SC)	10
CTL_SYNC	11
GND_ROOT	12

Figure A.3: Panel bus connector (2).

GND_SYSTEM	1
GND_CTL-1	2
GND_ROOT	3
PWR_BAT-1	4
PWR_BAT-2	5

Figure A.4: Analog umbilical line connector (3).

GND_SYSTEM	1
UML_UART (RXD)	2
UML_UART (TXD)	3
UML_SBW-1 (TDIO)	4
UML_SBW-1 (TCK)	5
UML_SBW-2 (TDIO)	6
UML_SBW-2 (TCK)	7

Figure A.5: Digital umbilical line connector (4).

System Ground and Global Deactivation Low-Side Switch	
GND_ROOT	Ground potential of power generating or storing devices. To be disconnected from GND_SYSTEM for storage and launch to comply with CDS 2.3.1, 2.3.2, 2.3.2.1, and 2.3.4.2. Subsystems must use GND_SYSTEM.
GND_SYSTEM	Global ground potential to be used by subsystems. Signal is floating during storage and launch.
GND_CTL-1	Redundant digital signals to control redundant ground bridge switches connecting GND_ROOT with GND_SYSTEM for testing and after satellite deployment. Signals driven by *Remove Before Flight Pin* and *Kill Switch* circitury accroding to CDS 2.3.2 and 2.3.4.
GND_CTL-2	

Power Path Source	
PWR_BAT-1	Direct access to redundant unregulated power buses for battery maintenance via umbilical line. Can be directly supplied by distributed peak power tracker on side panels. See 3.2 for detailed information.
PWR_BAT-2	
PWR_SC_X	Optional: Input for 3 central independent peak power tracking units. To be supplied by the solar panels.
PWR_SC_Y	
PWR_SC_Z	

Power Supply Buses	
SUP_3V3	3.3V common regulated bus combining both redundant power paths.
SUP_5V0	5.0V common regulated bus combining both redundant power paths.
SUP_UNREG	Common unregulated bus combining both redundant power paths.
SUP_BACKUP	Common unregulated bus (backup) combining both redundant power paths. Bus bypasses master switches of redundant power paths and is not affected during intentional power cycles initiated by asserting SUP_CTL-1 and SUP_CTL-1 simultaneously.
SUP_CTL-1	Redundant watchdog supervised digital control signals for individual deactivation of redundant power paths for maintenance or power cycles. Periodic signal change deactivates corresponding paths contributing to SUP_3V3, SUP_5V0, and SUP_UNREG. Simultaneous assertion initiates power cycle. For power path switch over simultaneous path activation has to be assured during transition. To be controlled by the OBC.
SUP_CTL-2	

Figure A.6: Signal description of the power bus.

General Subsystem Control	
BUS_I2C-1 (SDA)	Redundant I^2C interfaces for bidirectional data exchange among subsystems or direct access to remote I^2C devices (i.e. power monitors, temperature sensors). Subsystems might use the buses in multi-master mode for reception (subsystem is slave as default) and transmission (subsystem becomes master when required).
BUS_I2C-1 (SCL)	
BUS_I2C-2 (SDA)	
BUS_I2C-2 (SCL)	
BUS_JTAG (TDI)	Shared JTAG interface for subsystem software update via OBC. At maximum one JTAG device can be connected to the bus interface at a time. Per default the interface has to be disconnected by the standard subsystem interface control circuit.
BUS_JTAG (TDO)	
BUS_JTAG (TCK)	
BUS_JTAG (TMS)	
CTL_RESET	Global not-reset signal (low-active) driven by the OBC (default high).
CTL_SYNC	Global synchronization signal, driven by the OBC.
GPIO	General Purpose Input/Output Lines: UWE-3 OBC provides general purpose input/output lines with optional analog-digital converters or signal interrupt inputs for specific applications.
GPIO	
GPIO	
GPIO	
GPIO	

Special Subsystem Control: OBC Debug & Test Interface for Umbilical Line	
UML_UART (RXD)	Serial interface of the OBC for test and debug purpose during development, integration, test and checkout. Inactive in flight mode. Available on the digital interface of the umbilical line for checkout tests after integration in launch adapter.
UML_UART (TXD)	
UML_SBW-1 (TCK)	Spy-By-Wire interface for programming and in-system-debugging of the redundant OBC. Available on the digital interface of the umbilical line for software updates after integration in launch adapter.
UML_SBW-1 (TDIO)	
UML_SBW-2 (TCK)	
UML_SBW-2 (TDIO)	

Special Subsystem Control: Communication	
COM_UART-1 (RXD)	Redundant serial interfaces for dedicated one-2-one communication with the redundant radio communication subsystem.
COM_UART-1 (TXD)	
COM_UART-2 (RXD)	
COM_UART-2 (TXD)	
COM_IRQ	Dedicated interrupt request from redundant radio communication subsystem to indicate incoming frame.

Figure A.7: Signal description of the data bus.

A.2 Static Acceleration Analysis

This section provides the detailed result set from static acceleration analysis as described in section 2.6.1. Analysis has been conducted on a reduced CAD model (see figure A.8).

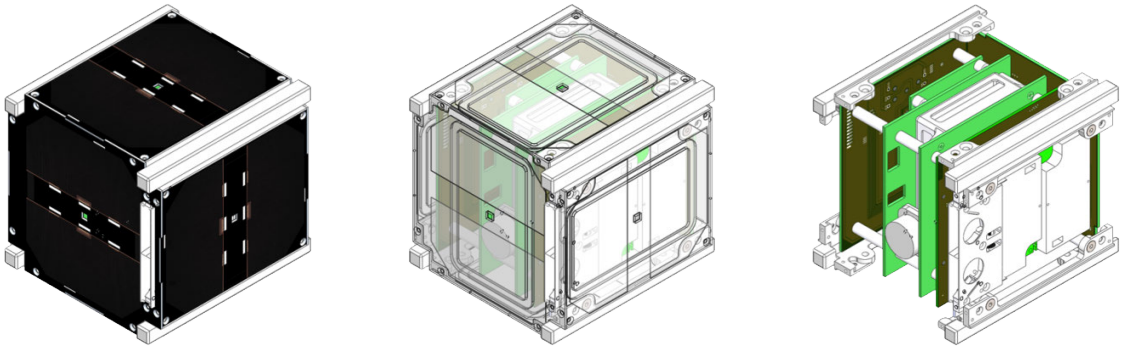


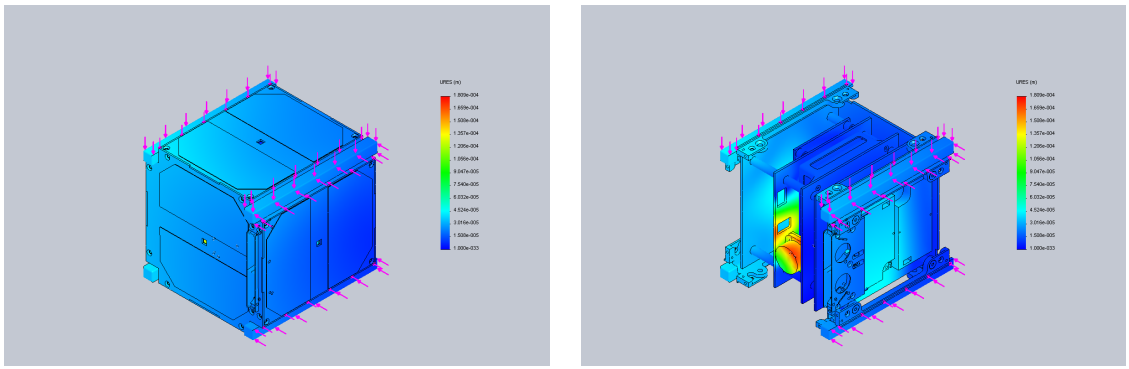
Figure A.8: Reduced CAD model used for static acceleration analysis

In 24 separate simulation scenarios static loads in terms of combined longitudinal acceleration (10.5 g) and transversal acceleration (3.4 g) have been applied to the satellite's corresponding structural interfaces for all possible orientations of the launch adapter in the launcher. Results are provided in form of relative node displacements of the accelerated rigid body. The relative node displacements for the individual scenarios are depicted in figures A.9 to A.14 and are summarized in table A.1.

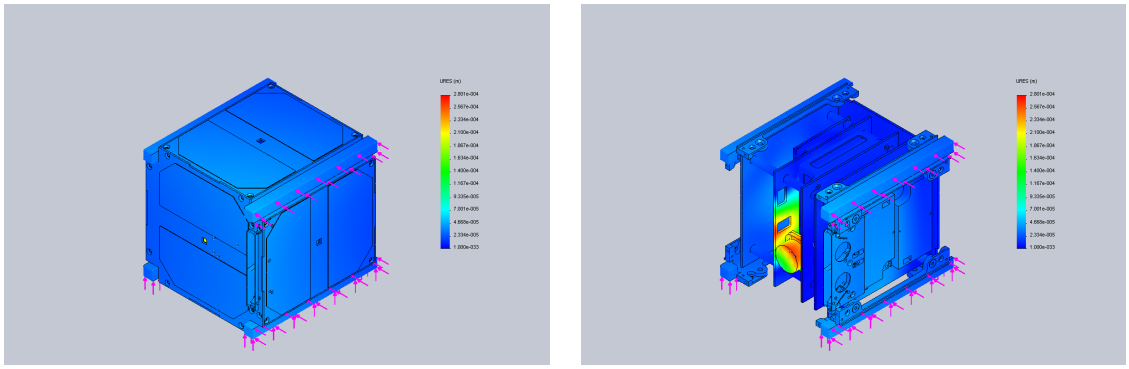
Longitudinal Axis: axis load 10.5 g	Transversal Axis: axis load 3.4 g	Maximum Displacement [m]
−X	−Y	0.000180949
	+Y	0.000280050
	−Z	0.000213652
	+Z	0.000278582
+X	−Y	0.000242318
	+Y	0.000180225
	−Z	0.000263843
	+Z	0.000221204
−Y	−X	0.000086855
	+X	0.000228103
	−Z	0.000213485
	+Z	0.000128198
+Y	−X	0.000226643
	+X	0.000086551
	−Z	0.000166234
	+Z	0.000199816
−Z	−X	0.000242958
	+X	0.000280381
	−Y	0.000273940
	+Y	0.000256355
+Z	−X	0.000304696
	+X	0.000192509
	−Y	0.000268140
	+Y	0.000311269

Table A.1: Maximum node displacements for all combinations of longitudinal and transversal static loads applied to the individual satellite axes (see also figures A.9 to A.14).

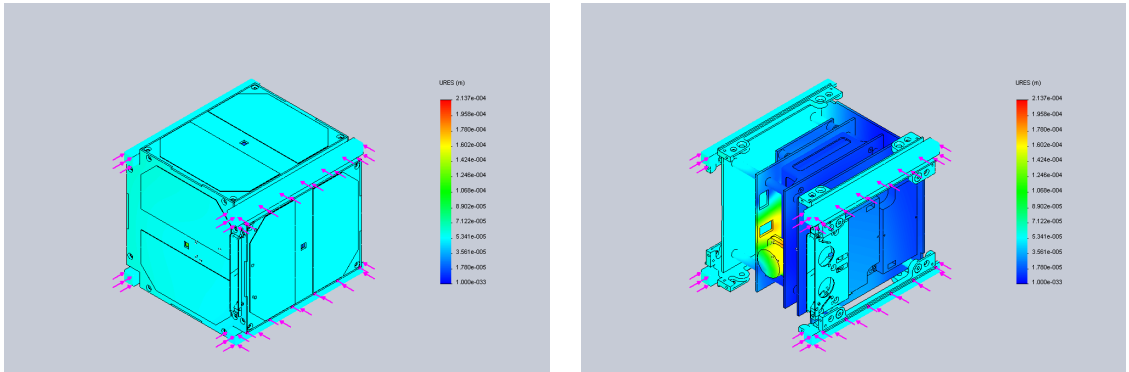
Longitudinal Axis: −X, Transversal Axis: −Y



Longitudinal Axis: −X, Transversal Axis: +Y



Longitudinal Axis: −X, Transversal Axis: −Z



Longitudinal Axis: −X, Transversal Axis: +Z

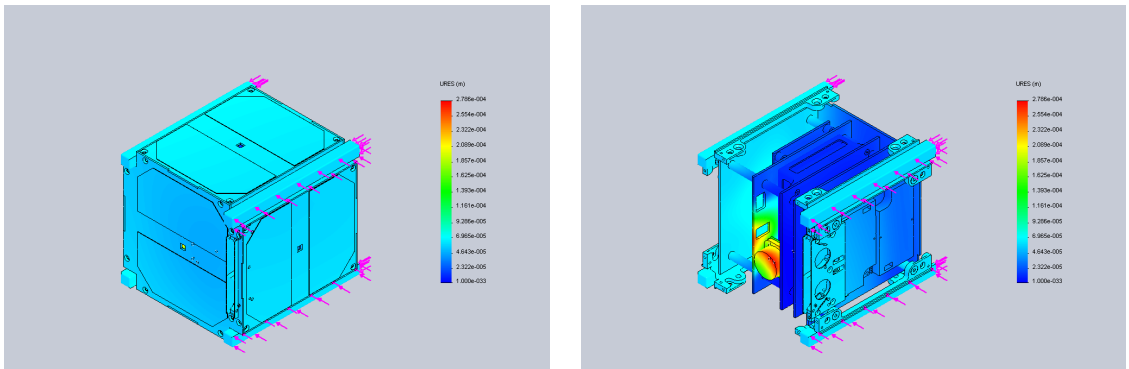
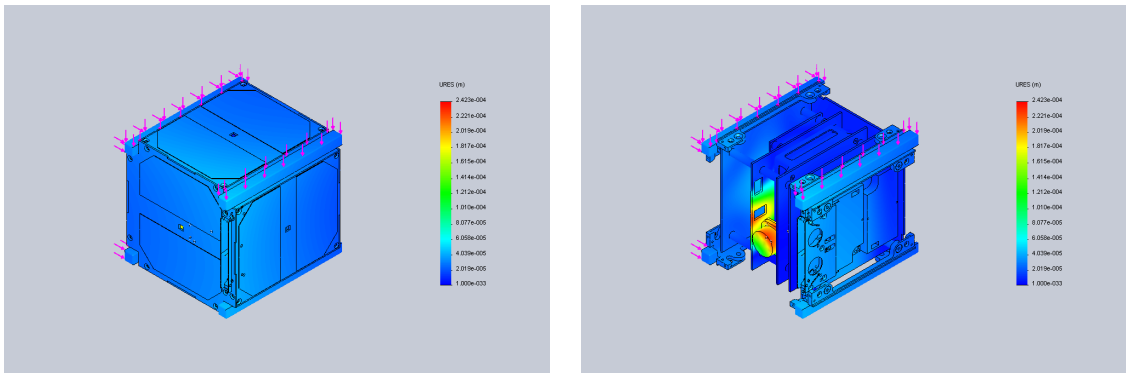
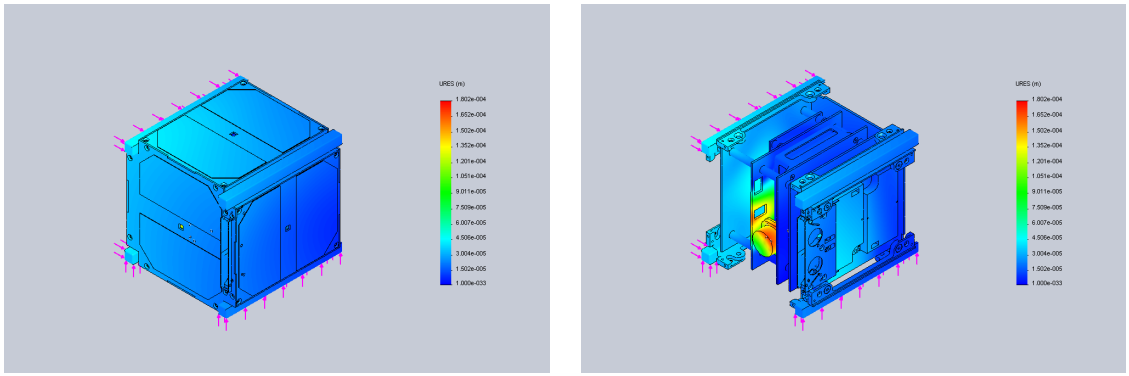


Figure A.9: Longitudinal Axis: −X

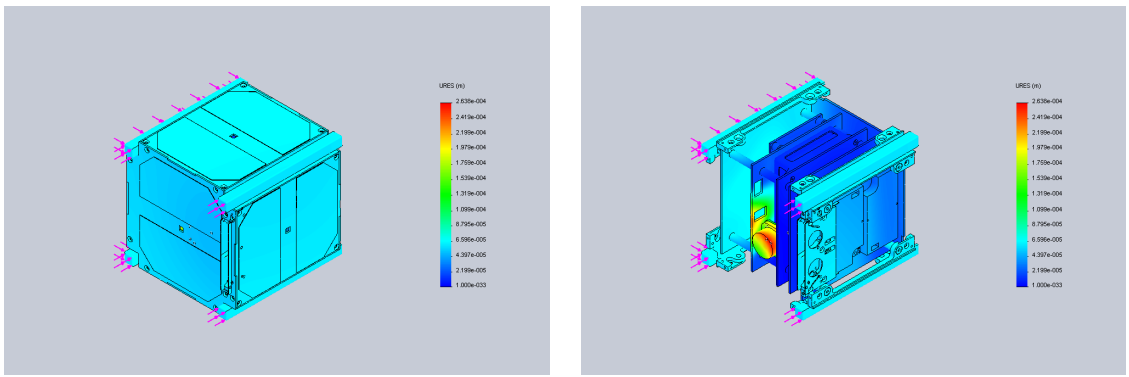
Longitudinal Axis: +X, Transversal Axis: −Y



Longitudinal Axis: +X, Transversal Axis: +Y



Longitudinal Axis: +X, Transversal Axis: −Z



Longitudinal Axis: +X, Transversal Axis: +Z

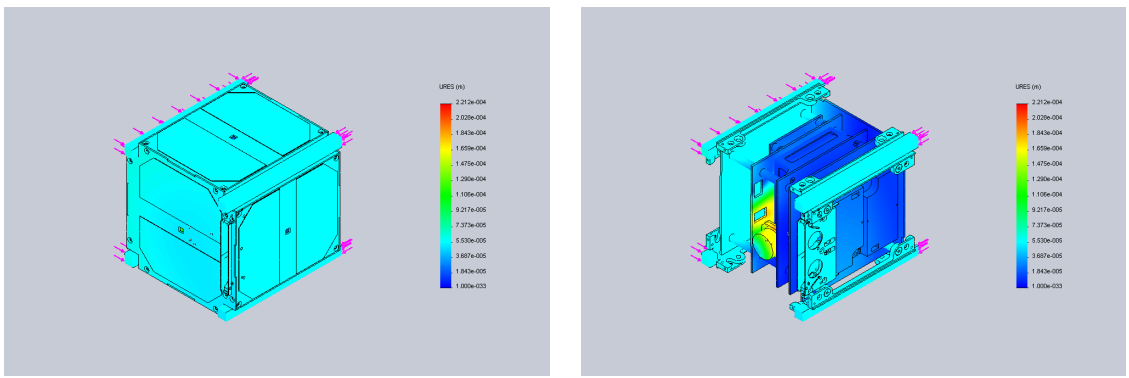
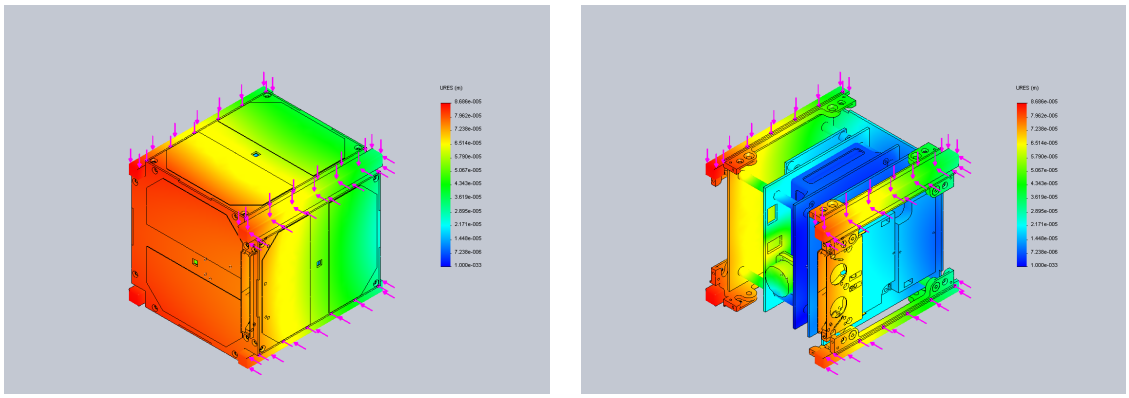
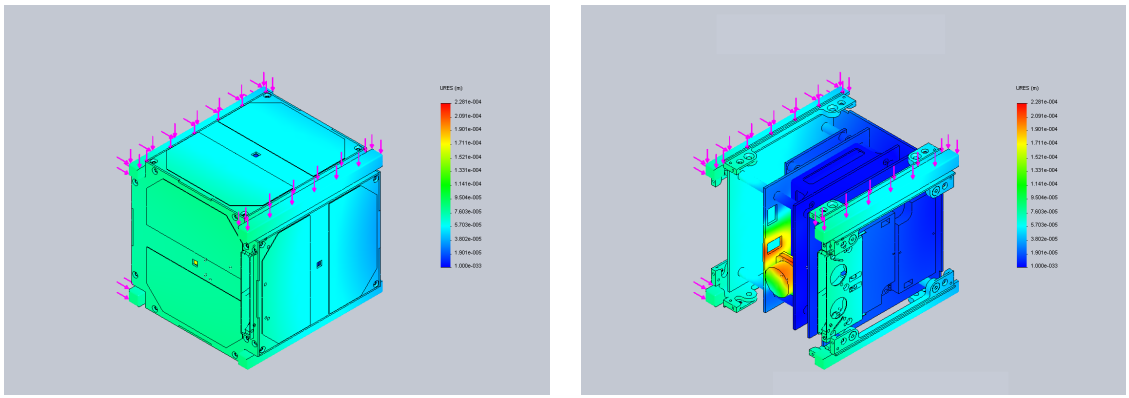


Figure A.10: Longitudinal Axis: +X

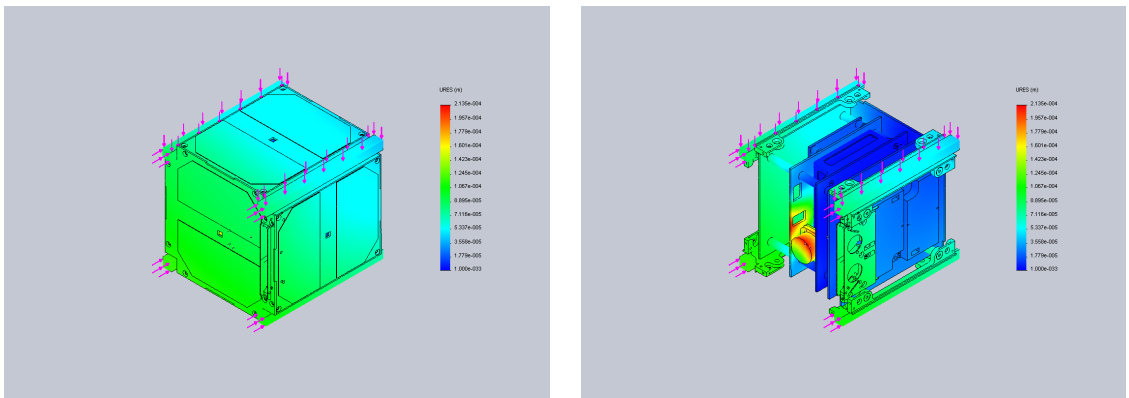
Longitudinal Axis: −Y, Transversal Axis: −X



Longitudinal Axis: −Y, Transversal Axis: +X



Longitudinal Axis: −Y, Transversal Axis: −Z



Longitudinal Axis: −Y, Transversal Axis: +Z

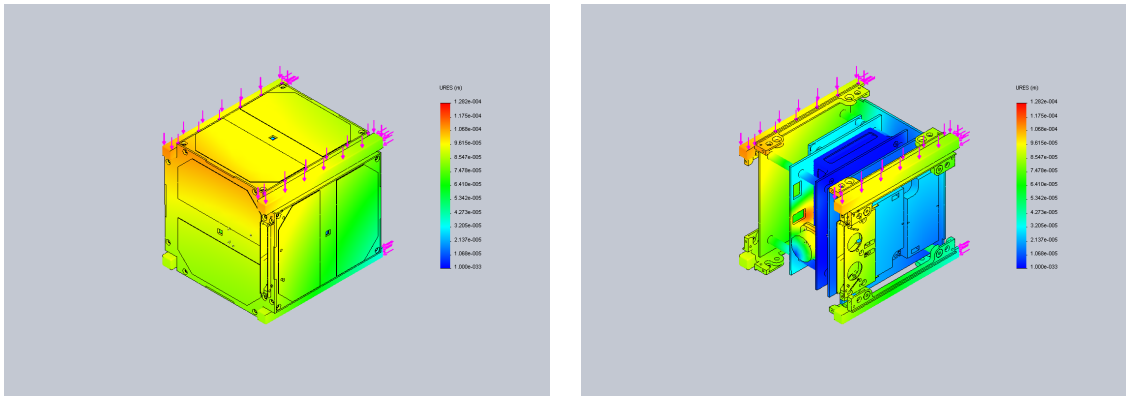
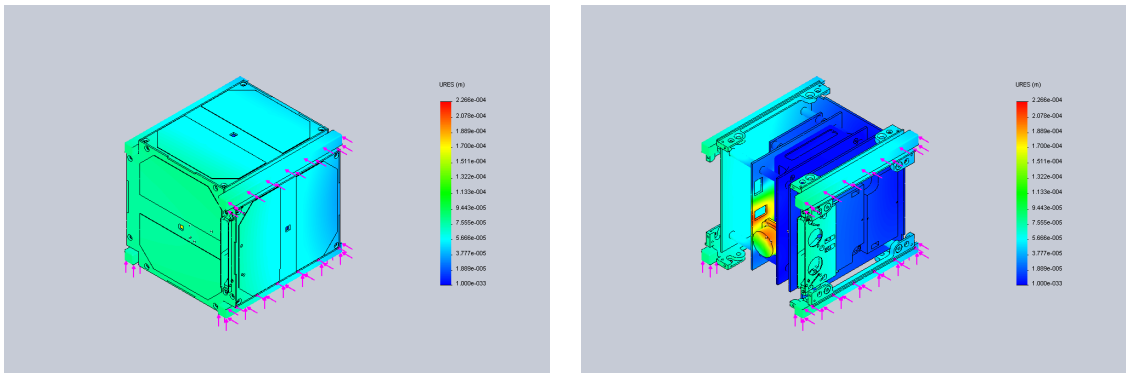
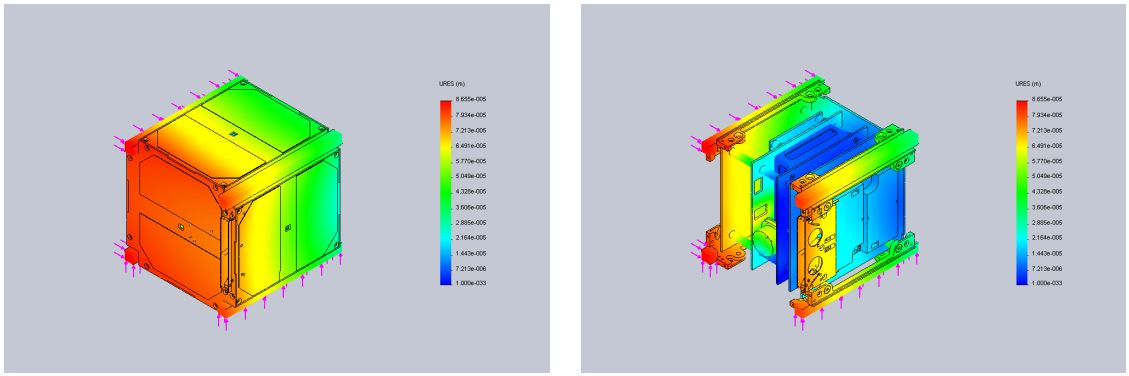


Figure A.11: Longitudinal Axis: −Y

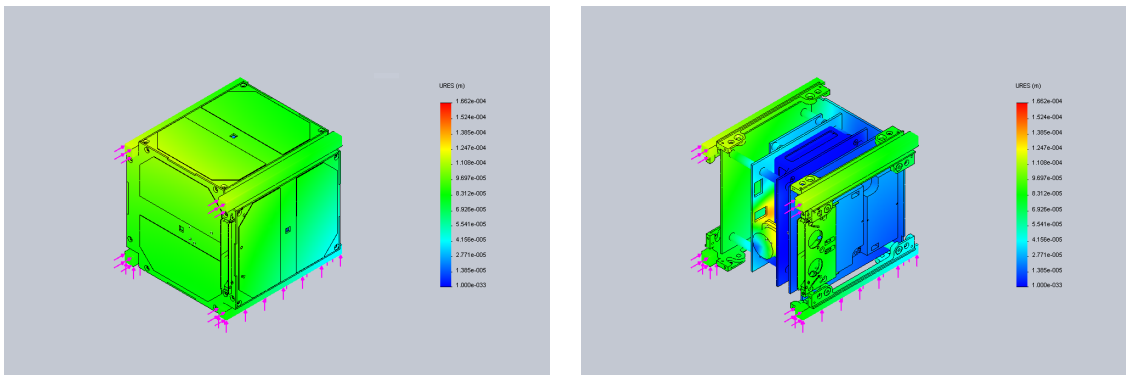
Longitudinal Axis: +Y, Transversal Axis: −X



Longitudinal Axis: +Y, Transversal Axis: +X



Longitudinal Axis: +Y, Transversal Axis: −Z



Longitudinal Axis: +Y, Transversal Axis: +Z

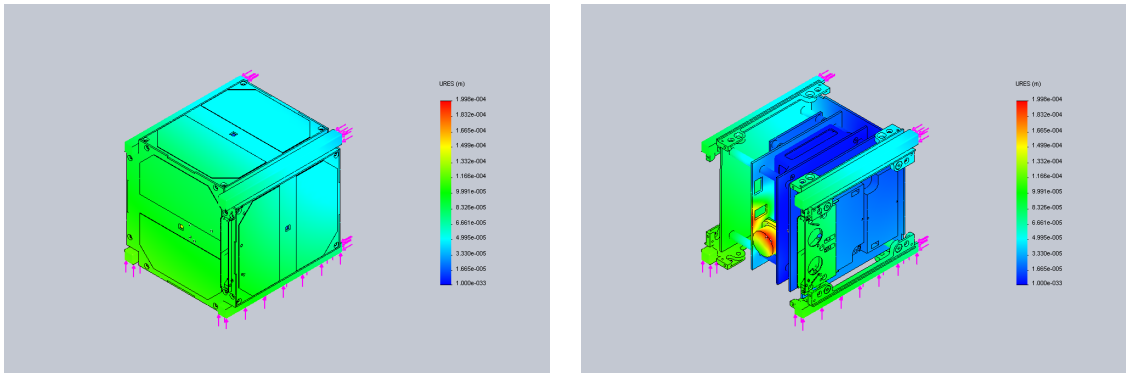
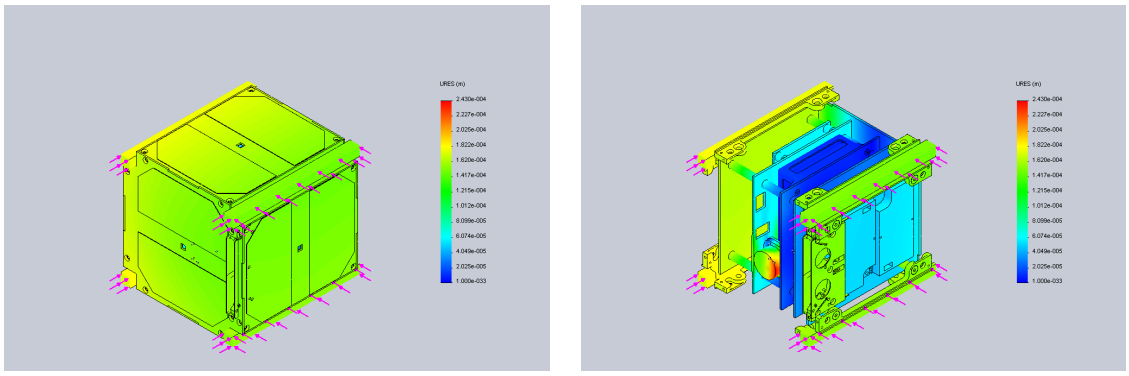
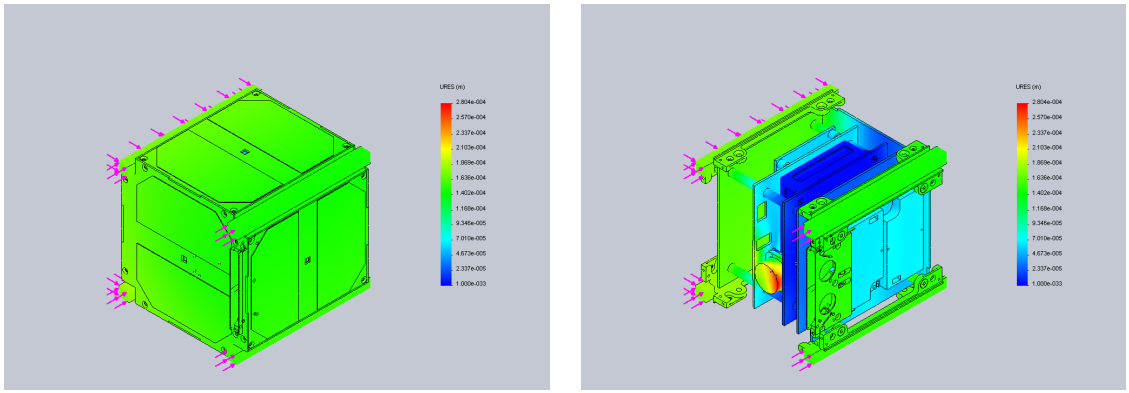


Figure A.12: Longitudinal Axis: +Y

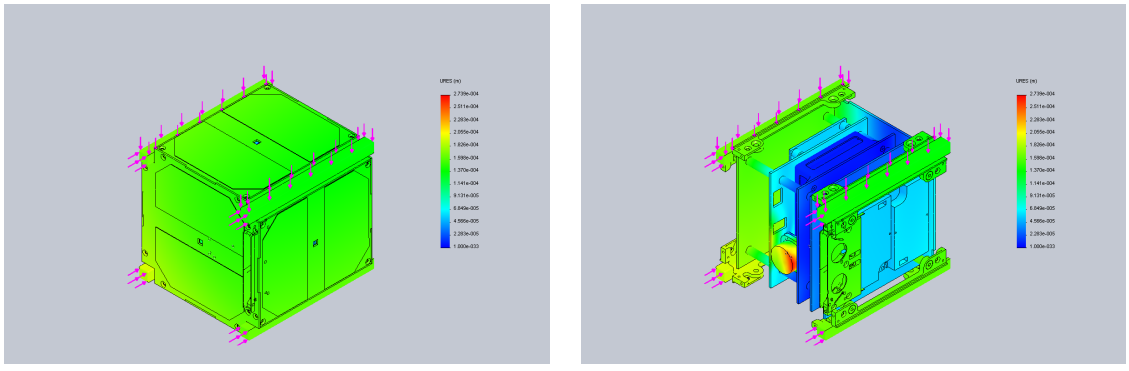
Longitudinal Axis: −Z, Transversal Axis: −X



Longitudinal Axis: −Z, Transversal Axis: +X



Longitudinal Axis: −Z, Transversal Axis: −Y



Longitudinal Axis: −Z, Transversal Axis: +Y

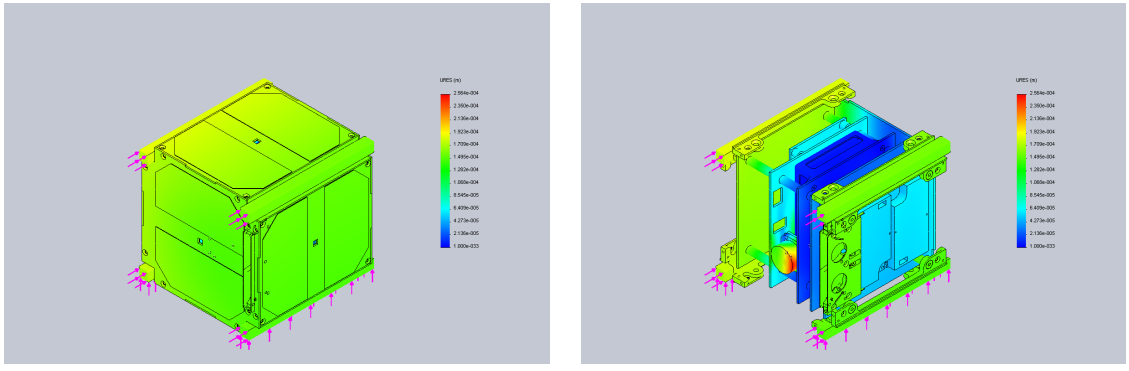
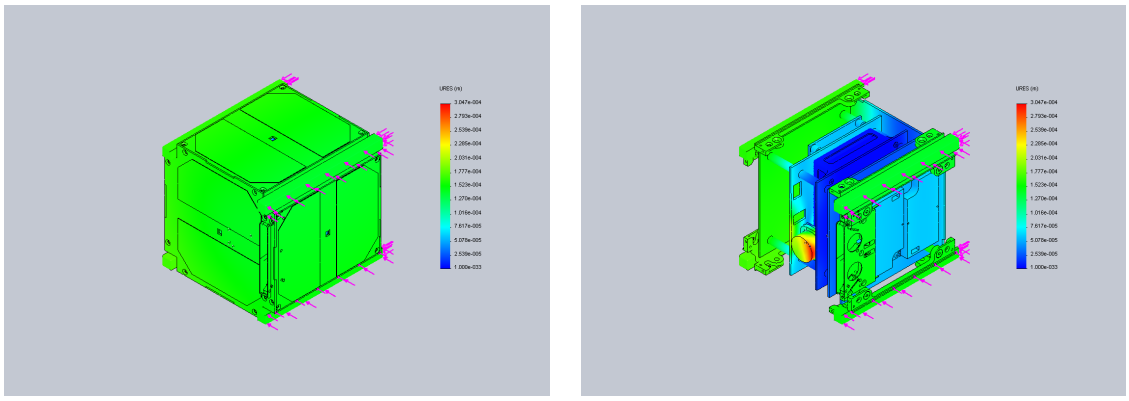
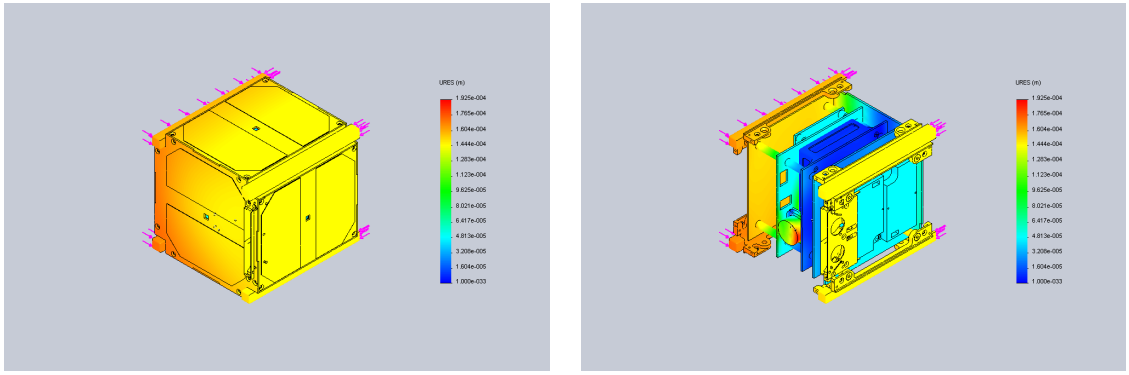


Figure A.13: Longitudinal Axis: −Z

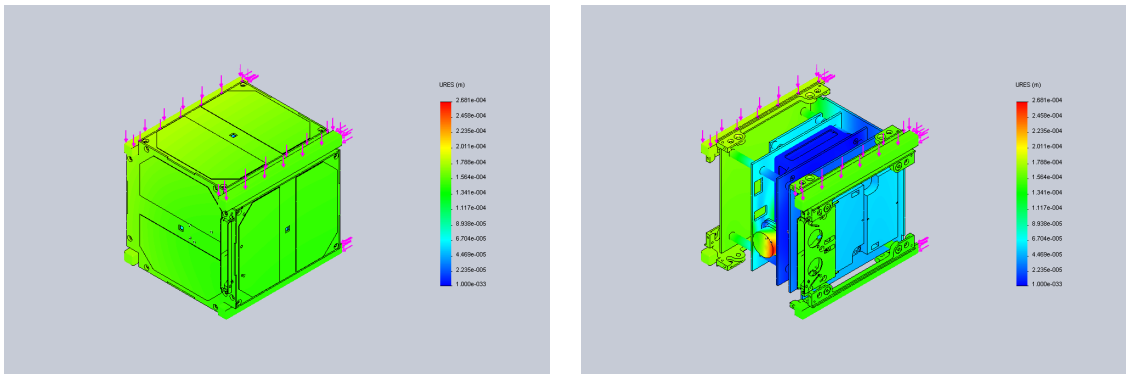
Longitudinal Axis: +Z, Transversal Axis: −X



Longitudinal Axis: +Z, Transversal Axis: +X



Longitudinal Axis: +Z, Transversal Axis: −Y



Longitudinal Axis: +Z, Transversal Axis: +Y

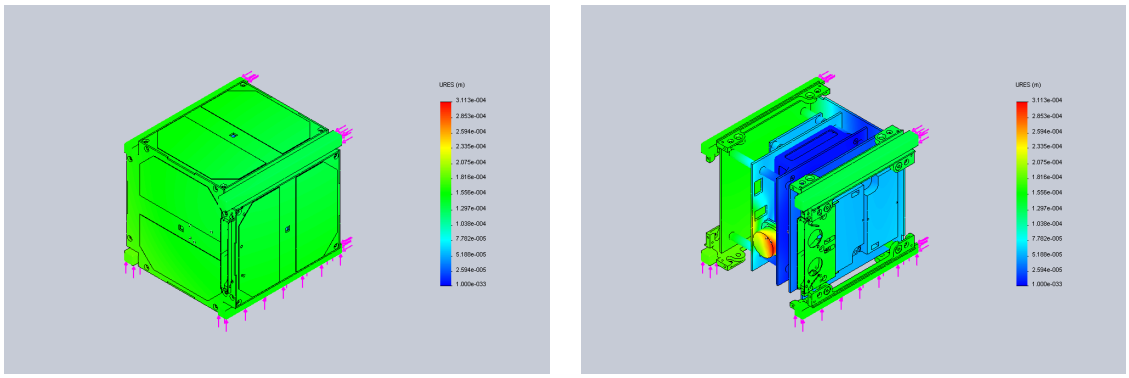


Figure A.14: Longitudinal Axis: +Z

B

Onboard Computer

B.1 Survival Analysis

Whenever the elapsed time until a specific event occurs is subject of statistical data evaluation *survival analysis* might provide the appropriate theory and tools. In medical statistics the lifetime of an individual suffering from a lethal disease might be of interest for the evaluation of a new treatment. In this case the specific event is actually death. However, an event could also be represented by a certain failure mode of an electrical component whereas the time could describe the amount of usage of the device. Various literature on survival analysis is available such as a comprehensive textbook from Kleinbaum and Klein (2011). The following paragraphs outline the fundamental definitions and important tools used for detailed evaluation of data obtained from the SWIFI test campaign.

Let X be a random variable describing the survival time of an individual or the amount of usage of a device until a specific failure occurs. Let further f describe the probability density function of X. Then, the cumulative distribution function F is defined as:

$$F(x) = \mathbf{P}(X < x) = \int_0^x f(s)ds \tag{B.1}$$

In survival analysis, the survival function S describes the probability of an individual surviving until time x. Thus, the survival function is defined by:

$$S(x) = \mathbf{P}(X \geq x) = 1 - F(x) = \int_x^\infty f(s)ds \tag{B.2}$$

The corresponding hazard function $h(x)$ describes the instantaneous failure rate or force of mortality and can be defined as:

$$h(x) = \lim_{dx \to 0} \frac{\mathbf{P}(x \leq X < x + dx \mid X \geq x)}{dx} = \frac{f(x)}{S(x)} = -\frac{S'(x)}{S(x)}. \tag{B.3}$$

The tools provided by survival analysis allow to estimate and interpret the survival function from survival data obtained by real observations. Thus, survival functions from different survival data sets can be compared and the results can be correlated with further determining factors. Various measures for comparison of survival functions exist. A simple but meaningful measure is given by a selection of quantiles Q_p which can directly be derived from the survival function. For each $p \in [0,1]$ the corresponding quantile Q_p is defined as:

$$Q_p = S^{-1}(1-p) = \inf\{x : S(x) \leq 1-p\} \tag{B.4}$$

With this definition $Q_{0.5}$ describes the *median lifetime* or *median amount of usage until failure*. Another interesting quantile is $Q_{0.95}$ which describes an upper limit for the time to failure of the majority (95%) of the observations.

For some observations the exact survival time of an individual might be unknown for different reasons. This can be due to the fact that the observation has been stopped before the specific event has occurred or the individual dropped out of the study for any other reason beside the event of interest. In this case only partial information is known about the individual and the observation is called *censored*. One speaks of right censoring when the individual has been observed from beginning on until a certain time but the exact survival time is unknown. In this case the only information available is that the event of interest did not occur within the observed time interval.

Once a sufficient number of observations has been recorded the empirical survival function of the observed population can be estimated. The Kaplan-Meier-Estimator (Kaplan and Meier, 1958) is a non-parametric estimator which also takes into account censored data. The confidence interval of the estimated survival function for a given confidence level can further be computed using Greenwood's formula (Greenwood, 1926).

B.2 Detailed Fault Injection Survival Analysis

In the following sections a more detailed statistical analysis of the event log recorded during the bit error injection test campaign as described in section 4.4 is presented.

Statically Allocated RAM (BSS)

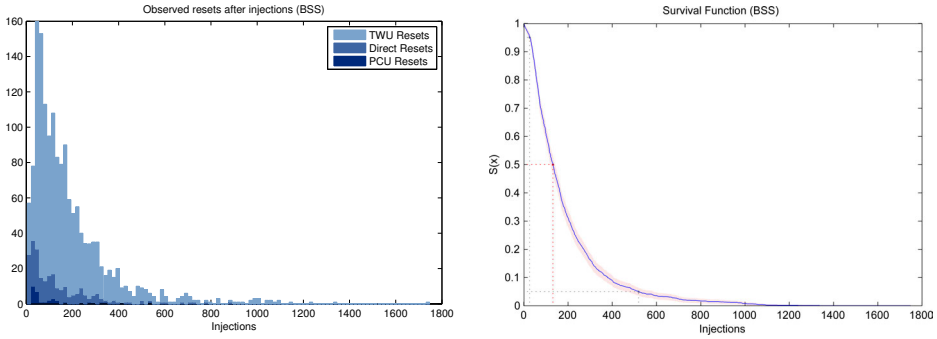


Figure B.1: SWIFI reset statistics for BSS as histogram (left) and estimated survival function (right).

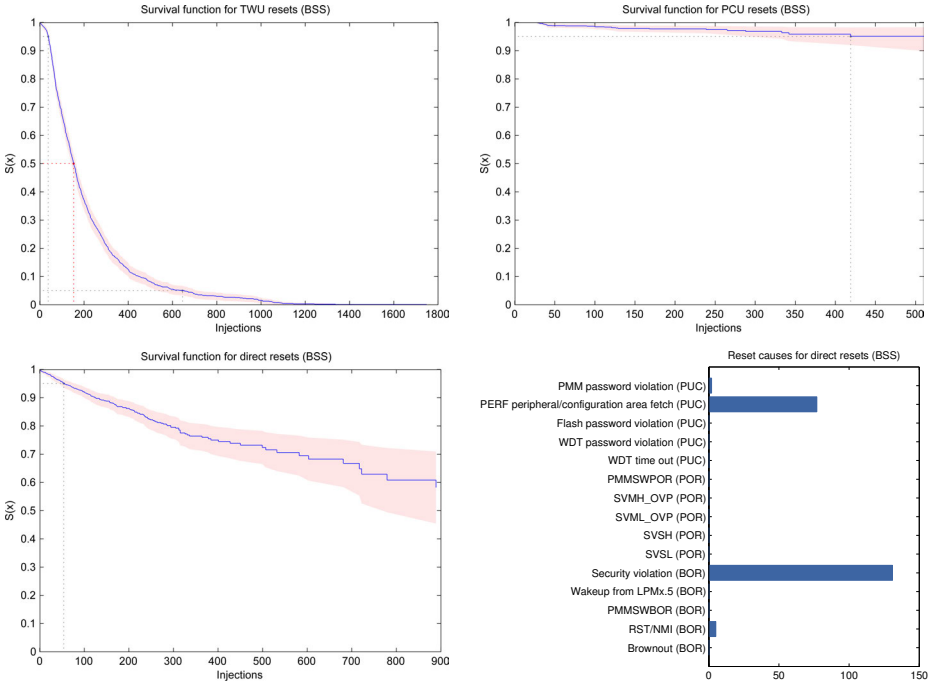


Figure B.2: Estimated survival functions for TWU recovery (top, left), PCU recovery (top, right) and direct resets with corresponding reset causes (bottom) in BSS memory.

Stack

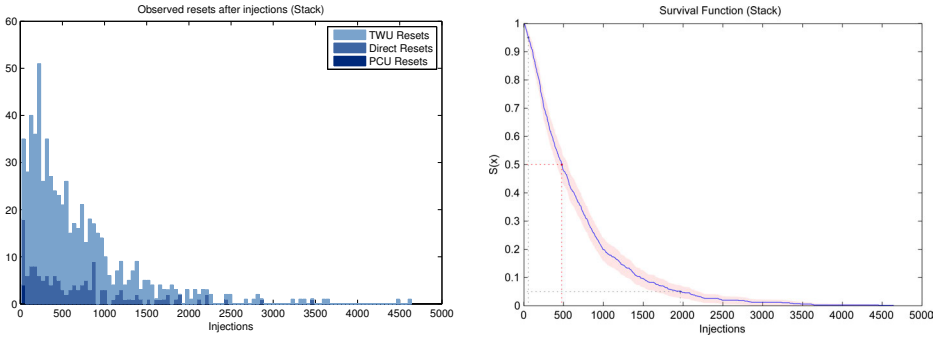


Figure B.3: SWIFI reset statistics for stack as histogram (left) and estimated survival function (right).

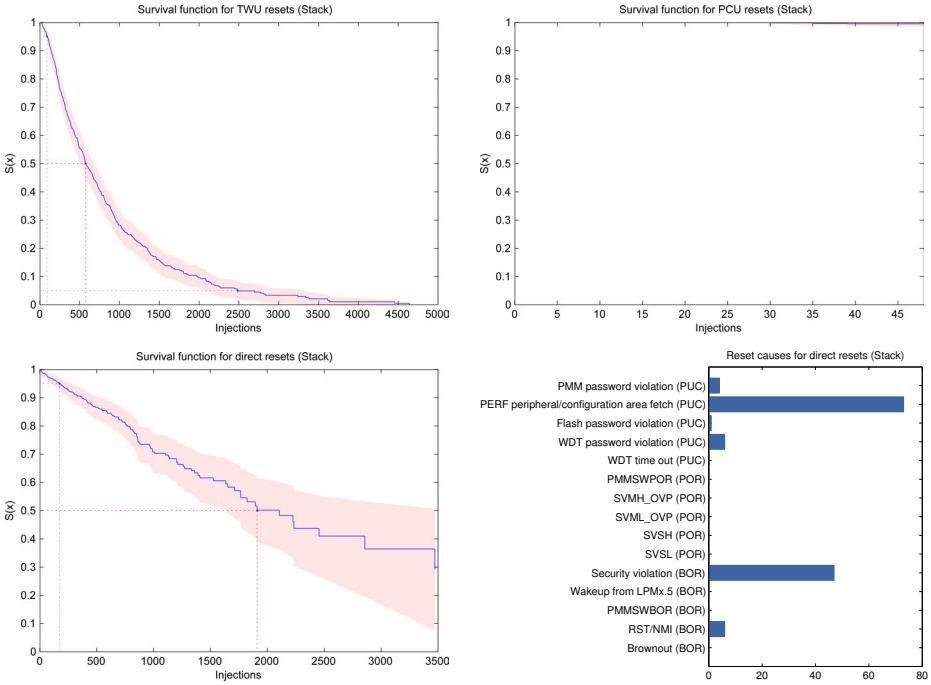


Figure B.4: Estimated survival functions for TWU recovery (top, left), PCU recovery (top, right) and direct resets with corresponding reset causes (bottom) in stack memory.

Peripheries (PER)

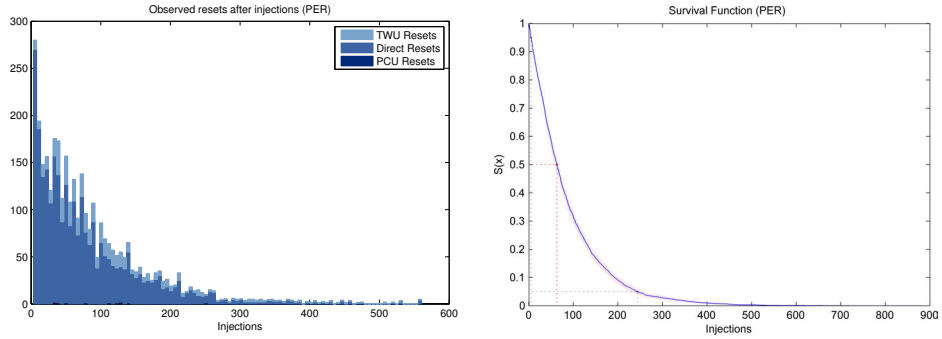


Figure B.5: SWIFI reset statistics for periphery memory as histogram (left) and estimated survival function (right).

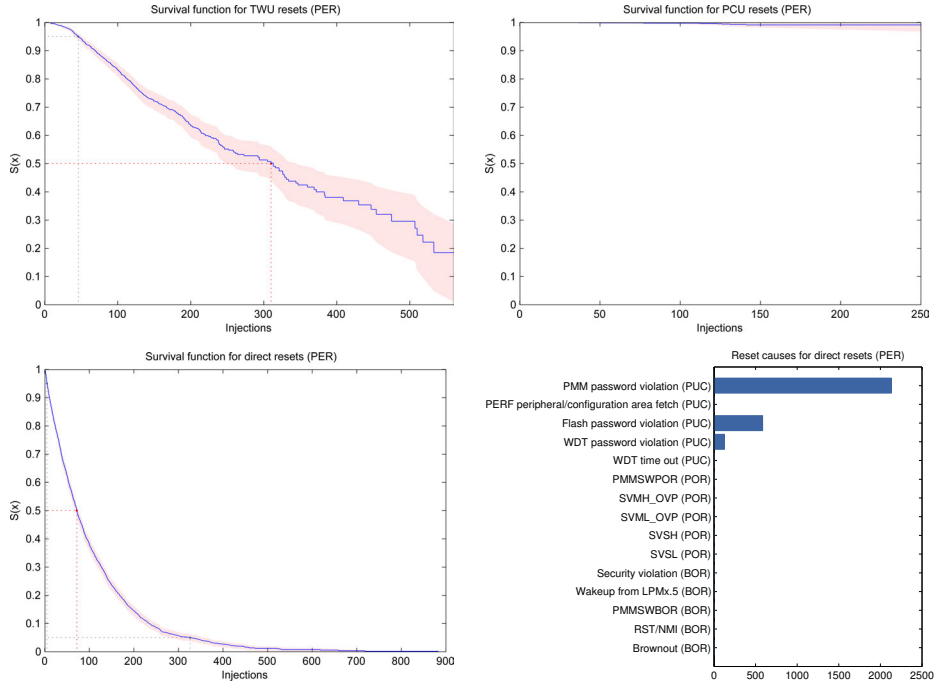


Figure B.6: Estimated survival functions for TWU recovery (top, left), PCU recovery (top, right) and direct resets with corresponding reset causes (bottom) in periphery memory.

Local Program Memory (LP)

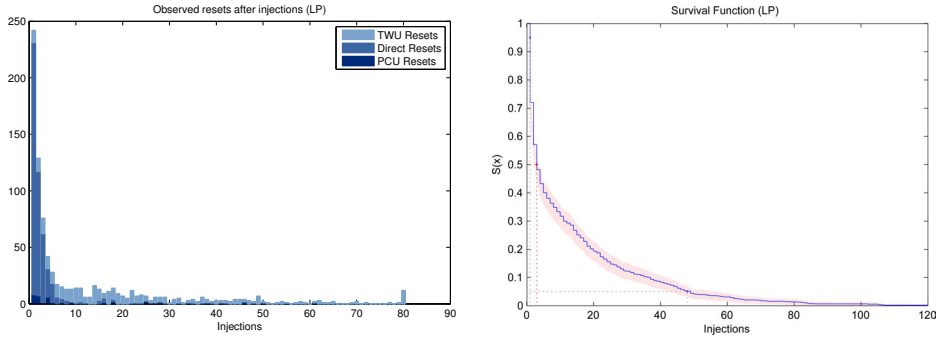


Figure B.7: SWIFI reset statistics for local program memory as histogram (left) and estimated survival function (right).

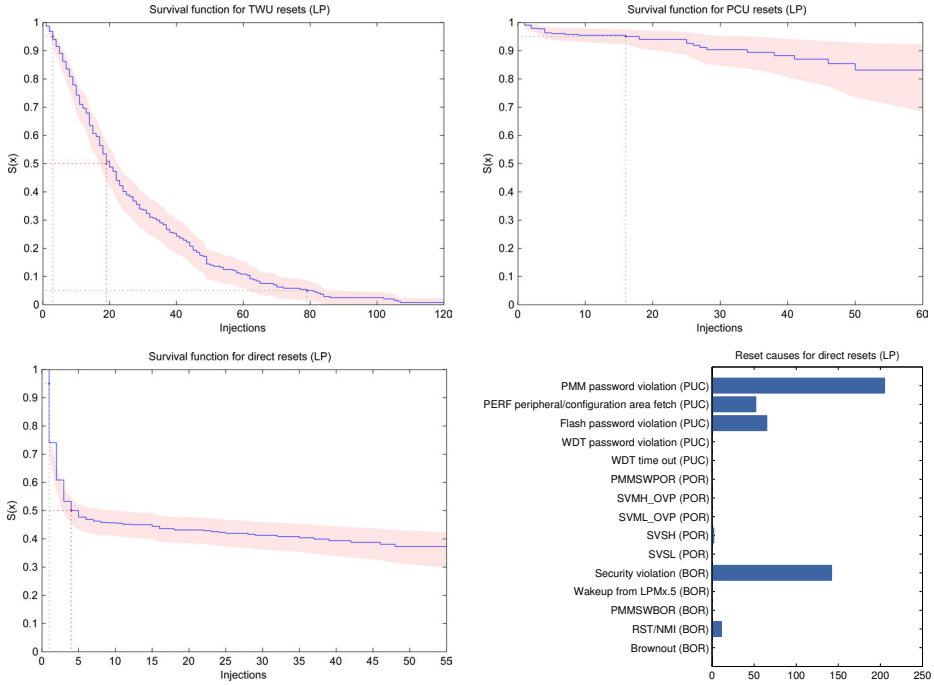


Figure B.8: Estimated survival functions for TWU recovery (top, left), PCU recovery (top, right) and direct resets with corresponding reset causes (bottom) in local program memory.

Summary

$S(x)$	PER	BSS	STACK	LP
min	1	1	5	1
$Q_{0.05}$	5	27	58	1
median	63	132	477	3
$Q_{0.95}$	244	519	1966	48
max	883	1748	4642	405
$S(x)$ PCU	PER	BSS	STACK	LP
min	35	28	30	1
$Q_{0.05}$		419		16
median				
$Q_{0.95}$				
max	253	530	48	61
$S(x)$ TWU	PER	BSS	STACK	LP
min	3	3	16	1
$Q_{0.05}$	46	38	90	3
median	310	153	577	19
$Q_{0.95}$		645	2485	79
max	561	1748	4642	405
$S(x)$ Direct	PER	BSS	STACK	LP
min	1	1	5	1
$Q_{0.05}$	5	54	173	1
median	72		1910	4
$Q_{0.95}$	326			
max	883	889	3472	55

Table B.1: SWIFI test campaign statistics.

List of Tables

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