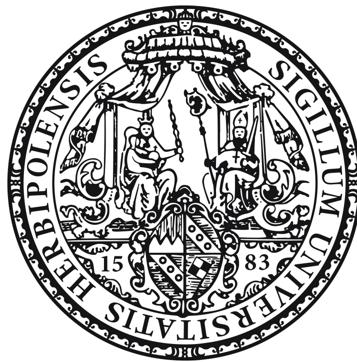
Molecular Beam Epitaxy of 2D and 3D HgTe, a Topological Insulator



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Contents

1 Introduction **1**

2 HgTe, a Topological Insulator **3**
2.1 Topological Insulator 3
2.2 Crystal Structure 5
2.3 Band Structure 6
2.4 HgTe - Two-Dimensional Topological Insulator 10
2.5 HgTe - Three Dimensional Topological Insulator 14

3 Experimental Techniques **17**
3.1 Molecular Beam Epitaxy - MBE 17
3.1.1 MBE-Setup in the EP III Laboratory 17
3.1.2 CMT - Chamber 18
3.1.3 Reflection High Energy Electron Diffraction - RHEED 21
3.1.4 Growth Modes 22
3.2 Analyzing Apparatuses 25
3.2.1 X-ray Photoelectron Spectroscopy - XPS 25
3.2.2 Differential Interference Contrast Microscopy 27
3.2.3 High Resolution X-ray Diffraction - HRXRD 28
3.2.4 Atomic Force Microscopy - AFM 33
3.3 Microstructuring and Electronic Transport Measurements 34

4 CdTe-Buffer on GaAs:Si **39**
4.1 MBE Growth 39
4.2 Characterization 46
4.2.1 GaAs:Si - Preparation 46
4.2.2 ZnTe - Growth 49
4.2.3 CdTe - Growth 52
4.2.4 Etch Pit Density 57
4.3 Summary 59

5 Undoped HgTe - Quantum Wells **61**
5.1 HgTe QWs on commercial CdTe 61
5.2 Surface 2DEGs 69
5.3 HgTe QWs on CdTe/GaAs:Si 72
5.4 Pre-Growth Preparation: HF Etching 81
5.5 Summary 85

6 HgTe - Bulk Structures 87
6.1 HgTe directly on CdTe substrate 87
6.2 HgTe Bulk embedded in CMT Layers 94
6.3 Summary 101

7 Summary 103

Zusammenfassung 107

Bibliography 111

List of Publications 123

Acknowledgement 127

List of Abbreviations and Symbols

2DEG	two-dimensional electron gas
a	lattice constant
$a_{\perp}$	vertical lattice constant
$a_{\parallel}$	horizontal lattice constant
AFM	atomic force microscopy
ALE	atomic layer epitaxy
ARPES	angle-resolved photoemission spectroscopy
B	magnetic field
CB	conduction band
CdTe	cadmium telluride
CMT	cadmium mercury telluride
d_c	critical thickness
EDS	energy-dispersive X-ray spectroscopy
f	lattice mismatch
FWHM	full width at half maximum
GaAs	gallium arsenide
HAADF	high-angle annular dark field
HF	hydrochloric acid
HRXRD	high resolution X-ray diffraction
LN_2	liquid nitrogen
MBE	molecular beam epitaxy
MEE	migration-enhanced epitaxy

ML	monolayer
MT	mercury telluride
N_2	molecular nitrogen
PBN	pyrolytic boron nitride
QSH	quantum spin hall
QW	quantum well
RHEED	reflection high-energy electron diffraction
RMS	root mean square
RSM	reciprocal space map
SdH	Shubnikov de Haas
TEM	transmission electron microscopy
U_{bg}	back gate voltage
U_g	gate voltage
UHV	ultra high vacuum
VB	valence band
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectivity

1 Introduction

In the majority of cases particle physics or astronomy is getting all the attention because the humanity is especially interested in the world of elementary particles and the infinite universe. Thus, the solid state physics is forgotten often. But no other physical field of research have been made considerable process in the past few years and here a new world opens up at the edges of certain materials literally. So, the most interesting topic of solid-state physics and material physics is the field of so-called "topological insulator" for almost the last 10 years. As an application, the edges of these materials may revolutionize the computer-chip industry and replace the silicon. Furthermore, these materials are predicted to provide all components for quantum computing. To understand these edge states, completely new concepts are required physically.
Firstly in 2005, these edge state concept was presented by Kane and Mele in graphene [1]. In the following years, several other materials were predicted and proved to join the group of topological insulators like $Bi_{1-x}Sb_x$, Bi_2Te_3, Bi_2Se_3, Sb_2Te_3, α-Sn [2, 3, 4, 5, 6]. However, in 2007 the first experimental discovery of the quantum spin Hall state which is associated with topological insulators is made in HgTe quantum wells at the Experimentelle Physik III (EPIII) in Würzburg by König *et al.* [7]. Due to crystalline impurities, low carrier densities and mobilities this effect is discovered in no other material system until now. Furthermore, the class of topological insulators provides a lot of more physical effects. So it is possible that completely new physical effects and particles can be discovered in topological insulators in combination with other materials like superconductors or magnetic materials [8, 9].
Furthermore, the discovery of the quantum spin Hall state in HgTe does not mean that this material system is exhausted. Due to the long tradition of Hg-based MBE growth, this material system provides world-best research in this physical field at EPIII. Equipped with a new MBE chamber, the growth process of HgTe quantum wells and strained HgTe bulk layers should be improved to understand the material system more clearly.
This thesis is therefore structured in five chapters:

- Chapter 1 just gives a short introduction and overview of this thesis which deals with the MBE growth and characterization of HgTe as a two and three dimensional topological insulator.

- In the 2. chapter the theory of this material system is given and explained in detail based on examples. Firstly, the field of topology is introduced shortly, followed by a closer description of the used material system $Hg_{1-x}Cd_xTe$ (CMT). Here, the crystal structure and band structure provide an insight of why and how this material system supplies these special properties. On the basis of HgTe quantum wells, a detailed explanation of a two dimensional topological insulator is given and former results are shown. At last,

the mechanism is described how HgTe is a topological insulator in the three dimensional case. Here, theory and previous results are shown.

- Chapter 3 has the focus on the applied experimental techniques. Here, the principle of MBE is explained on the basis of the CMT - chamber and the UHV system of EPIII. In addition, the analyzing apparatuses which are used during this thesis are listed and explained. This includes XPS, Nomarski microscopy, HRXRD and AFM. For electronic characterization measurements, principles of the lithography process and short introduction of low temperature measurements are shown at the end of this chapter.

- The MBE growth of (001) CdTe on (001) GaAs is discussed in chapter 4. This part was not planned at the beginning of the thesis and opened up due to unpredictable circumstances (earthquake and tsunami in Japan in 2011). Firstly, the MBE growth process and its optimization is demonstrated extensively. After that, the characterization results are shown and discussed in detail. The part is split in the analysis of the GaAs:Si preparation, the ZnTe growth and CdTe growth via Normaski microscopy, HRXRD and AFM. Additionally, etch pit density measurement technique was developed and applied.

- Chapter 5 is about undoped HgTe quantum wells. Here, the MBE growth and characterization via HRXRD and transport measurements is shown for HgTe quantum wells grown on commercial CdTe substrates. Furthermore, quantum wells located near the surface are discussed in another part. The main part here is the MBE growth and characterization of HgTe quantum wells grown on CdTe/GaAs:Si substrates which is a completely new issue. By rounding up this chapter, a new oxide etching test series on the CdTe substrates is shown and evaluated. Here, some experiments between HF and HCl as an etchant of CdTe oxide is shown the the results are compared and interpreted.

- As the main part of this thesis, chapter 6 deals with the MBE growth and analysis of HgTe bulk structures. At the beginning, HgTe bulk layer grown directly on commercial CdTe substrates are discussed. This is based on previous work and serves for better understanding of existing data and lays the foundation for the following. Therefore, a new MBE growth process is introduced for HgTe bulk layers in which the HgTe layer is embedded between HgCdTe barriers. This innovation results in an improvement of the interface conditions and therefore in a huge increase in carrier mobility. At last, a short introduction is given how the CdTe/GaAs:Si structure serves as a back gate for the HgTe bulk layer and can now manipulate the top and bottom surface separately in combination with a top gate.

So, all this investigations enhance the crystalline and electronic properties of HgTe as a two or three dimensional topological insulator and therefore also followed experiments. Therefore, this material system in connection with other materials will help to understand the field of topological insulators more explicitly.

2 HgTe, a Topological Insulator

In this chapter, mercury telluride (HgTe) is introduced as a member of a new class of matter, the topological insulator. Firstly, there is a short excursion to the field of topology. After that the crystal structure of $Hg_{1-x}Cd_xTe$ will be discussed because in this thesis HgTe, HgCdTe and CdTe are used during the whole MBE process. The band structure has to be explained in order to interpret the magneto transport measurements. Furthermore, there are three options to generate a topological insulator out of HgTe. The two and three dimensional cases are discussed and analyzed in this thesis, while the one dimensional case is treated elsewhere [10].

2.1 Topological Insulator

Topology is a subarea of mathematics which deals with geometric bodies and their transformation into one another through certain deformation. This transformation is called homeomorphism. If two bodies are marked homeomorphic, the topology of these two bodies is the same. So for example, a coffee mug and a torus are homeomorphic, but a sphere and a doughnut are not. Fig. 2.1 illustrates this phenomenon:

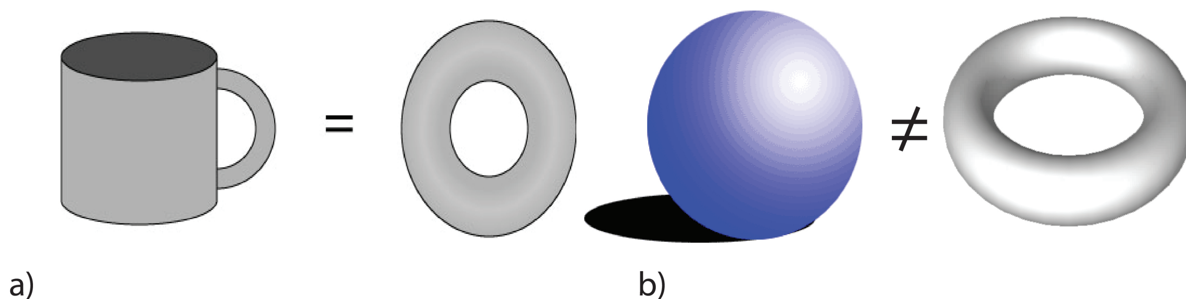


Figure 2.1: a) Coffee mug and torus can be transferred homeomorphic. They have the same topology. b) Sphere and doughnut are not homeomorphic because the quantity of the holes relates these two to different categories of topology.

In condensed matter physics, materials can also be classified into different topology classes. Here, the topology is defined as a Chern number n. This number does not change with a small variation of the Hamiltonian which describes the system. Only a rough change, e.g. a

introduction of a mass, can open or close a band gap. Small changes are comparable with compression or distortion. This is a homeomorphic transition as illustrated above. A strong variation can generate new holes for example. So in this case, conducting states have to exist at the interface of two materials who differ in their Chern number. A transition from an insulator to a topological non-trivial material is such a transition.

An understanding of this transition is given with the help of a 2D band structure. Crystals with an energy gap between valence and current band can be classified by the Chern number n. The surface integral of the total Brillouin zone of a band m is an integer quantized number.

$$n_m = \frac{1}{2\pi}\int d^2\mathbf{k}F_m. \tag{1}$$

F_m is the Berry flux and is given by $F_m = \nabla_k \times \mathrm{i}\langle u_m(\mathbf{k})|\nabla_k|u_m(\mathbf{k})\rangle$ where $|u_m\rangle$ is the Bloch wave function [9]. The total Chern number is defined as the sum over all occupied states $n = \sum_{m=1}^{N} n_m$ and is invariant even if there are degeneracies between occupied bands. This is valid if the gap which separates the occupied and the empty bands persists finite. Therefore the Chern number n is a topological invariant number and can not change even if the Hamiltonian varies smoothly. So therefore the band gap has to vanish at the transition which generates a change in n. This leads to conductive edge states which exist on interfaces between areas with different Chern numbers. Such edge states are well known at the interface between the integer quantum Hall state and vacuum [11]. But these edge states are chiral and so they propagate only in one direction along the edge. Furthermore these states only occur when time-reversal symmetry is broken. However, the new class of topological insulator is allowed by spin-orbit interaction when time-reversal symmetry is unbroken [1]. Here the time-reversal symmetry for spin 1/2 particles plays a big role for understanding this new class. The time-reversal operator Ψ of the Hamiltonian has the property for spin 1/2 electrons: Ψ^2 = -1. Therefore the important requirement known as Kramers theorem occurs in which all eigenstates of a time-reversal symmetry Hamiltonian are at least two fold degenerate. So in the presence of spin-orbit interactions it has non-trivial consequences while in absence of spin-orbit interaction, Kramers degeneracy is simply the degeneracy between spin up and spin down. So the time-reversal Bloch Hamiltonian has to be like:

$$\Psi H(\mathbf{k})\Psi^{-1} = H(-\mathbf{k}). \tag{2}$$

This leads to a resulting Chern number n = 0, but an additional invariant appears with two possible values ν = 0, 1. Fig. 2.2 shows the band structure of a 2D time-reversal invariant insulator parallel to its edge. The colored areas illustrate the bulk conduction and valence bands separated by an energy gap. So if edge states exist in the crystal, the Kramers‘ theorem forces a degeneracy of these states at the points Γ_a and Γ_b. In between, the degeneracy is lifted due to the spin-orbit coupling [cf. Fig. 2.2 (b)]. This represents a topological insulator. In Fig. 2.2 a) the degenerate states are connected in pairs as it is usual in normal insulators.

So, the additional $\mathbb{Z}_2$ invariant ν is deciding if the insulator is normal or topological. ν was able to be calculated by several mathematical formulations [1, 12, 3, 13, 6]. In a 2D system, the perpendicular spin S_z is conserved and the up and down spins have independent Chern numbers $n_\uparrow$ and $n_\downarrow$. Due to time-reversal symmetry, there has to be $n_\uparrow + n_\downarrow = 0$ and $n_\sigma = (n_\uparrow - n_\downarrow)/2$. This difference n_σ defines a quantized spin Hall conductivity and the $\mathbb{Z}$ invariant number

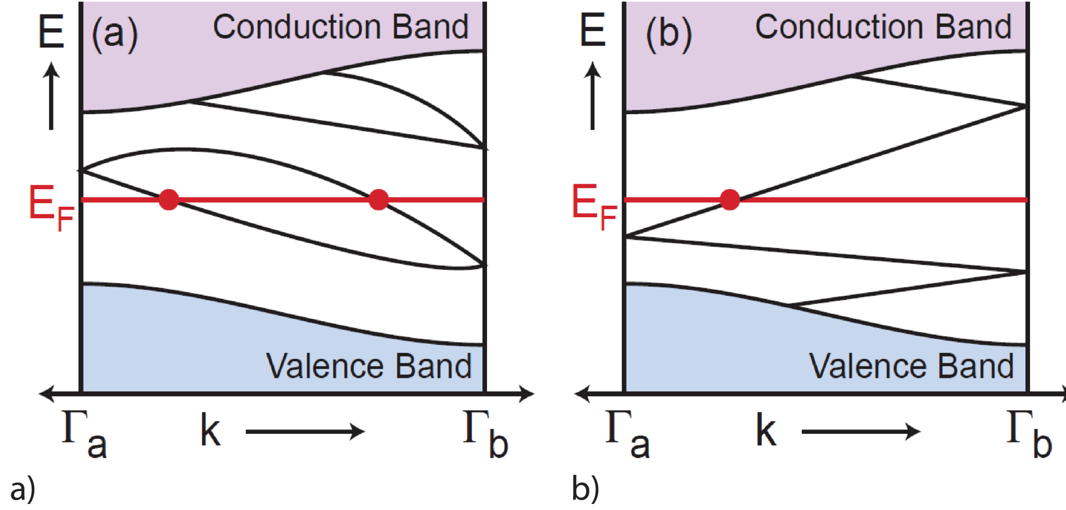


Figure 2.2: a) Pairwise connected edge states in the band gap of an insulator. b) Edge states of a topological insulator [9].

is then $\nu = n_\sigma$ mod 2 [14]. This leads to that a 2D topological insulator has topologically protected helical edge states which form a unique 1D conductor (cf. chapter (2.4)). Another simplification to calculating ν is the assumption of a crystal with inversion symmetry. So in 2007, three different groups generalized this system from 2D into the 3D system [4, 6, 5]. This will be discussed in chapter (2.5).

2.2 Crystal Structure

In this thesis, heterostructures of HgTe, CdTe and $Hg_{1-x}Cd_xTe$ were grown and analyzed. The $Hg_{1-x}Cd_xTe$ narrow gap semiconductors are alloys of CdTe and HgTe where Hg and Cd substitute each other nearly randomly. The composition of CdTe is x and of HgTe is *1-x*. They belong all to the group of II-VI semiconductors and the ground state crystallize in the cubic zincblende structure. Their space group is $F\bar{4}3m$ and their density ranges from 8.05 g cm^{-3} (HgTe) to 5.75 g cm^{-3} (CdTe) linearly [15]. Therefore, all atoms form a sp^3 hybridization. This crystal structure consists of two intersecting face centered cubic sublattices. One sublattice is occupied by Te anions, the other is randomly shared by Cd and Hg cations. In Fig. 2.3 (a), the yellow spheres represent the anions Te, while the cations (Hg, Cd) are illustrated by the grey spheres. These two sublattices are displaced to each other by the shifting ($\frac{1}{4}\,a_0$, $\frac{1}{4}\,a_0$, $\frac{1}{4}\,a_0$). Here, a_0 is the lattice constant [16].

The lattice constant of HgTe is 6.4619 Å [17], and that of CdTe is 6.4825 Å [18]. The lattice constant a of $Hg_{1-x}Cd_xTe$ can be described by [15]:

$$a = 6.4619 + 0.00084 \cdot x + 0.0168 \cdot x^2 - 0.0057 \cdot x^3. \tag{3}$$

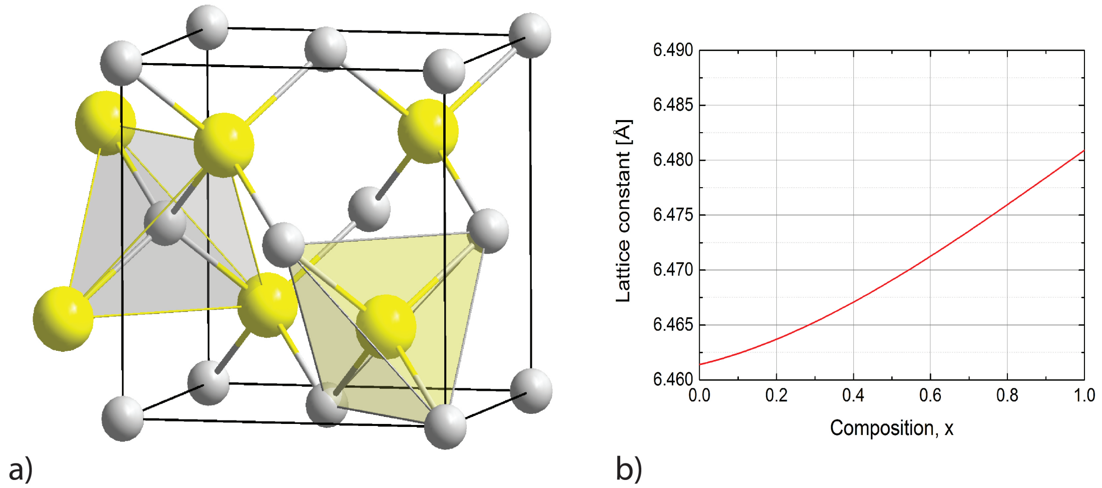


Figure 2.3: a) Zincblende crystal structure [19]: the grey spheres represent the cations (Hg, Cd), the yellow ones the anions (Te). b) Plot of the lattice constant versus composition of $Hg_{1-x}Cd_xTe$.

The lattice constant versus composition is plotted in Fig. 2.3 (b). It was found that the variation of a_0 with composition x is slightly non-linear. There are some different models of lattice constant calculation in literature who differ slightly in some assumptions, but this thesis will always refer to the calculation mentioned above. The density dependence of HgCdTe on composition is linear [20].

The primitive cell of $Hg_{1-x}Cd_xTe$ alloys has two atoms as in all zincblende cubic crystals. Six valence electrons are outside the core filled the shell of a Te atom in a $5S^2$, $5P^4$ configuration. In a Hg atom there are two valence electrons outside the core filled the shell in a $6S^2$ configuration and in a Cd atom in a $5S^2$ configuration. The chemical bond is mainly covalent, but there is a substantial ionic contribution [21]. The bonds direct along tetrahedral directions. The ionic component of the bonds is generated because the potential of Te atoms is deeper than that of the cations. So there is an electron transfer from the cations to the anions. The first Brillouin zone is a truncated octahedron.

2.3 Band Structure

This section discusses the band structure properties of CdTe and HgTe and explains why these heterostructure is suitable for topological insulator. The band structures of II-VI semiconductors were studied by Dresselhaus and Parmenter in the 1950s [22, 23]. At that time, they found already that the top of the valence band is composed of the p-symmetry Te states. Therefore it is six fold degenerate, including spin. The bottom of the conduction band is based on the s-symmetry states and is two fold degenerate. The conduction band is derived from the Cd or

Hg s-states. Due to the effect of **k·p**[1] and spin-orbit interaction terms, the symmetry of the Hamiltonian is broken and the degeneracy of the valence band is lifted into so-called Γ_8-bands and a split-off band (Γ_7).

At the Γ point (K=0), the Γ_8 band is four fold degenerate and the Γ_7 is two fold degenerate. The bottom of the conduction band is named Γ_6. Since Hg and Cd are elements with large atomic numbers and their electrons move faster in their orbitals, the relativistic corrections have to be included which leads to the spin-orbit interaction for the band structures of HgTe and CdTe and is large. So the Hamiltonian of a single electron contains the normal non-relativistic term H_1, the first correction term H_D (Darwin interaction), the second correction term H_{mv} (mass-velocity interaction) and the third correction term H_{SO} (spin-orbit interaction). The impact on the band structure for these corrections is shown in Fig. 2.4. Here the

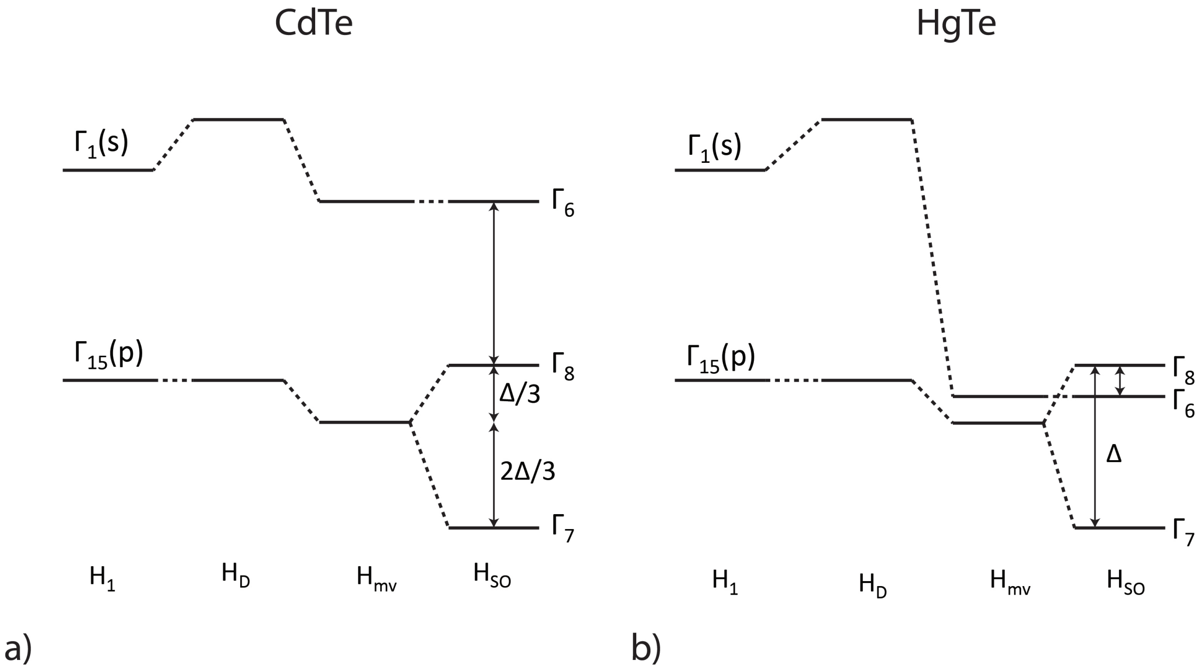


Figure 2.4: The formation of energy levels at the Γ-point in CdTe and HgTe due to their energy corrections.

energy levels which originate from the non-relativistic term H_1 are the same. The Darwin term H_D affects only the s-orbits and has for HgTe and CdTe almost the same value. The mass-velocity term induces a very different correction in the two compounds due to the large difference between the atomic masses of Hg and Cd (M_{Hg} = 200.6 u; M_{Cd} = 112.4 u). The spin-orbit interaction is dominated by the Te and therefore exhibits the same value. Due to all these relativistic correction terms, the position of the Γ_6 state is exchanged with the Γ_8 state in HgTe.

[1]The **k·p** is a perturbation method to research the wave-functions depending on the crystal symmetry, so the band structures can be calculated around some points in k space.

In Fig. 2.5, the whole band structure of CdTe and HgTe is shown. Here it is clearly visible that CdTe has a direct band gap at the Γ-point with a band gap of 1.56 eV. The band gap is calculated by the difference of the Γ_6 and the Γ_8 state: $E_G = \Gamma_6 - \Gamma_8$. In HgTe there is therefore a negative band gap of E_G = - 0.3 eV. Actually, in HgTe the Γ_8 band splits for $k \neq 0$ in a light hole (lh) and a heavy hole band (hh) which form the conduction (CB) and valence band (VB), respectively. So this is the reason that HgTe is a semi-metal because the band gap is zero. So for this symmetry inverted systems, the $\mathbb{Z}_2$ constant ν can be calculated out of the eigenvalues $\pm$ 1 of the parity operator. The parity change of the VB creates HgTe-CdTe as a candidate for a topological insulator. In two dimensional systems, topological insulators were also called quantum spin Hall (QSH) insulator in literature.
To sum up, this type of insulator has a charge excitation gap in the bulk , but has topologically protected gapless edge states which lie inside the bulk insulating gap and are invariant under time-reversal. Furthermore, in the two dimensional case the corresponding edge states have a distinct helical property which means that two states with opposite spin polarization counter-propagate at the given edge while in the three dimensional case the edge states add up to a two dimensional conducting surface with a spin momentum locking [1, 24, 25].
The topological properties of this HgTe-CdTe heterostructure will be discussed at first in the two dimensional system 2.4 and later on in the three dimensional system 2.5.

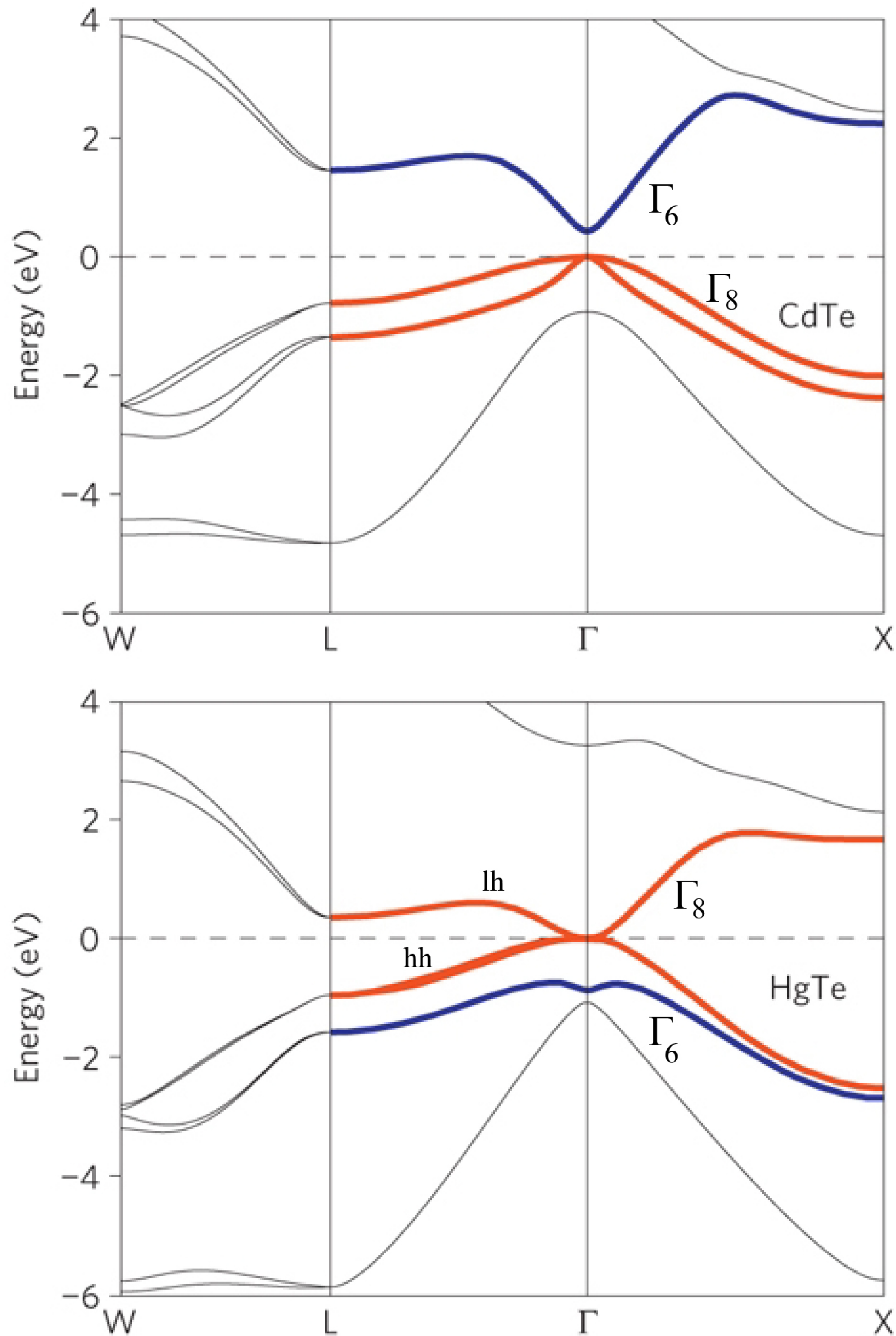


Figure 2.5: Band structure of CdTe and HgTe [26]. The bands of the CdTe band structure are ordered normal and between the Γ_8 and Γ_6 there is band gap. The Γ_8 and Γ_6 bands are inverted in HgTe and due to the touching of the Γ_8 bands at the Fermi energy (0 eV) HgTe is a semi-metal.

2.4 HgTe - Two-Dimensional Topological Insulator

If the dimension of a system is restricted in one direction, so that just the ground state is occupied, then there is originated a two dimensional electron or hole gas, depending on their charge carrier type. This two dimensional system is called a two dimensional electron gas (2DEG). A quantum well (QW) describes the course of its potential.
HgTe/CdTe quantum well structures offer a lot of special features provided primarily through the topological properties of HgTe. Due to these special features, a lot of quantum well structures can be fabricated with different properties for investigating plenty of physical effects. Especially, the understanding of the sub-band structure of the QW is very important.
As already mentioned, HgTe is a semi-metal as bulk material where the Γ_8 band forms both the conduction and the valence band. Additionally, the Γ_6 band is energetically located below the Γ_8 band with a negative band gap of $E_G \approx$ - 0.3 eV. In contrast to it, $Hg_{1-x}Cd_xTe$ is a semiconductor with a positive band gap for $x > x_0$ and CdTe exhibits a positive band gap of 1.56 eV. The band gap E_g of $Hg_{1-x}Cd_xTe$ is given by [15]:

$$E_g = -0.302 + 1.93 \cdot x + (5.35 \times 10^{-4}) \cdot T \cdot (1 - 2 \cdot x) - 0.81 \cdot x^2 + 0.832 \cdot x^3. \quad (4)$$

Here, x is the composition and T the material temperature.
Thus, the Γ_6 band lies above the Γ_8 band. In Fig. 2.6 the band structure of HgTe and $Hg_{0.32}Cd_{0.68}Te$ at the Γ-point is shown in a). The band gap of $Hg_{0.32}Cd_{0.68}Te$ is around 1 eV. Fig. 2.6 (c) shows the energetic sub band ordering of the resulting quantum wells for two quantum well thicknesses. This quantum well structures are so called type III quantum wells. This scheme and dispersion at the Γ-point is calculated by an 8 x 8 $\mathbf{k}\cdot\mathbf{p}$ model. Furthermore, the inverted band structure of the quantum well is presented. Due to quantum confinement, the energetic position of the sub-bands in the QW depends on the QW thickness d and the strain of the system [cf. Fig. 2.6 (b)]. For $d < d_c$ the sub-band E_1 (originates from the Γ_6 band) lies above the sub-band H_1 (originate from the Γ_8 band). The system acts now as an ordinary semiconductor. For $d > d_c$ the order of the bands is inverted and a 2D topological insulator exists. At a critical thickness d_c the bands are touching each other and the system is now called a zero-gap system. The critical thickness d_c is on a lattice matched substrate 6.3 nm and 6.6 nm on CdTe with a lattice mismatch of around 0.3 % [7, 24, 29]. These critical thickness will allow to compare the characteristic 2D TI regime with the characteristics of the normal regime.
In 2005 Kane and Mele predicted paired counterpropagating states which are completely spin polarized and lie in the band gap of the 2D system with band inversion. These states are called helical edge states. While in a quantum Hall system backscattering is suppressed by the channel pretended transport direction, the scattering in a QSH system is forbidden at non-magnetic impurities due to destructive interference. The system which were discussed by Kane and Mele [1] was graphene and exhibits a very small band gap which is inappropriate for detecting the QSHE. In 2007, the first experimental discovery of the quantum spin Hall effect in HgTe/HgCdTe heterostructures was done by König *et al.* [7].
In Fig. 2.7 the longitudinal four-terminal resistance, $R_{14,23}$, of various quantum well structures as a function of gate voltage is shown measured for B = 0 T at T = 30 mK. One normal (d = 5.5 nm) (black) and three inverted (d = 7.3 nm for red and green, d = 7.5 nm for blue) QWs

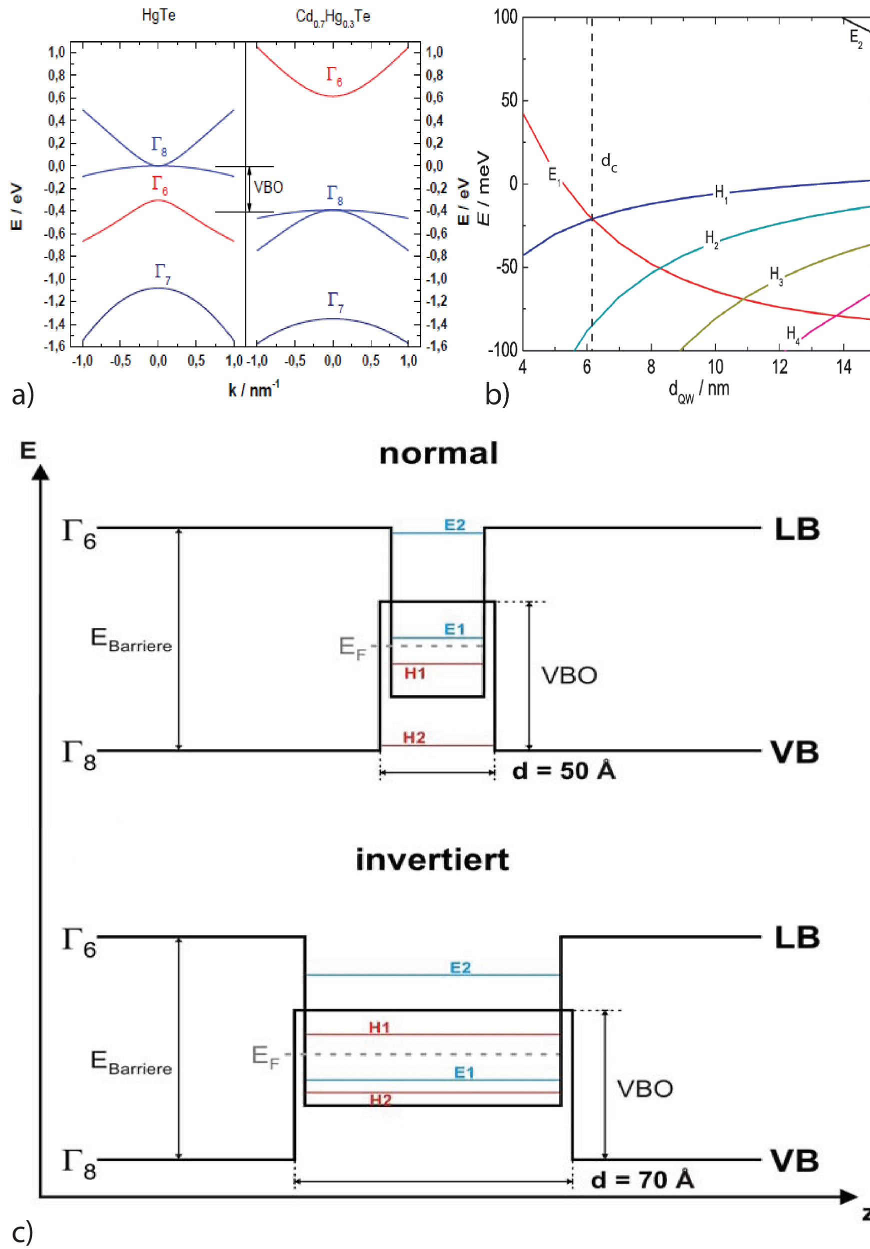


Figure 2.6: a) Sketch of the band structure of HgTe and $Hg_{0.32}Cd_{0.68}Te$ at the Γ-point. b) The energy of the states in the QW are plotted as a function of the width of the HgTe QW layer on a lattice matched substrate. c) Sketch of a HgTe quantum well embedded in HgCdTe barriers with sub-bands E_i and H_i. At the top: the not inverted band structure of a 5 nm thick quantum well. At the bottom: the inverted band structure of an 7 nm thick quantum well [27, 28].

were measured. The measurements were performed on Hall bar structures with the size of (1.0 x 1.0) μm^2 for black and blue, (2.0 x 1.0) μm^2 for device red and (1.0 x 0.5) μm^2 for device green. The current I_{14} is sent from contact 1 to contact 4 and the voltage U_{23} is measured between the contacts 2 and 3 [cf. Fig. 2.7 (b)]. So, the longitudinal resistance $R_{14,23}$ is:

$$R_{14,23} = \frac{U_{23}}{I_{14}}. \tag{5}$$

The Fermi level is varied by an applied gate voltage from the CB through the gap to the VB. For sample I (d = 5.5 nm) the electrical conductivity vanishes as expected for $d < d_c$ when the Fermi level is located in the band gap. The residual conductivity is the detection limit of the lock-in equipment used in the experiment. This is the clearly expected behavior of an conventional insulator. However, all other three inverted quantum well structures show a finite resistance in the insulating regime due to edge channel transport. Devices III and IV show exactly the theoretical proposed conductivity $G = 2e^2/h$. These two samples differ only in the width of the Hall bar. These results provide a first evidence for the existence of the QSHE in inverted HgTe quantum wells [7]. Due to the fact that the longitudinal resistance reaches the value of $h/2e^2$ independent of the sample geometry of the Hall bars. This can not be explained by usual diffuse electrical transport and is characteristic for edge channel transport. While this results provide first evidences for the existence of edge states in inverted HgTe QWs, the final proof for the predicted helical nature of these edge states has to be realized by a set of non-local transport measurement in the QSHE regime [7, 27, 30, 31, 32, 33, 34, 35, 36].

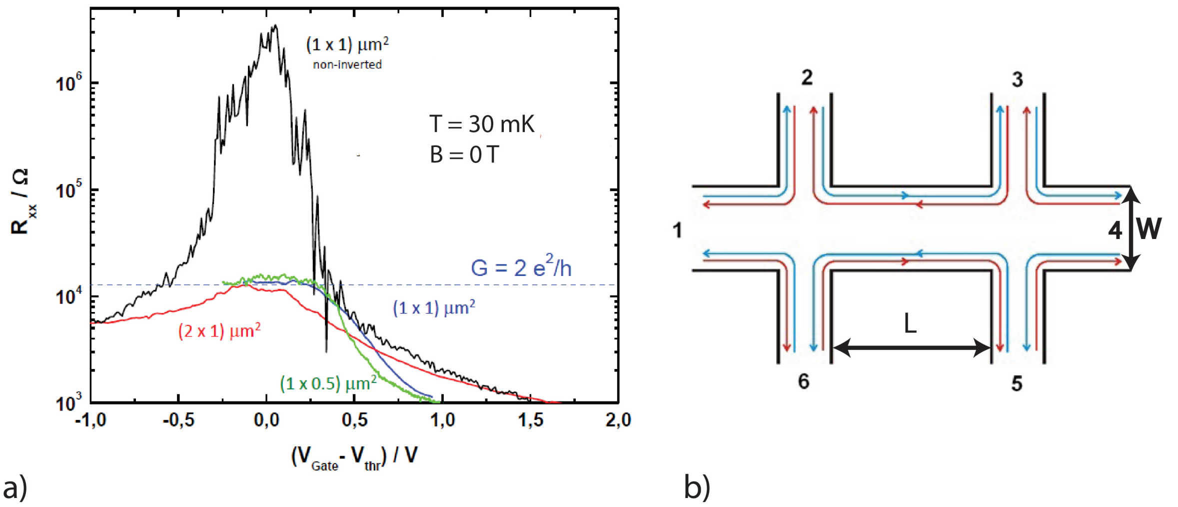


Figure 2.7: a) Longitudinal four-terminal resistance $R_{14,23}$ of four different devices: one normal (5.5 nm) and three inverted (7.3 nm) quantum wells. b) Schematic sketch of a Hall bar structure with the quantum spin Hall edge states illustrated [7, 27].

Till to the start of this thesis all samples were grown on $Cd_{1-x}Zn_xTe$ substrates. This substrates have nearly the same lattice constant as HgTe due to their zinc content and accomplished a high n-doping. Unfortunately, the availability of high quality CdZnTe was suddenly

limited because of production problems which made it necessary to search for alternatives. So a substrate is needed which provides high crystalline quality, nearly the same lattice constant as HgTe, long-time stability and a positive, large band gap. Therefore, only CdTe satisfies all this criteria.So in this thesis, only CdTe substrates were almost used to grow on. With the discovery of the QSHE, the ambition emerged to grow HgTe samples with lower carrier density. This offers the possibility that the Fermi energy can be tuned through the band gap by applying a gate voltage. So, a clean refurbished MBE chamber launched with the beginning of this thesis and this was the perfect moment to start growing undoped HgTe sample. In this thesis, only undoped HgTe quantum wells were analyzed.

2.5 HgTe - Three Dimensional Topological Insulator

In 2007, the theory for topological insulators was extended from 2D systems to 3D systems [4]. Similar to chapter 2.1, these time-reversal invariant systems can be characterized by four $\mathbb{Z}_2$ invariants ν_0, ν_1, ν_2, ν_3. Here, ν_0 indicates the kind of a 3D topological insulator. For $\nu_0 = 0$, it is a weak topological insulator (WTI) which is comparable with a layered 2D state. For $\nu_0 = 1$, a strong topological insulator (STI) is generated which exhibits a distinct 3D state. ν_1, ν_2 and ν_3 refer to the translational symmetry of the lattice. In the presence of disorder, WTI acts like a trivial insulator. In STI, topologically protected surface states arise with a linear dispersion relation and are Kramers degenerated. Furthermore these Kramers degenerate points form 2D Dirac points in the surface band structure. These surface states of a STI build a single continuous 2D topological metal with a spin momentum locking. For a normal metal, there are spin up and spin down at every point at the Fermi surface. Here on a STI metallic surface, the surface spins are not spin degenerated (helical). Due to time-reversal symmetry, the spins have the opposite direction at momenta **k** and -**k**. Therefore the spin rotates around the Fermi surface [3, 4, 9].

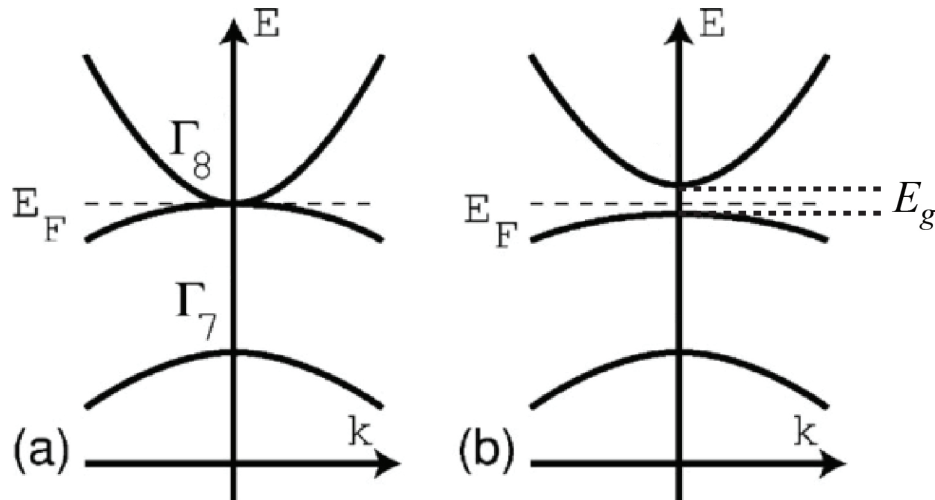


Figure 2.8: Band structure sketch of a) unstrained and b) uni-axially strained HgTe at the Γ-point [3].

HgTe is a semi-metal. In order to form a topological insulator, there has to open up a band gap. Fu and Kane [4] predicted in 2007 that uni-axial strain opens up a band gap between the Γ_8 heavy and light hole band (Fig. 2.8). This can be done by MBE. Here, a proper substrate has to be selected. Due to the large lattice constant of HgTe, a lot of substrates, which are well-known and inexpensive to produce, exclude themselves only because of the smaller lattice constant. So, Si, InP or GaAs exhibit lattice constants below 5.9 nm. This huge lattice mismatch will cause a lot of growth defects. This can be seen in chapter (4) where CdTe is grown on GaAs by MBE. Beside the lattice constant, the crystalline quality, long-life

stability, adequate large band gap, non-magnetic, II-VI material and an ordinary processability are very important. Furthermore, a small lattice mismatch is requested because strain opens up a band gap in HgTe bulk samples. Therefore, all this specifications are satisfied by CdTe only. Though, other substrates like MnTe, MgTe or InSb have similar lattice constants but the handling and further processing is very complicated. Additionally, MgTe is very unstable at oxidizing atmosphere. Furthermore, CdTe is a well investigated material because it is used as substrate of the infrared technology. HgTe is grown tensile uni-axially strained on CdTe in the (001) direction. This leads to a split of the Γ_8 heavy and light hole bands with a maximum band gap $E_G \approx 22$ meV at the Γ-point due to the lattice mismatch of around 0.3% [37, 40]. Fig. 2.9 shows an angle-resolved photoemission spectroscopy (ARPES) measurement of a 1 μm thick HgTe layer grown on CdTe. Due to the thickness, the HgTe layer is approximately completely relaxed and exhibits its natural lattice constant. This is an assumption and based on experience. This thesis will investigate therefore the topic of strain and relaxation more in detail. The relaxation, however, closes the band gap again. Furthermore, there is clearly visible the presence of the linearly dispersing surface state band (SSB) and the coexisting bulk bands (BB). Here, the surface states arise out of the band inversion of the Γ_8 light hole and the Γ_6 electron band, according to theory [41]. The bulk band belongs to the Γ_8 heavy hole band and show up almost at the same energy as the surface states.

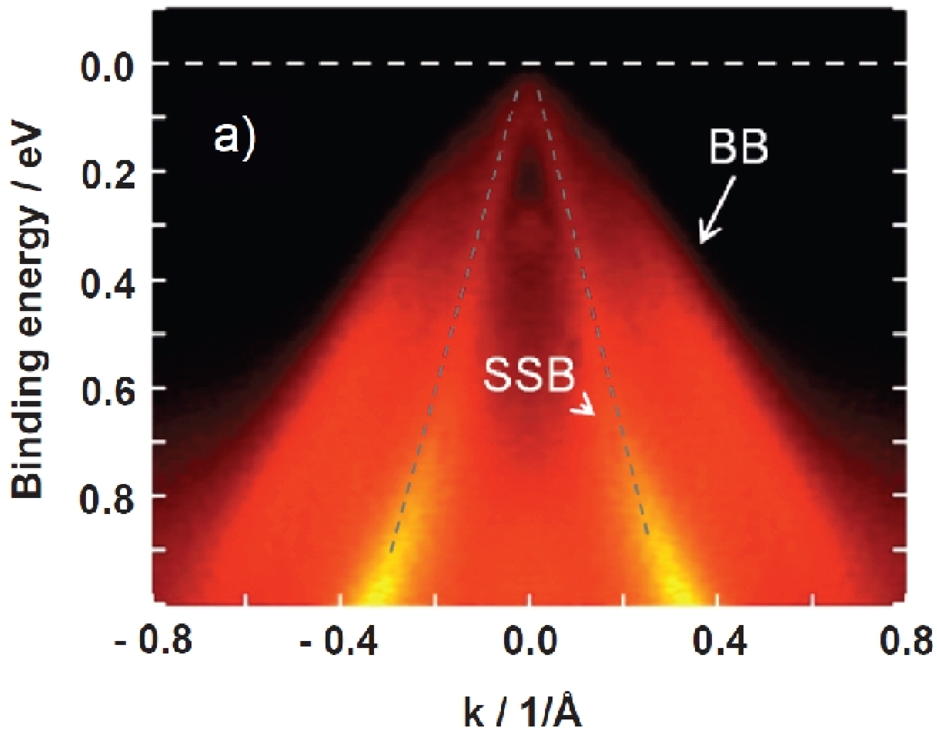


Figure 2.9: Angle-resolved photoemission spectroscopy (ARPES) measurement of a nearly full relaxed 1 μm HgTe layer [37].

Additionally, Fig. 2.10 shows a standard Hall measurement (a) and the corresponding Hall conductivity σ_{xy} (b). The 70 nm fully strained bulk sample shows clear Hall plateaus in the Hall resistance R_{xy} and Shubnikov-de Haas (SdH) oscillations in the longitudinal resistance R_{xx}. The R_{xy} plateaus exists at the same magnetic field where R_{xx} shows a minimum. This are distinct features for a 2D electron system. Furthermore, the filling factors ν have at lower magnetic fields the sequence $\nu = 9, 7, 5$. This is a considerable indication for Dirac-like states of two surfaces. The Hall conductivity in a Dirac system is given by:

$$\sigma_{xy} = m\left(n + \frac{1}{2}\right)\frac{e^2}{h}. \tag{6}$$

Here, m is the number of degenerated Dirac cones and n is the Landau level index. This odd number filling factor sequence is expected for a 3D TI because only the top and the bottom surfaces are affected by the perpendicular magnetic field. The even filling factors $\nu = 4, 2$ at high magnetic fields arise due to the different densities of the two surface systems and the degeneracy of the two systems is removed. This effect is explainable by looking on the layer stack of this sample. So, the HgTe has two different interface conditions on the top and bottom surfaces. On the top, vacuum is connected to the surface state and on the bottom CdTe. This unequal electrostatic environment affects the electron density of both surfaces severally. These lifted degenerate states appear only at higher magnetic fields. Here, the Landau level splitting is large enough to dissolve them separately [37].

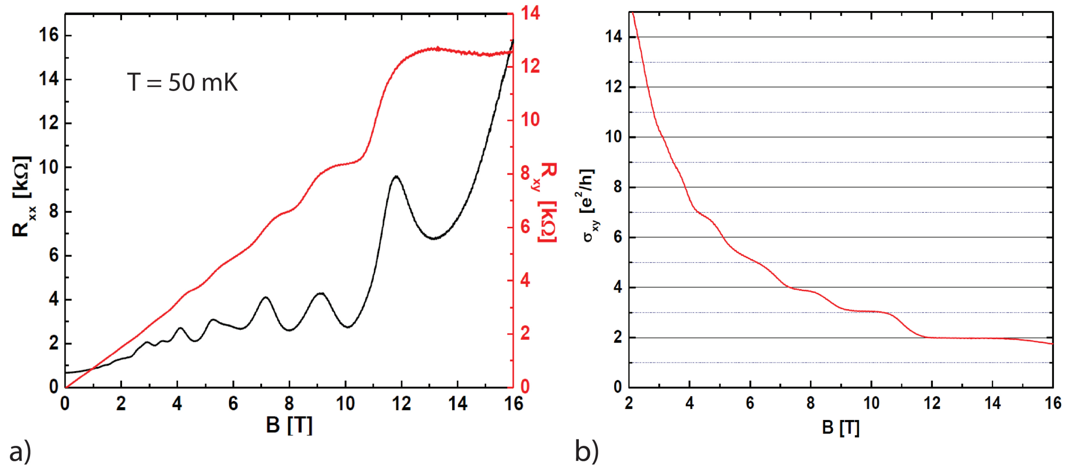


Figure 2.10: a) Hall measurement of an fully strained 70 nm HgTe bulk layer. The longitudinal resistance R_{xx} is plotted in black and the Hall resistance R_{xy} in red. b) Hall conductivity σ_{xy} of a 70 nm thick fully strained HgTe layer [37].

This analyzed 70 nm HgTe sample has the properties of a electron density of n = 8.5×10^{11} cm^{-2} and a carrier mobility of $\mu = 34\,000$ $cm^2V^{-1}s^{-1}$. One important challenge of this thesis was to increase the crystal quality and interface conditions to keep the density the same or even lower and to rise up the mobility. Additionally, it would than be interesting to be capable to modify the carrier density in order to identify the contribution of different Dirac surfaces.

3 Experimental Techniques

In this chapter the main goal is to show and explain setups used for the realization of this work. First, the mode of operation of the MBE is explained, followed by a description of in-situ characterization techniques RHEED and XPS and standard ex-situ characterization setups, as Nomarski Microscopy, HRXRD and AFM. Finally,a short explanation of the lithography process and the sample preparation for the magneto-transport measurements is given.

3.1 Molecular Beam Epitaxy - MBE

Molecular beam epitaxy (MBE) is a multi-purpose technique to deposit thin epitaxial crystals made from metals, semiconductors and insulators, investigated by A.Y. Cho and J.R. Arthur in the late 1960s [39]. Several other methods for thin film epitaxy such as vapor-phase epitaxy (VPE), chemical vapor deposition (CVD), liquid-phase epitaxy (LPE), physical vapor deposition (PVD) or metal organic vapor phase epitaxy (MOVPE) subsist, and the MBE method outperforms these in its precise control of the beam fluxes and growth conditions, the lack of chemical reacting agents and the possibility to control the sample growth in-situ by surface sensitive diagnostic methods like RHEED, AES, or ellipsometry in UHV.

3.1.1 MBE-Setup in the EP III Laboratory

A few month before this thesis started the department Experimentelle Physik III of the University of Wuerzburg acquired a new MBE Riber CMT 32 chamber from Riber/ France to replace the old MBE Riber chamber in order to improve the crystal quality of the samples. By connecting this new chamber to the so-called Modutrak the pressure in this system, which can be reached by pumping with vacuum pumps, is about 10^{-10} Torr. In Fig.3.1, the Modutrack which connects six MBE chambers and several other analysis and technology chambers is shown, so one can transfer samples through this system in UHV without exposure to atmospheric air. So after the resumption of the old CMT - chamber a GaAs, GaMnAs, CT, Heusler and two CMT - chambers are coupled with an XPS, metalization and a sputter chamber. Furthermore there is an option to load or unload the samples over an UHV load lock or a nitrogen box, providing the opportunity to transfer the sample out of the lab without air contamination (UHV box) or preparing the grown structures in nitrogen atmosphere for further experiments (N_2 box).

This large UHV transfer system with several different technology additions is one of only a few world wide and this offers unique possibility for growing sophisticated samples, which are the subject of this thesis.

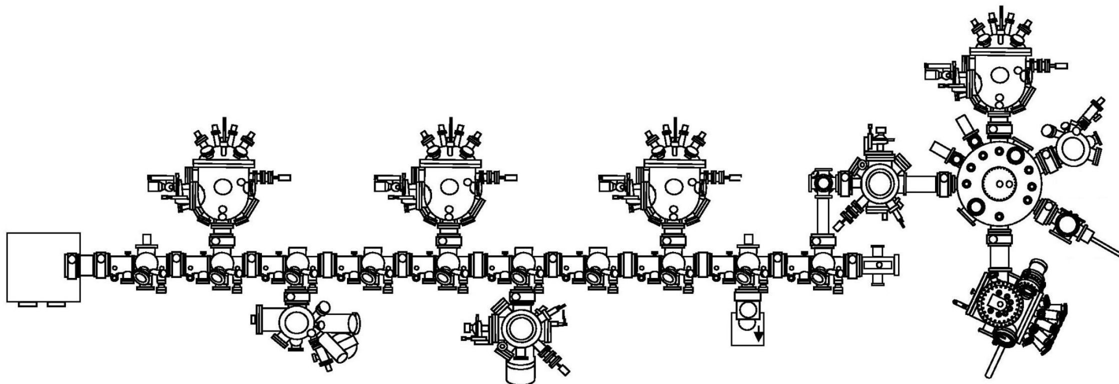


Figure 3.1: Modutrack of the EP III with all MBE, analysis and technology chambers

3.1.2 CMT - Chamber

For Hg-based MBE structures a certain type of MBE machine is necessary to grow epitaxial crystals properly. An obvious difference to all other MBE chambers is that the CMT - chamber is built horizontally whereas all others run in a vertical design, which means that the eight cell ports in the CMT - chamber are adjusted in two horizontal rows, one upon the other. The upper row embeds an angle of 12.11° with the horizontal for the cells 2 and 3 and 33.47° for the cells 1 and 4 and the lower row 40.37° for cell 6 and 7 and 50.05° for 5 and 8. This geometry minimizes the mercury usage [42]. In Fig.3.2 an illustration of the front view, the side view and the top view are shown with legend which enumerates the visible components. In the vertical geometry the cells are arranged in a circle at the bottom of the chamber. Furthermore, only cryo pumps, no turbo molecular pumps, were used in our MBE, which trap gases and vapors by condensing them on a cold surface, here activated carbon cooled to 10 K. Due to the high mercury fluxes during growth [43] this type of pump guarantees a perseverative usage as cryo pumps have no moving components in the UHV in comparison to turbo molecular pumps. In addition self-made cooling traps are mounted in front of the cryo pumps. These cooling traps are cooled with liquid nitrogen (LN_2) and prevent the mercury atoms from reacting with carbon because mercury is a very reactive element and would destroy the activated carbon. Moreover, in the MBE chamber there are three further cooling shrouds, one located at the bottom of the chamber, one around the growth area and one around the cell and shutter feed throughs. As residual gases and surplus material are trapped on these cooling shrouds, a improved vacuum can be provided. At last, a Titan sublimation pump was installed at the bottom of the chamber,

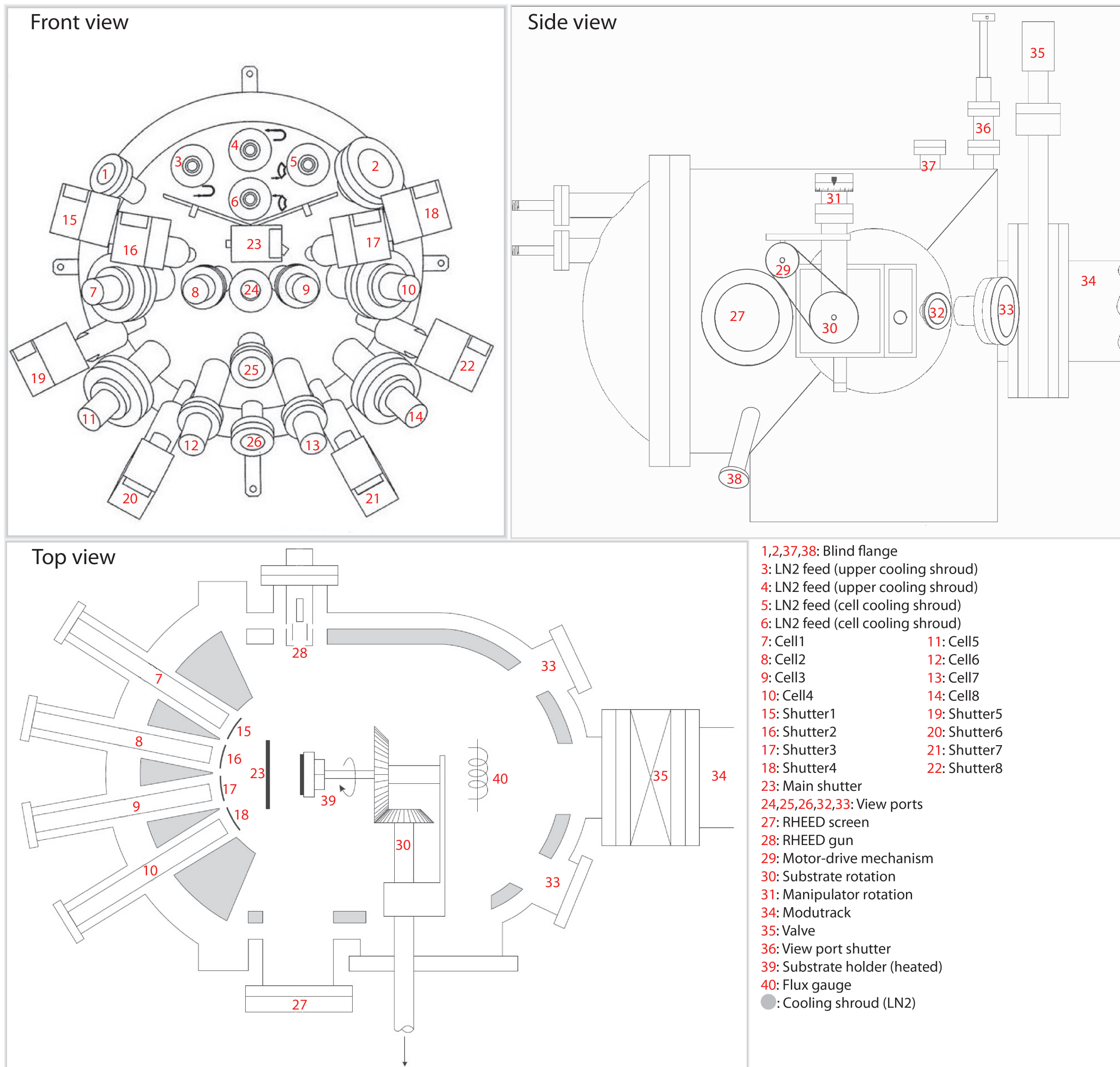


Figure 3.2: Schematic illustration of the Riber CMT 32 MBE chamber. Visible components are numbered and labeled in the adjacent legend. The side view and top view are illustrated in a reduced view in comparison to the front view. (Front view and top view are created in style of [44].

too. On account of the usage of two cryo pumps, three cooling traps, three cooling shrouds and one Titanium sublimation pump the background pressure of the CMT - chamber can be reduced to about 2x10^{-10} Torr. The following listing gives an overview over the other important components of the MBE machine:

- **Effusion cells:** The CMT - chamber is equipped with seven standard effusion cells. Each cell is appointed with the required growth material in a Pyrolytic Boron Nitride (PBN) crucible. These crucibles are surrounded by an electric controlled heating coil, so the temperature of the material and thereby the particle flux can be varied very accurately. The materials of the effusion cells are all solid, so the standard process of evaporating is the sublimation. Fig.3.3 illustrates the schematic sketch of an effusion cell.

- **Shutters:** In front of each effusion cell a shutter is located to stop the relative particle flux to the substrate. The main shutter is mounted near the substrate so the whole particle flux of the cells can be stopped.

- **Hg-cell:** Due to the high mercury flux during growth and the material property mercury is liquid at room temperature, the Hg-cell needs to be equipped with a valve. This means that in order to open and close the cell, a valve is used and no shutter is required. The Hg-cell is a self-made product of the EP III.

- **Substrate holders:** The molybdenum block with the substrate on it is fixed at the substrate holder. For the exact ratio of diffusion and adsorption the substrate holder is heatable and rotatable, which leads to consistent and high quality growth. Furthermore, the substrate holder is swivel-mounted and can thus change between growth, flux and transfer position.

- **RHEED:** A RHEED system, which includes an electron gun and a photoluminescent detector screen, is also installed in the CMT - chamber to control the growth. A closer explanation of the operating mode will be given in chapter 3.1.3.

- **Vacuum Gauges:** The residual gas pressure in the chamber is controlled via three Bayard-Alpert hot-cathode ionization gauges. One is located at the bottom of the chamber, one at the top and the third one is installed at an 90°-angle to the growth direction at the manipulator. To layers with high crystalline quality and very precise thickness the particle fluxes of the materials have to be calibrated by the temperature of the effusion cells.

- **Transfer manipulator and valve:** To avoid contamination of other chambers and samples with CMT materials a valve is installed between each chamber and modutrack. The samples can be passed in and out by the transfer manipulator.

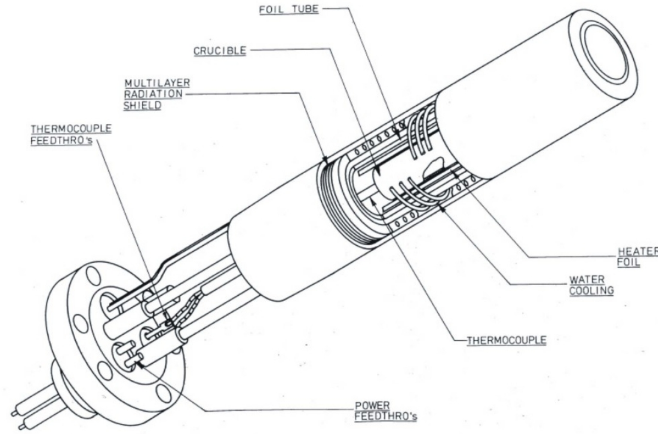


Figure 3.3: Schematic sketch of an standard effusion cell attached to the CMT - chamber

3.1.3 Reflection High Energy Electron Diffraction - RHEED

Reflection High-Energy Electron Diffraction (RHEED) is a common technique used in MBE technique. Its two main advantages are high surface sensitivity and in-situ compatibility with crystal growth. The following short introduction to the RHEED process is based on the works of W. Braun [45] and A. Ichimiya, P.I. Cohen [46].

First of all the RHEED apparatus requires an electron gun, a flat crystalline sample surface and a fluorescent screen. Furthermore, UHV is required for the whole system, so the electrons exhibit a long mean free path. The energy of the electron beam in our MBE system is about 12 keV. Due to the low penetration depth of the beam into the surface of solid state crystals, the de Broglie wavelength of these electrons ($\lambda_{deBroglie} \approx 1.1$Å) and the glancing incidence angle geometry ($2-3^{\circ}$), the electron beam interacts only with a few atomic layers [47] and therefore, RHEED is a very surface sensitive analysis tool. However, some electrons cover a distance of more than a few monolayers. Thereby, multiple scattering occures and the physical interpretation becomes very complex.

Nevertheless, a qualitative analysis of the crystal surfaces and its symmetries can be carried out by observation of the diffraction pattern on the fluorescent screen with the naked eye or a camera setup. The position of the reflections can be easily determined by an Ewald sphere construction and is essential for the diffraction conditions:

$$\triangle\vec{k} = \vec{k}_{out} - \vec{k}_{in} = \vec{G} \quad (1)$$

Due to the fact that RHEED is surface sensitive, the periodicity of the lattice is omitted in z-direction for atomically flat surfaces, also referred to the growth direction. The reciprocal lattice then degenerates into a set of one-dimensional rods along the z-direction, perpendicular to the surface. Using the reciprocal lattice, one gets the Ewald sphere construction used in RHEED which is shown in Fig.3.4. Due to the high electron energy, the radius of the Ewald sphere is more than 50 times larger than the reciprocal lattice unit of CdTe and the Ewald sphere cuts almost planar through the first Brillouin zones of the reciprocal lattice. Since the

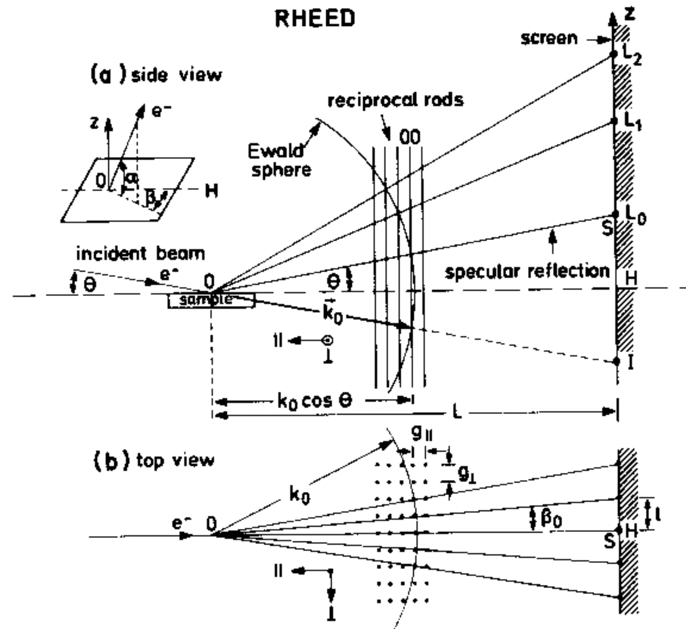


Figure 3.4: Schematic sketch of RHEED

reciprocal lattice consists of continuous rods, every rod produces a reflection in the diffraction pattern. In reality structural defects, thermal vibration or a stepped surface broaden the rods and the Ewald sphere has a finite extension due to the spread electron energy and beam convergence. Consequently, a streaky pattern is generated on the fluorescent screen instead of sharp dots as illustrated in Fig. 3.5. As the surface of a real sample is not a perfect two-dimensional lattice the diffraction pattern is generated in transmission. So transmission-reflection diffraction through surface asperities produces a spotty diffraction pattern on rough surfaces. Thus the difference in diffraction pattern can be utilized to control the current surface condition.

3.1.4 Growth Modes

The composition of the grown layers and the doping concentration are addicted to the flux ratios of the used materials. By reason of deposition of the materials in vacuum the MBE growth does not proceed in thermodynamic equilibrium and is mainly driven by the surface kinematics of the substrate. The most important surface processes are listed in the following [49]:

a) adsorption of the constituent atoms or molecules impinging on the substrate surface

b) surface migration and dissociation of the absorbed molecules

c) affiliation of the involved atoms into the crystal lattice of the substrate or the epilayer which has already grown

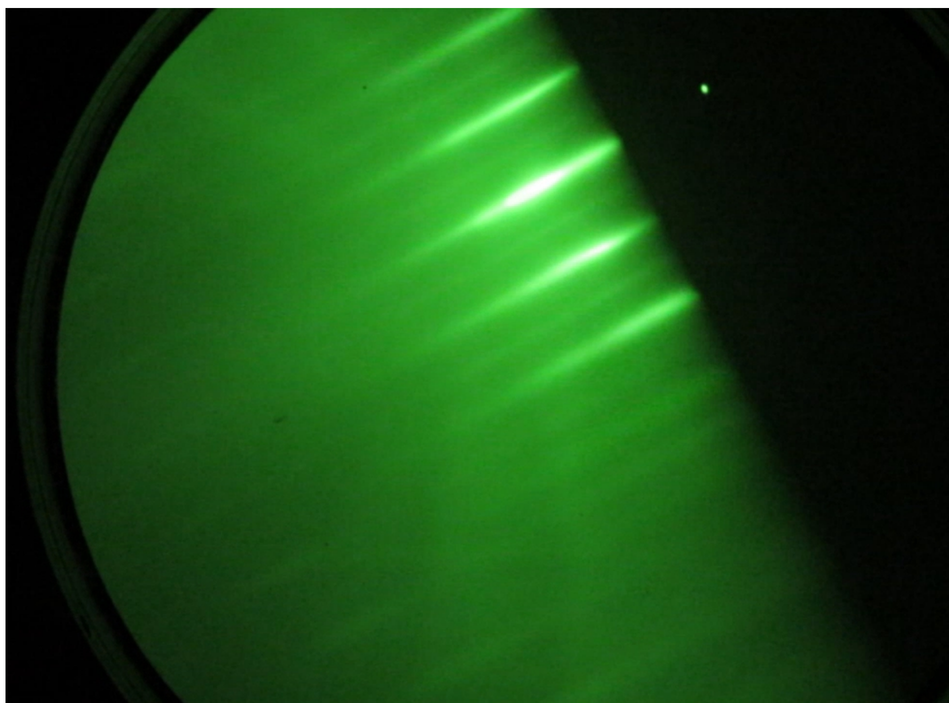


Figure 3.5: RHEED picture of 2x1 reflection of CMT

d) thermal desorption of the molecules which are not incorporated into the crystal lattice site.

These processes are illustrated in Fig.3.6. When the gaseous materials impinge on the substrate they are physisorbed before they are chemisorbed into the crystal. As long as the particles are not incorporated they can freely diffuse on the substrate surface. The atom or molecule can find a suitable, energetic favorable lattice site which is reachable within a certain diffusion length. The atoms which do not find a convenient lattice site either desorb directly after arrival or after larger diffusion lengths on the surface. To sum up it is possible for some atoms or molecules at certain growth parameters to accumulate on the substrate surface (nucleation) or to switch sites with atoms which are already incorporated in the crystal (interdiffusion).

One distinguishes between three growth modes shown in Fig.3.7. If atoms or molecules of the deposit are more strongly bound to each other than to the substrate, the so called Volmer-Weber growth leads to the formation of three dimensional adatom clusters or islands. The growth of these islands causes rough multi-layers on the substrate surface and a three dimensional, spotty RHEED.The Frank-van der Merwe mode demonstrates the opposite characteristics. Adatoms prefer attaching to surface sites forming atomically smooth layers, because the atoms are more strongly bound to the substrate than to each other. In this layer-by-layer growth mode complete films are formed prior to growth of successional layers appearing as streak pattern on the RHEED screen. The Stranski-Krastanov, or layer-plus-island, growth mode is an intermediary process. At a critical thickness a transition from Frank-van der Merwe to Volmer-Weber growth takes place because after forming the first or a few monolayers (wet-

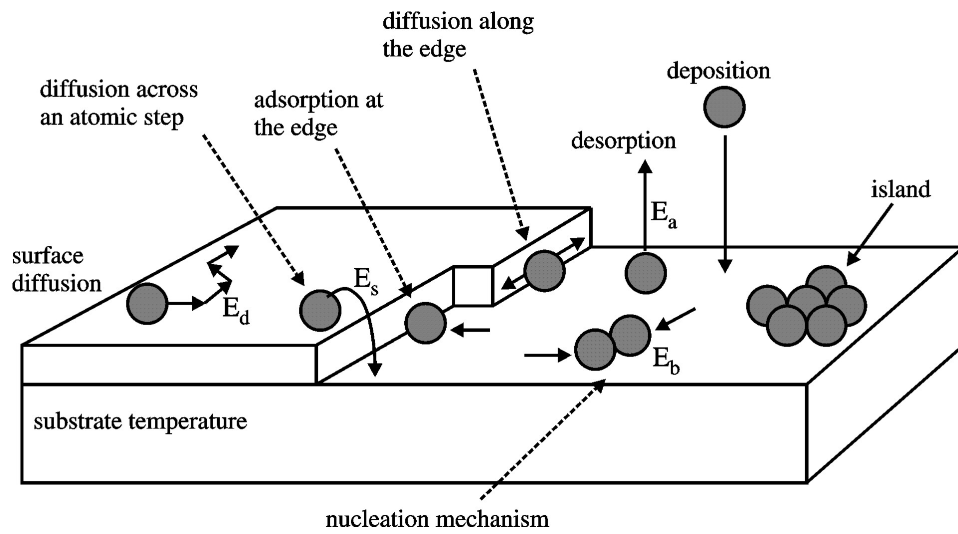


Figure 3.6: Illustration of the growth processes occurring on the substrate surface during MBE growth.

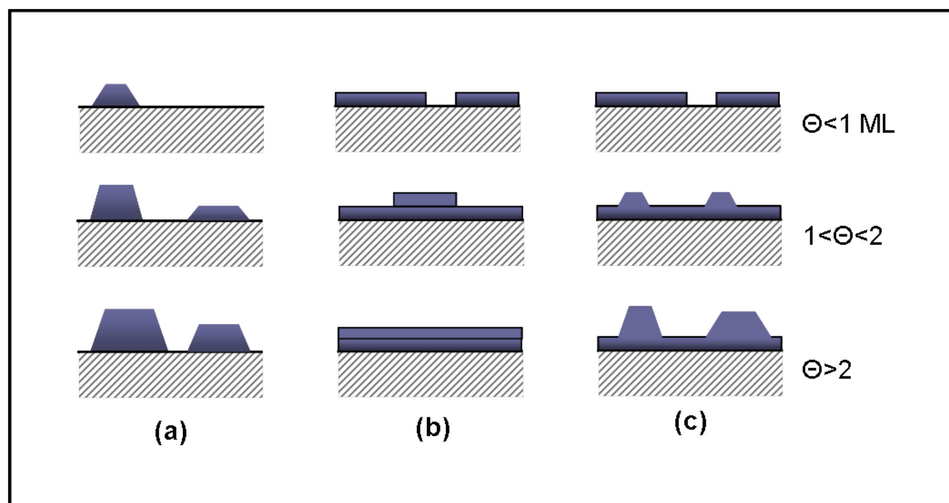


Figure 3.7: Schmetic sketch of the three standard growth modes including (a) Volmer-Weber (Island growth), (b) Frank-van der Merwe (layer-by-layer growth), (c) Stranski-Krastanov (layer-plus-island). Θ represents the coverage in monolayers.

ting layer) the adatom-adatom interaction becomes stronger than the bond of the adatom with the wetting layer. Here chemical and physical properties of the lower crystal, such as surface energies or lattice parameter, play a major role. The RHEED is a mixture of streaks and well defined spots. The requested growth mode in this thesis is the layer-by-layer growth to get nice, sharp HgTe quantum wells and bulk layers.

3.2 Analyzing Apparatuses

In the following an introduction and explanation of the tools which were used to analyze the samples outside the MBE chamber will be given. XPS is hereby the only one which can be used in-situ, whereas all other techniques operate in atmospheric air pressure so the sample contaminates and oxidates as soon as the sample is outside the UHV system. Therefore, a very accurate handling of the samples is essential.

3.2.1 X-ray Photoelectron Spectroscopy - XPS

An additional in-situ application besides RHEED is the X-ray photoelectron spectroscopy (XPS) to investigate the sample surface. This setup is attached to the UHV-Modutrack-system. The build up of an XPS spectrometer is much larger than an RHEED setup, so it is not comfortable to operate this setup directly in the growth chamber. The XPS analyzes the surface by irradiating the sample with mono-energetic soft X-rays and deconstructs the energy of the emitted electrons. These electrons have an exit length out of the crystal of only a few monolayers and therefore this analysis technique is very surface sensitive.

In our system the Magnesium-K_α (1253.6 eV) and Aluminum-K_α (1486.6 eV) X-rays were used as excitation wavelengths [50]. Due to their high energy these photons penetrate the solid only in a distance of micrometers. The physics behind this measuring apparatus is based on the photoelectric effect. The X-rays interact with the atoms the solid but only the surface near electrons are emitted because they react more likely with atomic nuclei and electrons of the crystal. The kinetic energy of the released electrons is given by:

$$E_{kin} = E_{photon} - E_b - \phi \tag{2}$$

E_{photon} is the energy of the incoming photon, E_b the binding energy of the atomic orbital where the electron is coming from, and ϕ is the work function of the spectrometer which is an adjustable instrumental correction factor.

Only the emitted electrons, which actually escape from the sample into the vaccum can be detected by an electron energy analyzer. The analyzer can be adjusted by electrostatic lenses and counter-voltages so that only electrons with a certain kinetic energy can pass through. Consequently, the electrons from inner layers collide with other atoms on their way into the vacuum. The kinetic energy decreases and these electrons are counted to the background intensity. Furthermore, the attained electrons are detected by an electron multiplier. A spectrum in which the intensity or count rate is plotted over the binding energy is shown in Fig.3.8. Here, a typical XPS spectrum of a CdTe buffer on GaAs:Si is demonstrated which is etched by HF.

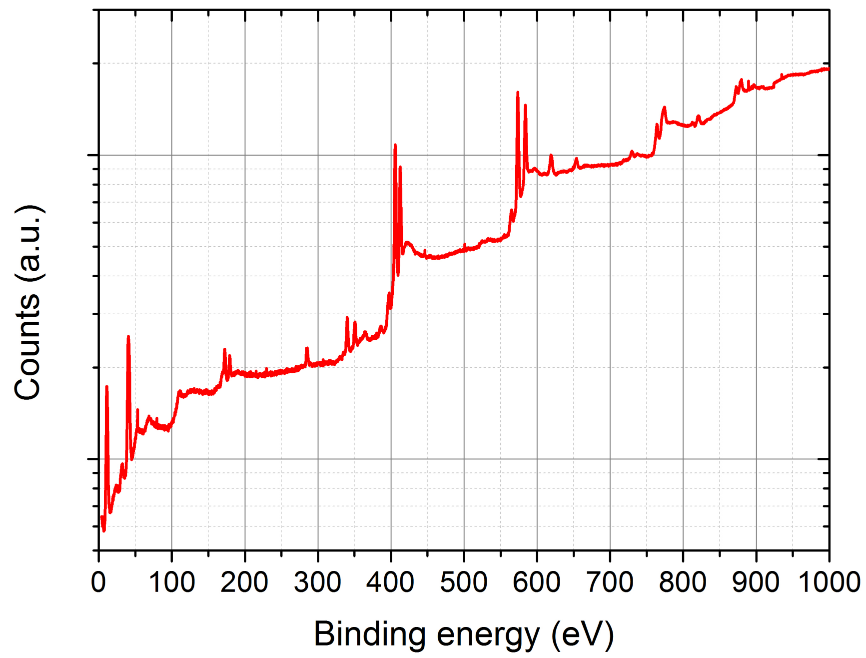


Figure 3.8: XPS measurement of an CdTe substrate etched for 30 seconds in HF. The energy range of about 400 eV to 600 eV is the interesting area for analyzing Cd- and Te-shifts due to chemical binding energy and oxidation behavior.

The interesting area of the graph for this thesis is between 400 eV and 600 eV. Here, one can clearly evaluate the Cadmium $3d_{5/2}$ (405 eV) and $3d_{3/2}$ (412 eV), the Tellurium $3d_{5/2}$ (573 eV) and $3d_{3/2}$ (583 eV)and the Oxygen 1s (531 eV) orbital peaks. This leads to meaningful achievements in matters of chemical composition and oxidation of the surface layers.

All measurements were performed by the Mg-K_α wavelength.

3.2.2 Differential Interference Contrast Microscopy

The Differential Interference Contrast (DIC) Microscopy, also known as Nomarski Microscopy, is an optical microscopy illumination technique used to take a picture of the grown structure to analyze the surface constitution in relation to surface contamination, big growth defects and an approximate rating of the surface roughness.

A polarizer after a white light source is used to set the angle of the polarized incident light on the Wollaston prism, as shown in Fig.3.9. The light is split by the Wollaston prism into two beams with perpendicular polarizations. After reflection on the sample surface the Wollaston prism recombines the two beams and a fixed analyzer behind it transmits the components of the two polarizations and generates an interference picture.

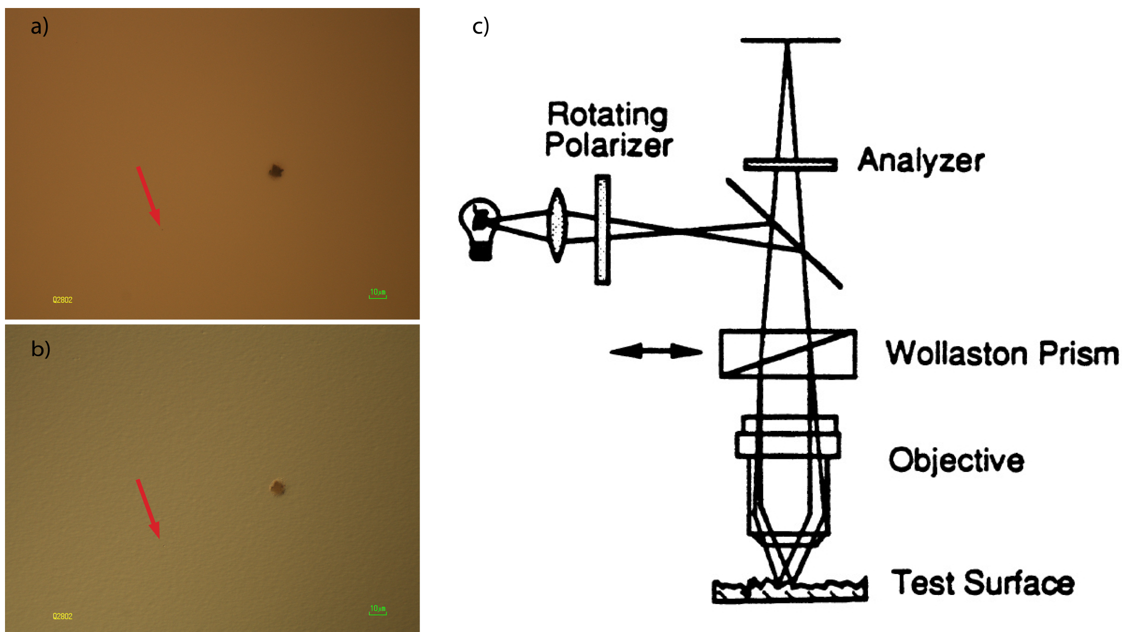


Figure 3.9: a) Picture without Nomarski optics at 50 times magnification; b) Picture with Nomarski optics at 50 times magnification; one can clearly see the roughness in b) is superiorly to detect than in a) and furthermore some defects which are marked with the red arrows are slight easier to discover with Nomarski optics.In c) a sketch of the Nomarski microscopy apparatus is shown with the optical path.

The resulting pattern shows the difference between two closely spaced points on the sample

surface. The point separation is usually comparable to the optical resolution of the microscope objective. However, because DIC utilizes optical path differences within the specimen to generate contrast the three-dimensional appearance may not represent reality. In other words the 3-D relief of DIC imaged specimens is an optical rather than a geometric relief [51].

3.2.3 High Resolution X-ray Diffraction - HRXRD

The most important measurement technique for ex-situ characterization of epitaxial layers is High Resolution X-ray Diffraction (HRXRD). This non-destructive analysis technique yields detailed information on crystallographic structure, chemical composition, strain situation and layer thickness. A Philips X'Pert system was used for standard characterization with a 4-crystal Ge(220) Bartels monochromator and a 2-crystal analyzer. Fig. 3.10 shows a sketch

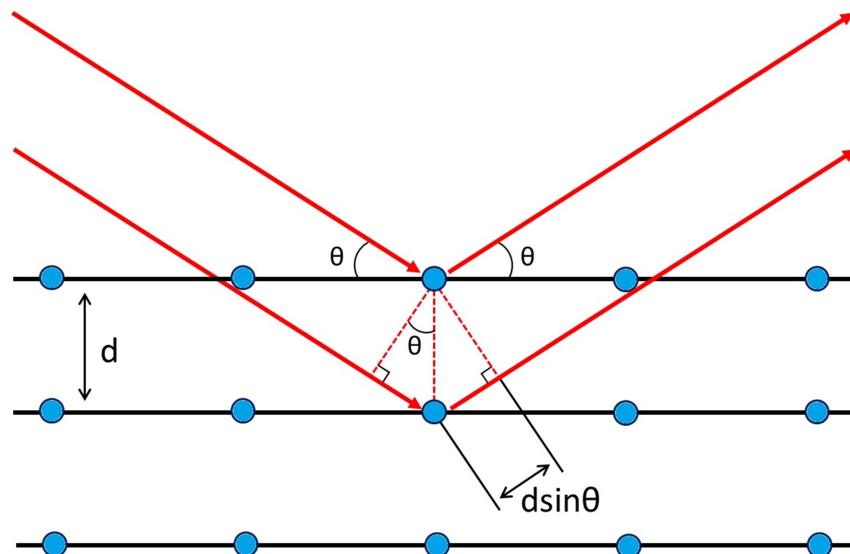


Figure 3.10: Geometrical illustration of Bragg's law. Due to the reflection on the parallel lattice planes the incident coherent X-ray beam is diffracted and the result is constructive or destructive interference.

of the diffraction geometry. Diffraction occurs when the distance of the lattice planes of the diffraction grating is in the order of the used wavelength. The wavelength of X-rays is in between the range of picometer to 10 nanometer, which corresponds to the distance between the lattice planes of the crystal. The waves which are diffracted at the electron shell of the atoms interfere with each other. Depending on the distance of the lattices planes different optical path differences are the result of the diffracted X-ray waves and therefore, one can observe constructive or destructive interference at a certain diffraction angle. Mathematically,

the scattering condition is described by Bragg's law [49],[52]:

$$2 \cdot d \cdot sin\theta_B = n \cdot \lambda \tag{3}$$

Here, d is the distance between the parallel lattice planes. θ_B is the angle of incidence, n an integer number in the order of the analyzed maximum and λ the wavelength of the X-rays. The lattice planes are generally identified by the Laue conditions (h,k,l). For the cubic system $Hg_{1-x}Cd_xTe$, d_{hkl} is calculated with the following equation [53]:

$$d^2{}_{hkl} = \frac{a^2}{h^2 + k^2 + l^2} \tag{4}$$

ω - 2Θ - Scans

In an $\omega - 2\Theta$-scan the sample stage and the detector are both varied, while the detector (2Θ) is moved twice as fast as the sample (ω). So, in a sample with multiple layers a high intensity peak can be correlated to the corresponding peak in an $\omega - 2\Theta$-scan because by changing the incident beam angle Bragg´s law conditions for other lattice parameters are complied and therefore, an $\omega - 2\Theta$-scan is often used to analyze samples with several layers of different compositions. Fig.3.11 shows an $\omega - 2\Theta$-scan of the (004) reflection of a HgTe layer on CdTe. This reflection is called symmetric because the diffracting lattice plains are parallel to

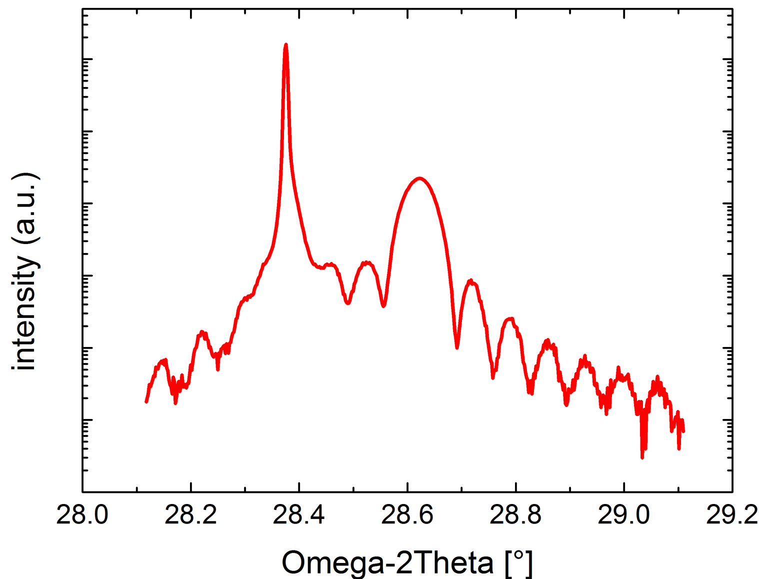


Figure 3.11: $\omega - 2\theta$ - scan of an (004) reflection of HgTe on CdTe.

the sample surface. In these diffractograms one receives only information about the vertical lattice constant due to the fact that only the l reciprocal direction plays a role in the formula

for d_{hkl}, while h and k are zero. The distance of the lattice plains of the (004) reflection is $\frac{1}{4}$ of lattice constant according to equation 4. Asymmetric reflections are reflections where the lattice planes are not parallel to the sample surface. These reflections imply data of two or all three spatial dimensions, contingent on the specific reflection.

For this thesis $\omega-2\Theta$-scans were only performed on the symmetric (004) reflection. Due to the Bragg angle Θ_B of the CdTe substrate and the $Hg_{1-x}Cd_xTe$ layer it is possible to find out the composition of the $Hg_{1-x}Cd_xTe$ layer, as long as the layer is completely strained or completely relaxed. Otherwise, the layer is in a condition with two unknown parameters. Partly relaxed layers can easily be analyzed by reciprocal space mapping as explained in the following section.

In addition to the composition analysis one can obtain the layer thickness, which is also an indication of high interface and layer quality. As shown in Fig.3.11 there is a large number of additional small peaks, thickness oscillation peaks, whose period is defined by the thickness of the HgTe layer. So-called interface fringes have their origin in the different optical path lengths of the X-rays occurring through multiple refraction of the X-ray beam between the top and bottom interface of the layer. From Bragg equation 3 one can determine the thickness fringe peak positions n_1,n_2,n_3,...etc, and determine a characteristic length scale L. So there are two equations for scattering from planes parallel to the surface:

$$2 \cdot L \cdot sin\Theta_1 = n_1 \cdot \lambda \tag{5}$$

$$2 \cdot L \cdot sin\Theta_2 = n_2 \cdot \lambda \tag{6}$$

So the layer thickness L is finally given as:

$$L = \frac{(n_1 - n_2) \cdot \lambda}{2 \cdot (sin\Theta_1 - sin\Theta_2)} \tag{7}$$

The analysis of these fringes is a possibility to determine the thickness of an MBE grown layer and its growth rate, because the growth time of the layer is usually known. Furthermore, the composition of the layer $Hg_{1-x}Cd_xTe$ can easily be calculated by applying the Vegard´s law [54]. The lattice constant of the alloy is a linear interpolation between the lattice constants of HgTe and CdTe:

$$a_{Hg_{(1-x)}Cd_xTe} = a_{CdTe} \cdot (1-x) + a_{CdTe} \cdot x \tag{8}$$

Reciprocal Space Map - RSM

Because $\omega-2\Theta$-scans of the (004) reflection can only give information about the vertical lattice constant $a_\perp$, as shown in the prior section, there is the method of reciprocal space map (RSM) around an asymmetric reflection which allows to analyze the horizontal and the in-plane lattice constants $a_\parallel$ as well. A common use is the determination of the relaxation degree of stressed layers [53, 57].

In Fig.3.12 a two-dimensional pattern of the reciprocal lattice in the diffraction plane is shown. The colored dots represents schematically the position of the peaks in the reciprocal space for different strain conditions. The crystal lattice of the substrate has a cubic unit cell

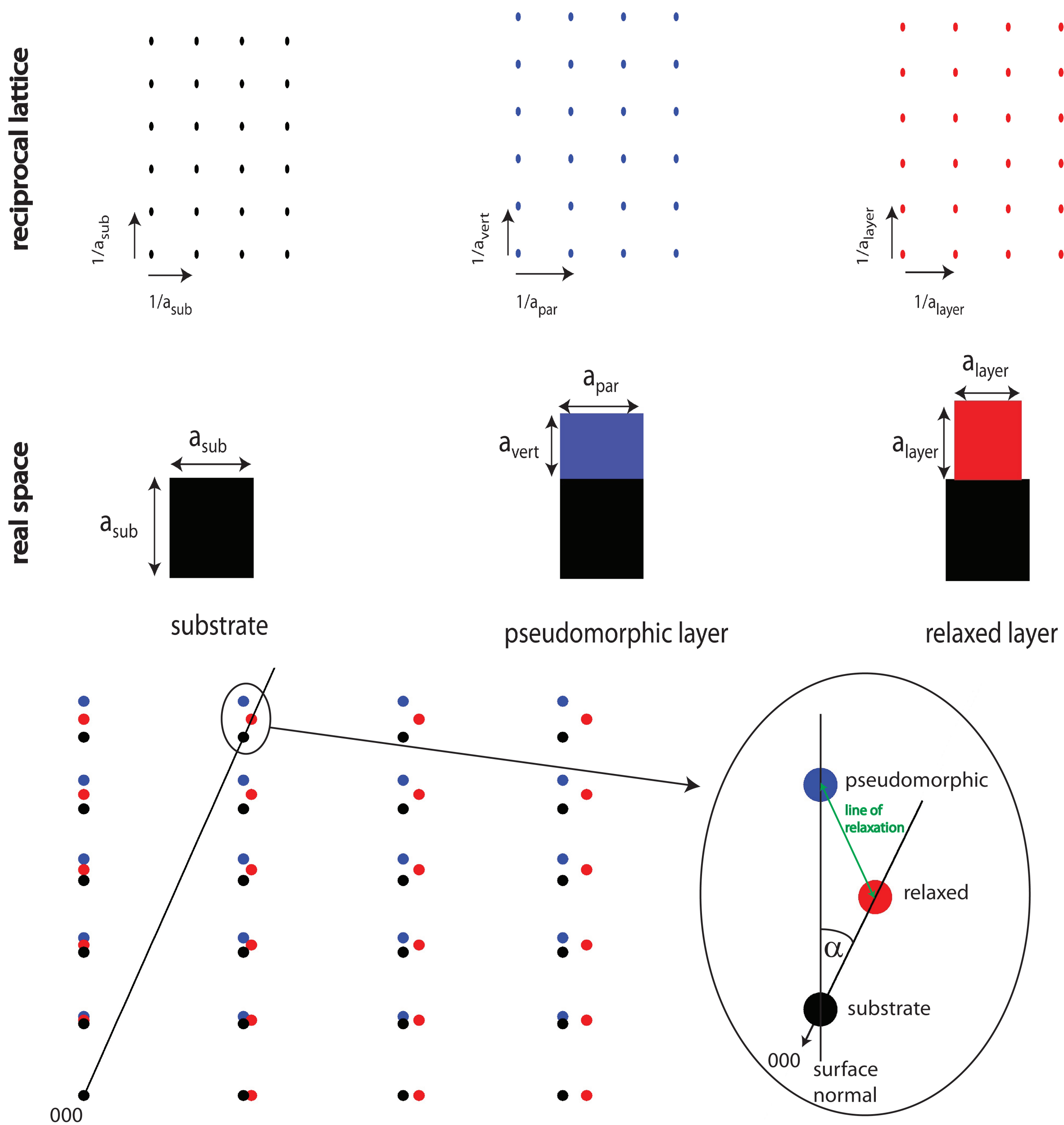


Figure 3.12: Upper part: Schematic sketch of the reciprocal lattice for a cubic substrate (black), a pseudomorphic, fully strained (blue) and a fully relaxed cubic layer (red). Lower part: Combination of all above three cases and the zoomed area refers to the asymmetrical (115) reflection and corresponding relaxation triangle.

and the lattice constant a_{sub}. The corresponding reciprocal lattice exhibits a cubic symmetry as well. The reciprocal lattice constant is therefore given by $1/a_{sub}$. The materials which were grown for this thesis by MBE differ generally in their lattice constants a_{layer}. If the difference of both lattice constants, also called lattice mismatch, is relatively small, usually an epitaxial layer grows initially completely strained on the substrate. The lateral lattice constant of the layer a_{lat} is the same as the lattice constant of the substrate, $a_{lat} = a_{sub}$. This condition of the layer is called pseudomorphic. The in-plane distortion of the layer is compensated by a change of the lattice constant in growth direction a_{vert}. The cubic unit cell of the layer is so deformed tetragonally due to the Poisson effect. An epitaxial layer is then critically thick when the stored strain energy is sufficient to form a dislocation. The lattice mismatch is released by the assembly of dislocations. When at some point the layer is fully relaxed, it has reached its natural lattice constant a_{layer} and cubic unit cell structure. Besides relaxation of the layer the creation of point defects, stacking faults and hillocks can also lead to a disordered crystal.

In the lower part of Fig. 3.12 the combination of three reciprocal lattices is shown relatively to each other for different reflections. The zoomed region of the (115) reflection is exemplary selected to explain the process of relative peak positions a pseudomorphic and relaxed layer compared to the substrate. These selected region shows the three peaks which form the extrema of the so-called relaxation triangle and the line between a pseudomorphic and a relaxed layer which is called the line of relaxation. The black spheres stand representatively for the substrate (CdTe) and for the layer, e.g. HgTe, the red and blue spheres are used. The (115) reflection is chosen due to the highest intensity of all allowed asymmetric reflections of these material system. Due to the fact that the transition from the pseudomorphic state to the fully relaxed state does not occur abruptly, the Bragg peak of a partially relaxed layer is located on the line of relaxation between the two cases, depending on the degree of relaxation. The peak of a fully relaxed layer is at the intersection of the line of relaxation and the line coming from the (000) reflection. Conditional on the geometry of the $\omega - 2\Theta$-Scan of an asymmetric reflection the surface normal and reflecting plane do not stand perpendicular to each other and the angle between is given for h = k by:

$$tan(\alpha) = \sqrt{2}\frac{h}{l} \tag{9}$$

This leads to an angle α of 15.79° between the line through origin of the (115) reflection and the surface normal. The degree of relaxation is defined as the ratio of the in-plane $\triangle a_{\|}$ and the relaxed $\triangle a_{rel}$ lattice mismatch referred to the substrate and this is direct proportional to the angle between the surface normal and the peak of the layer compared to the angle between surface normal and line through origin:

$$\gamma = \frac{\triangle a_{\|}}{\triangle a_{rel}} = \frac{a_{\|} - a_{sub}}{a_{rel} - a_{sub}} = \frac{\alpha}{\alpha_{LTO}} \tag{10}$$

For $\gamma = 0$, it is the pseudomorphic, fully strained state and for $\gamma = 1$, it is the fully relaxed state. Therefore the relaxation triangle is a very important instrument to analyze strained layers [58, 59, 61].

To get a undistorted presentation of an RSM the angles ω and 2θ have to be converted into coordinates of the reciprocal space q_x and q_y and arise out of the incidence and emergent angle

ω_i and ω_e through following transformation:

$$q_x = \frac{1}{\lambda}(cos\omega_e - cos\omega_i) \tag{11}$$

$$q_y = \frac{1}{\lambda}(sin\omega_e + sin\omega_i) \tag{12}$$

This transformation leads to a simpler presentation of RSMs to work with.

Furthermore it is important to mention, all HRXRD measurements were done relatively related to the known lattice constants of CdTe and GaAs substrates, so the resulting values are not generally normalized.

3.2.4 Atomic Force Microscopy - AFM

Atomic force microscopy is a very high resolution type of scanning probe microscopy, which allows to determine the surface topography of the grown layer up to atomic resolution in z-direction. In the 1980s Binning *et al.* [62] developed the AFM after the scanning tunneling microscope (STM) and it turned out that the AFM is more flexible in usage as STM, because it can be used on one hand under ambient air conditions and on the other hand on both conducting and insulating samples. However, the resolution is usually a little bit lower [63].

A schematic setup of AFM is presented in Fig.3.13, consisting of a fine, sharp tip mounted on a cantilever, a laser beam, piezoelectric elements, a detector and controller. There are two types of scanning modes. Firstly there is the DC mode (contact mode), in which the cantilever touches the surface and the force is kept constant. Secondly one can use the AC mode (non-contact mode), which is the standard mode and the only one used in this thesis. Here the cantilever is permanently excited to its resonance frequency and in close proximity to the layer surface (few nanometers) the cantilever oscillations will be changed due to the van-der Waals force. This change in oscillations will be registered by the detector via laser beam. The data of the detector is continued processing by a computer software which displays a colored image. The gradient of the color is an indication of altitude differences. piezoelectric elements attached in the scanning head move the cantilever across the surface in x and y direction. So combined with the measured altitude profile of the layer surface, a three dimensional colored image of the surface is generated. To prefocussing a CCD camera is installed in the scanning head for simpler adjustment the sample and scanning head by micrometer screws.

The effective radius of the curvature of the tip is the limiting factor of the measuring. New tips are specified to be below 10 nm and so one can resolve holes and valleys with diameter larger than 20 nm. Therefore the x and y resolution is limited by the effective tip radius and the step size accuracy of the piezoelectric elements positioning after every line scan.

The root mean square (RMS) is used for characterization and comparison of the analyzed layer surfaces. A manually selected area is read out by the AFM software which calculated the RMS by the following definition:

$$\mathrm{RMS} = \sqrt{\sum_{n=1}^{N} \frac{(Z_n - \overline{Z})^2}{N}} \tag{13}$$

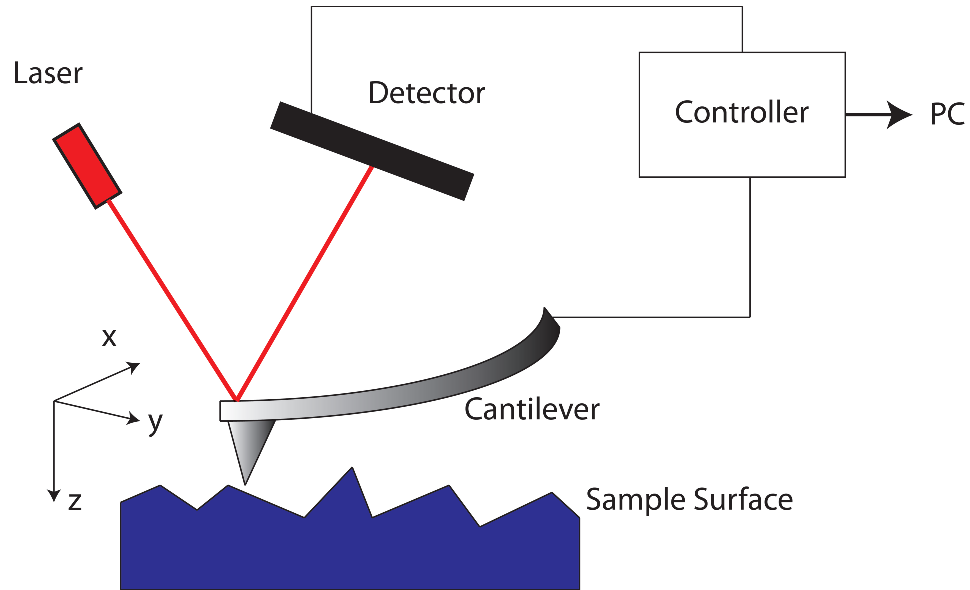


Figure 3.13: Sketch of an AFM setup.

where n represents a single data point, Z_n the z-value of that point and $\overline{Z}$ is the average of all z-values of the selected area [64]. So RMS depends only on the value of each data point and not on the surroundings. Thus there is no possibility to distinguish different topographies and bigger values have larger impact on RMS due to squared data point use. Therefore a few points with very large altitude values can make a big difference in RMS. So it only makes sense to interpret and compare surface roughness of different layers with similar topography and without surreal deviating data points. Furthermore size of scan range and scan speed influence RMS indirectly because of the impact on the measurement. In conclusion, the samples should be measured with the same scan parameters.
All measurements in this thesis were done on a DME DualScope^{TM} DS 95-50/200 in combination with the associated software (DualScope^{TM}/Rasterscope^{TM} SPM Version 2.3.0.6).

3.3 Microstructuring and Electronic Transport Measurements

After MBE growth and standard characterization by Nomarski microscope, AFM and HRXRD the heterostructures have to be processed for further electronic transport characterization. Standard Hall bar geometry as sample design and a conventional helium bath cryostat are used for these transport measurements about the following section is giving a short overview.

Lithography

To the fabrication of different sample structures optical or electron beam lithography are resorted depending on the structure size. In this thesis only structures down to 10 μm are processed via optical lithography. A typical complete processed sample is shown in Fig.3.14 with dimensions for the large included. For smaller, special designed structures one have to use electron beam lithography. A standard optical lithography process starts with coating a resist on the heterostructure and exposing thereof through a mask with UV light (mercury-vapor lamp). The used Hall bar geometries have the dimensions (600 x 200) μm^2 and (30 x 10)

Figure 3.14: Microscope picture of a structured sample.

μm^2. After removing the unexposed resist[1] the mesa[2] structure can be etched either via wet chemically, using a potassium iodide-iodine-hydrogen bromide-mixture (KI:I:HBr), or dry chemically with ion beam etching (argon ions). The lift-off process removes the remained resist. To get ohmic contacts, resist is coated for a second time and exposed on selected contact areas. After developing, a gold-germanium (Au/Ge) layer stack is evaporated and during the lift-off process the resist is removing the metal lying on these resist. The metal is now only connected to the mesa where no residual resist was located. Only the evaporation of the metal is effective to contact a normal 2DEG or capped bulk structure in certain depth because the metal diffuses into the heterostructure based on thermal excitation[65].

Furthermore it is possible to add an isolator on the mesa coated with an gold-titanium (Au/Ti)top gate. The complete processed sample is then glued into a normed chip carrier.

[1] There are two types of exposure, the positive and the negative process. These differ in which part of the resist is removed during the development process. The positive process is described in the text.

[2] Mesa: defined geometry of the sample

The on-chip contacts are bonded to contact pads on the chip carrier by ultrasound bonding with Au wires. Deviant sample structures are explicitly explained in the following chapters.

Measurement Technique Setup

The chip carrier with the bonded sample is then inserted into a cryostat for low temperature electronic measurements. ^{4}He bath cryostats are used which are different in their maximal end temperature as well as in the magnitude of the applied magnetic field. The two cryostats, which provide a magnetic field up to B = 5 T or B = 16 T, respectively, enable a measurement temperature of T = 4.2. K which is the temperature of ebullition of ^{4}He at atmospheric pressure. Here the sample couples directly to the helium bath via the exchange gas He. Contrariwise a so called 1K-pot is installed in the cryostats with maximal attainable magnetic fields B = 7 T and B = 10 T. As one sees in Fig.3.15 (a), a schematic sketch of the 10 T cryostat, the 1K-pot can be pumped down by a rotary vane pump so the boiling point of the operating ^{4}He can be reduced due to the partial vacuum. This leads to the result that the possible temperatures can

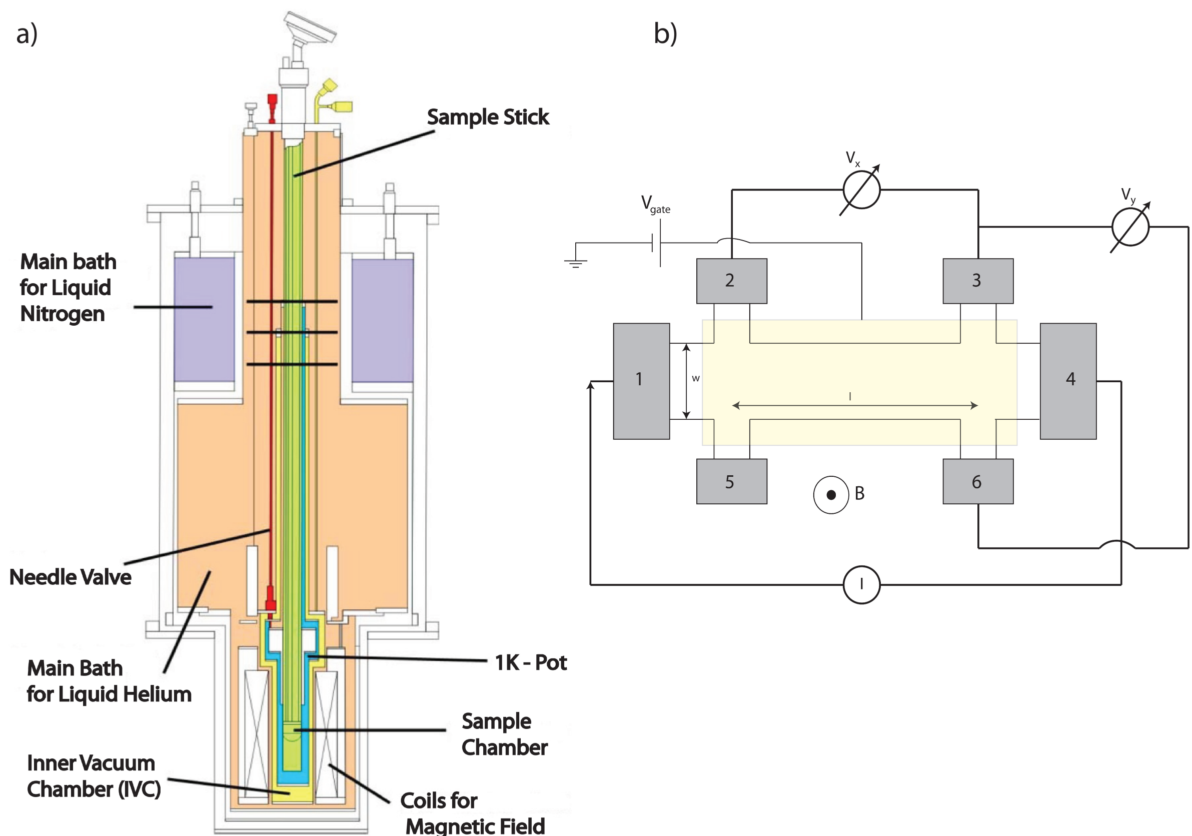


Figure 3.15: a) Schematics of the 10T cryostat. b) Simplified drawing of the measurement configuration after [60].

hold steady at T_{10T} = 1.4 K and T_7T = 1.8 K. For further and more precise setup information

several diploma thesis and dissertation are advised [67, 68, 69, 70].

A circuit diagram of a measuring setup for a DC-setup is shown in Fig.3.15 (b). As excitation voltage either an analog voltage output card or an external voltage generator are used. The principle of six-point-geometry is utilized for all measurements. This means that the voltage measuring is not taken on the contacts which carries the current, but on the contacts which are applied additionally on the sample. This leads to the Hall bar geometry. So because a currentless measurement of the voltage takes place on these contacts, possible additional resistances due to the contacting of the Hall bar have no influence on the result. For measuring the current through the sample a known resistance is destined as reference and is connected in series with the sample. By voltage measurement, the current through the reference resistance and also through the sample can now be determined.

Because all samples should have a two dimensional electron gas, the appearance of the quantum Hall effect can be detected and additional with the geometry the carrier concentration n_s and the carrier mobility μ can be calculated out of the measurands V_x, V_y and the sample current I. The Hall resistance is than defined as:

$$R_{xy} = \frac{U_y}{I} \tag{14}$$

Via Drude theory of electrons in conducting materials characteristic factors can be calculated out of the transport measurements. However there are some false assumptions which were enhanced by Sommerfeld [63, 71, 72].

In two dimensions the current density $\vec{j}$ can be linked with the electric field $\vec{E}$ over a 2 x 2 - tensor σ(B) which is magnetic field dependent:

$$\vec{j} = \begin{pmatrix} j_x \\ j_y \end{pmatrix} = \sigma(B) \cdot \vec{E} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ \sigma_{yx} & \sigma_{yy} \end{pmatrix} \cdot \begin{pmatrix} E_x \\ E_y \end{pmatrix}. \tag{15}$$

After the theory of Sommerfeld the conductivity tensor has the form after [66]

$$\sigma(B) = \frac{\sigma_0}{1 + (\omega_c \tau)^2} \begin{pmatrix} 1 & -\omega_c \tau \\ \omega_c \tau & 1 \end{pmatrix} \tag{16}$$

with

$$\sigma_0 = \frac{n_s e^2 \tau}{m^*} \tag{17}$$

Furthermore $\omega_c = eB/m$ is the cyclotron frequency and τ is the scattering time.

With these equations the Hall voltage U_y can be determined with the current in x-direction and the magnet field in z-direction by [63]:

$$U_y = \frac{I_x \cdot B_z}{n_s \cdot e} \tag{18}$$

Together with equation 14 the Hall resistance is defined as:

$$R_{xy} = \frac{U_y}{I_x} = \frac{B_z}{n_s e} \tag{19}$$

Hence there is a linear dependence on the magnetic field and so an easy determination of the carrier density n_s is possible in samples with Hall bar geometry. The physical values as carrier density n_s and mobility μ provide a basis for characterization and comparability of the samples. The mobility is here connected with the conductivity as follows:

$$\sigma_{xx} = n_s e \mu \tag{20}$$

By inverting equation 15 the tensor of the specific resistance in two dimensional structures can be calculated with eq.16 to:

$$\rho(B) = \sigma(B)^{-1} = \frac{1}{\sigma_0} \begin{pmatrix} 1 & \omega_c \tau \\ -\omega_c \tau & 1 \end{pmatrix} \tag{21}$$

By reason of ρ_{xx} = ρ_{yy} and ρ_{xy} = -ρ_{yx} it is notably true as well:

$$\sigma_{xy} = \frac{\rho_{xy}}{\rho_{xx}^2 + \rho_{xy}^2} \tag{22}$$

Therefore it is sufficient that one is measuring longitudinal resistance R_{xx} and Hall resistance R_{xy} for calculating the Hall conductivity. Due to the Hall bar geometry the electrical resistivity is dependent on the longitudinal resistance by following equation:

$$\rho_{xx} = R_{xx} \frac{w}{l} \tag{23}$$

where w is the width of the Hall bar and l the distance between the contacts.

After [66] there is no distinction between R_{xy} and ρ_{xy} in a two dimensional system, because equation 19 is already independent of the sample geometry.

4 CdTe-Buffer on GaAs:Si

In March 2011 the Tōhoku earthquake and tsunami hit the Japanese eastern coastline and caused a flood which destroyed large parts of japan. Furthermore three reactors of nuclear power plant at Fukushima suffered meltdowns. All this accidents led to a temporal breakdown of the Japanese economy [73]. Because the only commercial producer for CdTe substrates has located its production center in Japan, through this natural disaster there were a delivery bottleneck and quality problems with the ordered substrates. In this period of time we decided to try growing CdTe buffer by MBE because CdTe crystal surfaces are essential for Hg - based MBE grown crystals. Furthermore, prior considerations contained already to grow CdTe buffer on a doped substrate which can be used in connection with this insulating CdTe as a back gate.

4.1 MBE Growth

The aim of this part of the thesis was to find growth parameter for CdTe (001) buffer on another substrate, so the HgTe quantum wells on these buffers reach the same carrier densities and mobilities as grown on commercial CdTe substrates. The biggest problem of growing CdTe (001) by MBE is to find a suitable substrate. Commercial substrates as silicon (Si) or gallium arsenide (GaAs) have a lattice constant which is rather far away from the lattice constant of CdTe. The mismatch to silicon is around 17 % and to GaAs nearly 15 %. This means that there is a lot of lattice stress in the first monolayers of CdTe, so a lot of lattice defects, dislocations and grain boundaries originate there [74, 75, 76, 77]. Due to the smaller lattice mismatch we started first tests on GaAs substrates. This substrates were n-doped by Si, so it is possible to analyze the grown structure via SEM, because the electrons does not generate charging effects in the sample. Moreover the n-doped GaAs substrates have a big advantage compared to the commercial CdTe substrates. There were anterior plans to manipulate the Fermi level of the HgTe structures by a back gate. This could now be realized by the n-doped GaAs substrate and the thick CdTe buffer which works as an insulator (band gap $\approx$ 1.56 eV). As another advantage of these self grown CdTe buffer on GaAs the size of the samples is a further benefit. While the commercial CdTe substrates only have dimensions of 10 x 10 mm, the GaAs substrates are standard 2 inch wafers which can be used. But in the progress of getting CdTe (001)-oriented buffer with good quality there were a lot of challenges to go through.

For the achievement two MBE chambers interconnected to the same UHV cluster were used. On the one hand a III-V chamber which is equipped amongst others with an arsenic cracker cell (As) and a gallium (Ga) effusion cell, on the other hand a II-VI chamber equipped amongst others with a cadmium (Cd), a tellurium (Te) and a zinc (Zn) cell was in usage. These

two chambers differ in detail to the CMT - chamber described in chapter 3.1.2. While the CMT - chamber is a horizontal system, the III-V and II-VI chambers have a vertical buildup. But the fundamental functional components are in all three chambers nearly comparable.
The growth of a II-VI semiconductor CdTe on a III-V surface of GaAs is connected to two essential problems. One is that CdTe and GaAs exhibit a very large difference in the lattice constant as mentioned before. This will be discussed later more in detail. The second problem is that such a transition causes a disturbance of the II-VI and the III-V band structure. So the polarity of the III-V surface and the binding behavior of the group II and VI elements affect which value and sign the carrier density attains accumulated at the interface. These charging effect manipulates the upper lying layers by its electrostatic field [78]. The existence of this effect can not be forgotten for the evaluation of the magneto transport measurements when a functional HgTe layer is on top of it. But due to the gating of all samples and to a very low impact, all HgTe samples are measured in a vertical electrostatic field, so the charging effect at the III-V II-VI interface can be neglected for standard characterization measurements.

Lattice Mismatch

As mentioned above, the lattice constant of CdTe and GaAs differ a lot. So is the lattice constant of CdTe 6.4825 Å[17] and of GaAs 5.65325 Å[79]. As a consequence of this, the lattice mismatch f between CdTe and GaAs is:

$$f = \frac{a_{CdTe} - a_{GaAs}}{a_{GaAs}} \approx 14.7\%. \qquad (1)$$

This large lattice mismatch leads to different growth directions of CdTe on (001) GaAs at diverse preparations of the substrate [80]. If the natural oxidation layer of GaAs is removed completely, CdTe grows in the (111) direction on (001) GaAs. After leaving parts of the oxide on the GaAs substrate CdTe grows in the (001) direction, but in very bad quality. So very many stacking faults and micro-twins exist at the interface and extend into the layer [75, 76, 81]. In our first experiments the (111) growth direction of CdTe was proved as shown in Fig.4.1. The peak with the high intensity is the Bragg reflex of the (004) plane of (001) GaAs at 33.0266°. The peak with the lower intensity originates from the (111) CdTe reflex.

The focus of this work is however located on the growth in (001) direction because of the further Hg-based heterostructures. By Feldman *et al.* [82] $Cd_{1-x}Zn_xTe$ is grown on (001) GaAs with a variation of x from 0 to 1. Here it is reported that ZnTe grows all the time in (001) direction and the surface morphology and crystal quality of (001) CdTe on top is immense improved by this progress. Through XRD measurements it is shown that the CdTe - FWHM of ω-scans for CdTe-ZnTe-GaAs structures is explicit smaller than the FWHM for CdTe-GaAs structures. With this previous knowledge a new growth process is designed for good quality samples of (001) CdTe.

As mentioned before, for high crystalline quality MBE samples it is necessary for the growth start to get ride of the oxide. This oxide on GaAs is not natural. After polishing the GaAs wafer is put into H_2O_2 which leads to an oxidation of the surface as protection. This is made on purpose. Therefore, it is common for GaAs to heat the wafer in the MBE chamber

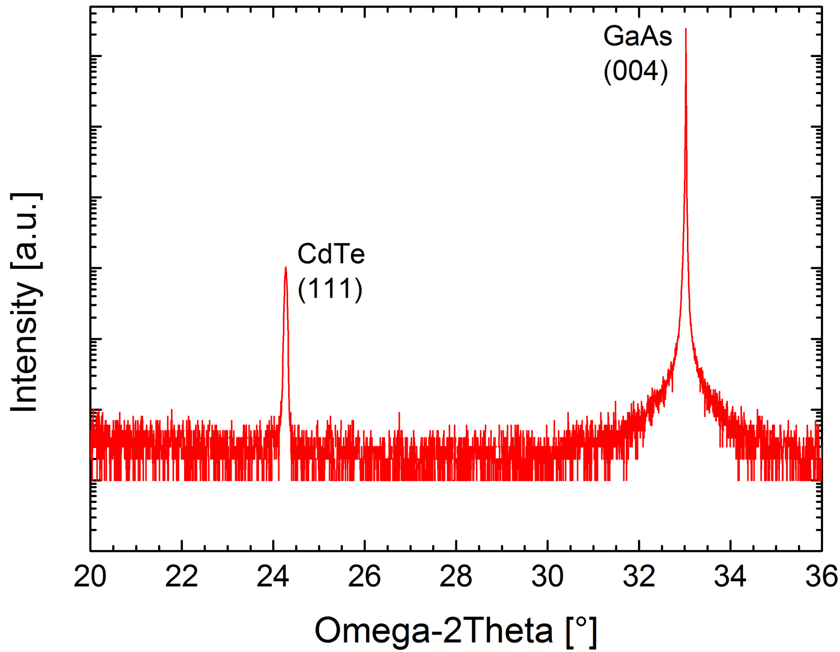


Figure 4.1: ω-2Θ-scan of the GaAs (004) and CdTe (111) reflection.

as high as the oxide desorbs. This can be done in arsenic atmosphere in the III-V chamber or rapidly in the II-VI chamber. Both techniques provide a minor arsenic desorption for temperatures over 550°C. In literature the desorption point of the oxide is at 582°C [83]. In our CdTe chamber there is no possibility of oxide desorption under arsenic flux. Therefore the wafer is heated up to 500°C. Afterward the heating power of the filament is maximized, so the GaAs substrate is only a short time in this arsenic out-gassing region. After recognizing a change in the RHEED pattern, a spotty (2x4) reconstruction is determined as shown in Fig.4.2 (a). To avoid a surface contamination with Te the Zn shutter is opened for the entire cooling down process. Tellurium reacts with the GaAs substrate to a monolayer (ML) of Ga_2Te_3 and this turns into a (111) orientated surface [84]. Zinc does not affect the surface in a verifiable way (Fig.4.2 (b)). The substrate temperature of GaAs is changed in this thesis between 320°C and 370°C for ZnTe growth. Rheed pattern looks always the same during the growth start. With only the Zn shutter open, a (2x4) reconstruction is visible, as mentioned above. After opening of the Te shutter, the reconstruction disappears after around 2 seconds and after approximately 10 seconds the typical three dimensional spotty RHEED pattern of the zinc blende structure appears (see Fig.4.3 (c)). The spots are broaden and not sharp as the streaks of the (2x4) reconstruction. However, it is observable that the distance of the reflexes decreases in the reciprocal space which means that the ZnTe starts already to relax within the first seconds after the growth start. Pseudomorphic fully strained layers were observed for deposits up to 4 ML,

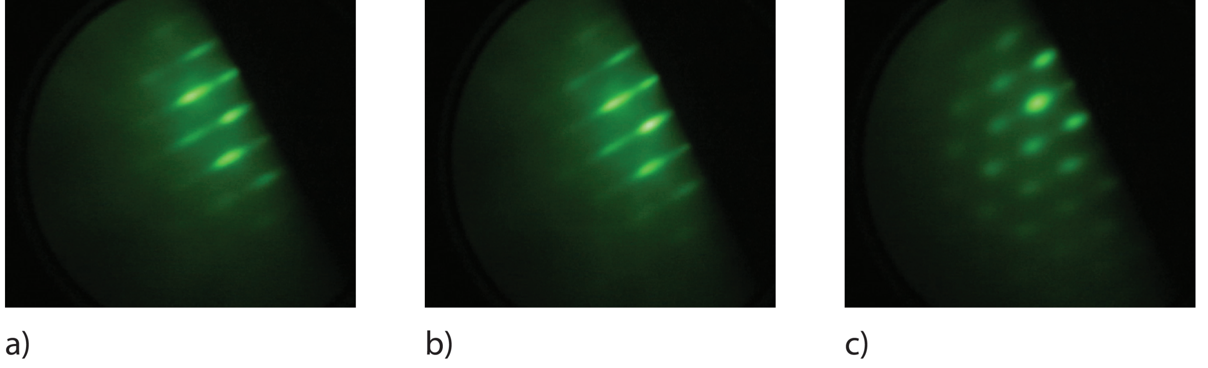


Figure 4.2: RHEED pattern of (a) GaAs substrate, (b) GaAs substrate and Zn sutter open, and (c) GaAs substrate with 20 seconds ZnTe growth.

whereas plastic relaxation sets in after a critical thickness of about 5 ML with the onset of a 3D island growth [85]. The growth times of ZnTe were varied between 15 seconds and 30 minutes. The best results for CdTe layers are achieved with a 30 second ZnTe growth so far as shown in chapter 4.2.2 by XRD and AFM measurements. In Fig.4.3 the temporal evolution of

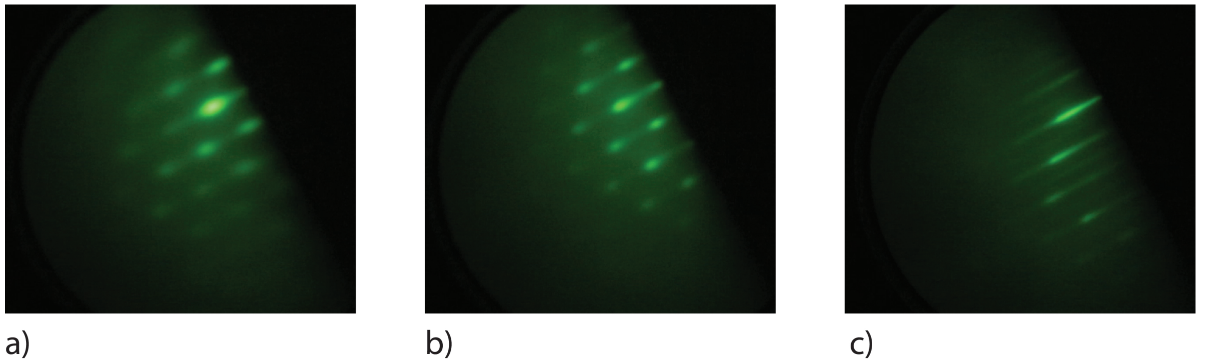


Figure 4.3: RHEED pattern of (a) GaAs/ZnTe and 30 seconds CdTe, (b) GaAs/ZnTe and 90 seconds CdTe, and (c) GaAs/ZnTe and 3 minutes CdTe.

the CdTe growth start is shown. So, with closing the Zn shutter, the Cd shutter is opened and three minutes long standard MBE growth of CdTe proceeds. It is clearly visible by RHEED that the (2x1) reconstruction becomes clearer and the lines become sharper. Furthermore the spots which appeared due to the ZnTe growth vanishes within 3 minutes nearly completely and a 2 dimensional RHEED pattern is exhibited at the fluorescent screen. The relaxation behavior of CdTe on ZnTe is comparable to ZnTe on GaAs. The lattice mismatches are nearly in the same range [79]:

$$f_1 = \frac{a_{ZnTe} - a_{GaAs}}{a_{GaAs}} \approx 8.0\% \tag{2}$$

and

$$f_2 = \frac{a_{CdTe} - a_{ZnTe}}{a_{ZnTe}} \approx 6.2\%. \qquad (3)$$

Therefore there is observable a decrease of distance of the RHEED reconstruction lines in the first seconds of CdTe growth which means CdTe starts to relax. Furthermore, one can see in Fig.4.3 that the reflections get much more sharper. This is a hint that homogeneous crystallographic planes of CdTe appear in the area of the sample where the electron beam of the RHEED system hits the sample when CdTe is grown on a very thin and rough ZnTe surface. Fig.4.4 shows the (2x1) reconstruction of the RHEED signal in (110) direction after a 60 minutes growth. CdTe buffer layers on GaAs:Si are grown to the thickness of about 4 μm, so the subsequent Hg-based heterostructures are not influenced by the III-V/II-VI interface, the gating properties of the insulating CdTe buffer is sufficient and the quality of CdTe is serviceable for HRXRD measurements. In the further CdTe growth process there is no relevant change in RHEED observable.

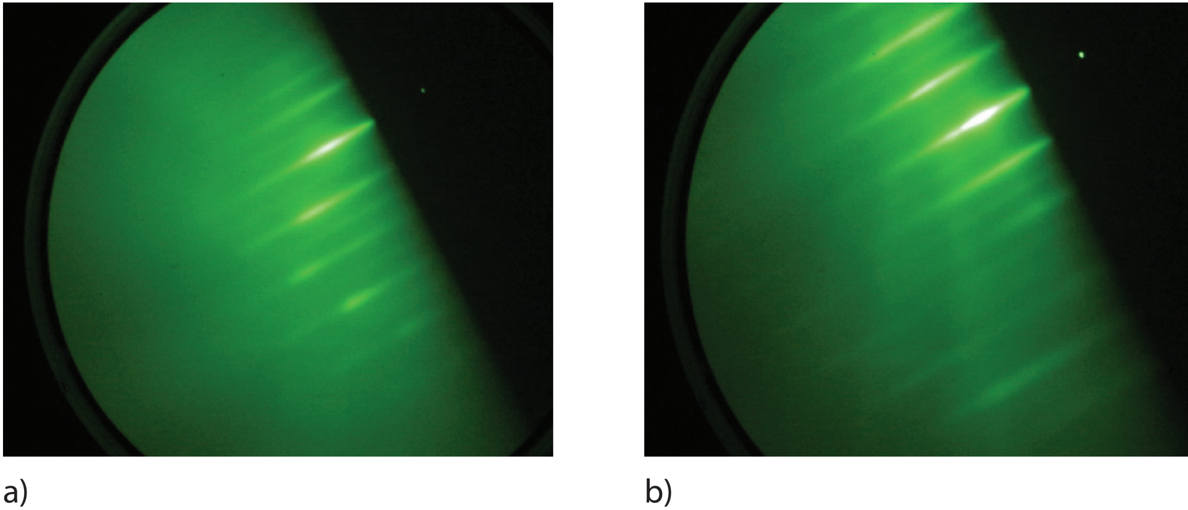


Figure 4.4: RHEED pattern of (a) 60 min and (b) 10 hr CdTe growth on a GaAs substrate.

Growth Parameters

For optimization of the crystalline quality of the CdTe buffer layers there are many parameters to work with. At first the preparation of the GaAs:Si surface is to analyze and to improve. Here we tried three different approaches where in all three the oxide removal plays a very important role. We started with a standard thermal desorption which is reached at temperatures around 630°C and cooled down in a zinc atmosphere. This could be done in the II-VI chamber. Furthermore we did the same in the III-V chamber, but opened the As cell at T=550° to avoid As desorption as well as during the cool down until the substrate reached T≈500°C. Based on this results a third attempt attached after the oxide desorption a 30 minutes GaAs

buffer growth at T=580° which generates a sharp (2x4) surface reconstruction in the RHEED pattern.

After the GaAs surface preparation the second big part to investigate was the growth start of the ZnTe layer. Here by changing the growth time and flux ratio of Zn and Te, we analyzed the start conditions. Time spreads of 15 seconds up to 30 minutes Zn/Te-ratios between 0.8 and 1.6 and substrate temperature were studied. Finally, the parameters of the CdTe growth itself were researched by optimizing the growth temperature and flux ratio of Cd and Te. Furthermore, the growth mechanism were reconsidered by integrating growth breaks or annealing times.

In the following the CdTe (001) growth design on Si-doped GaAs (001) substrates is presented with the optimized growth conditions and sequences. The RHEED pattern mentioned before are valid for all produced samples qualitatively and give feedback about the growth direction and mode in real-time. A quantitative analysis occurs in chapter 4.2.

Optimized Growth Design

All GaAs wafers were treated the same way until they reached the III-V or II-VI MBE chamber. A two inch epi-ready GaAs:Si wafer is quartered along the crystallographic directions (110) and $(1\bar{1}0)$ and one quarter is glued with molten indium on a molybdenum block. This block is then locked into the UHV system. Here, the wafer is baked out at a temperature of 300°C for 15 minutes. Afterward, the molybdenum block is transferred into the particular MBE chamber.
The optimized growth design of CdTe (001) on GaAs:Si (001) for further Hg-based layer growth is given below:

- The substrate is firstly heated up to 500°C. When temperature is stabilized, the power supply output power of the substrate heater is regulated to the tolerated maximum (current around 13 amps) to reach the oxide desorption point rapidly.

- When the oxide desorption point is achieved by change of the RHEED pattern, the output power of the power supply is switched off and the Zn cell is opened immediately. During the cool down process the substrate is exposed the Zn flux all the time.

- After stabilizing at T=315°C, the Zn and the Te cell are opened together for 30 seconds. The flux ratio Zn/Te $\approx$ 0.88 prefers good growth conditions. The RHEED pattern show the growth of ZnTe (cf. Fig.4.2).

- After 30 seconds ZnTe growth, the Zn cell is closed and the Cd cell is opened simultaneously. Cd and Te cells are open for 3 minutes. Here, the flux ratio for two dimensional growth is Cd/Te $\approx$ 1.9.

- Hereupon, the investigated migration-enhanced epitaxy (MEE) is applied for three cycles. While the Cd cell is always open, the Te is programed to open for 30 seconds and close for 10 seconds for 300 times at each temperatures of 315°C, 300°C and 290°C.

- During the five minute cooling-downs, the sample is annealed in Cd flux.

- After these three MEE cycles, the sample is annealed for 30 minutes in Cd, so the closed Te cell can cool down.

- As last step, the CdTe sample is steadily cooled down in Cd flux until substrate temperature T=100°.

A schematic sketch of the substrate temperature distribution is shown in Fig.4.5. Indium is chosen as adhesion promoter. This is unusual in the mercury business because gallium, which is the common adhesion promoter for Hg-based growth, does not keep its adhesive properties at higher temperatures. Due to the high temperatures for GaAs oxide desorption, the gallium starts to diffuse into the molybdenum block and into the GaAs wafer. Several experiments confirm this fact [88, 89]. A mixture of indium and gallium does not work as well. The use of indium may cause a degeneration of the carrier mobility of the HgTe layers after in-situ growth because the separating of the ready grown sample from the molybdenum block takes place at around 200°C. This is a higher temperature as the ordinary growth temperature for HgTe. Nevertheless, two and three dimensional HgTe layers grown on CdTe/GaAs:Si show very promising results which will be discussed later in chapter 5 and 6.
The characterization and analysis of the CdTe samples are shown in the following chapter.

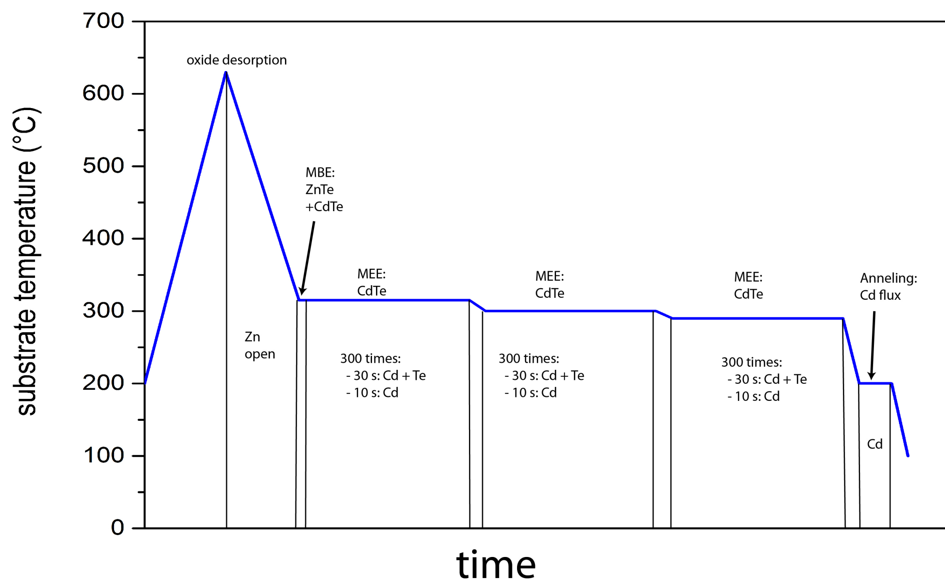


Figure 4.5: Schematic sketch of the growth design of the optimized 4 μm thick CdTe buffer layer.

4.2 Characterization

The CdTe samples were analyzed by RHEED, differential interference contrast microscopy, high resolution X-ray diffraction and atomic force microscopy. Furthermore, chemical etching experiments were performed to determine the etch pit density of the CdTe layers. The layer quality is ranked by RHEED pattern, surface roughness and the crystalline purity grade which is important for subsequent HgTe growth. However, the CdTe growth had to be optimized before in-situ HgTe growth, so all analyzed CdTe samples has seen atmospheric air during characterization and therefore have an oxidized surface.

4.2.1 GaAs:Si - Preparation

The overall start condition plays a very important role for MBE layer growth. So the GaAs:Si surface preparation matters a lot, as mentioned above. The GaAs wafers receive a special surface oxidization by the producer company to obtain the same surface conditions for all wafers. To avoid chemical contamination, a common procedure for GaAs is thermal desorption in the MBE chamber to get rid of the surface oxide. In this thesis it is investigated three surface preparation techniques for the ZnTe start on GaAs. Firstly, the GaAs substrate is heated up to a temperature around T = 550°C. Then the arsenic cell is opened and under As flux the thermal desorption of the oxide happens at around 620°C in the III-V chamber. The desorption point is determined by RHEED. The whole heating process can be done in an accurate time scale because, due to the As flux, the crystalline quality of the wafer does not degenerate veritably. The cool down is equal in As flux down to temperature T = 550°C. At 200°C the substrate can be transferred out of the III-V chamber and can be treated to further experiments.

A second approach can be done in the III-V chamber. Here, the same thermal oxide desorption happens as above but a big difference occurs right after the desorption point. When the oxide is removed, the substrate temperature is stabilized at T=580°C and the gallium cell is opened for 30 minutes. With a flux ratio of Ga/As $\approx$ 0.4/6.0 provided a two dimensional GaAs surface is generated and can be confirmed by a sharp 2x4 RHEED surface reconstruction pattern. During the cool down process the As cell is closed at T=550°C again.
As third preparation technique a simple rapid heating process is used without any cell shutter open. Here, only after the oxide desorption the Zn cell will be opened during the cool down to prevent atomic evaporation of the substrate. Zn does not affect the GaAs surface as much as Te and is required for the subsequent ZnTe layer as well. As big advantage of this method there is no III-V chamber necessary and as extensive prospect the whole growth process can be done in the CMT - chamber because Hg, Te, Cd and Zn are available in both CMT - chambers, so no transfer is required.

Fig.4.6 shows SEM pictures of the first and third preparation technique. In Fig.4.6 (a) it is clearly visible that no flat surface is preserved anymore and a lot of holes with different diameters and depth arise due to the thermal oxide desorption. On the other hand, the GaAs surface in As atmosphere during oxide desorption does not feature these holes and seems almost flat (cf. Fig.4.6 (b)). After growing the GaAs buffer after oxide desorption the surface has the best prepared and most comparable condition.
However interestingly, the rapid thermal oxide desorption with Zn cool down generates the

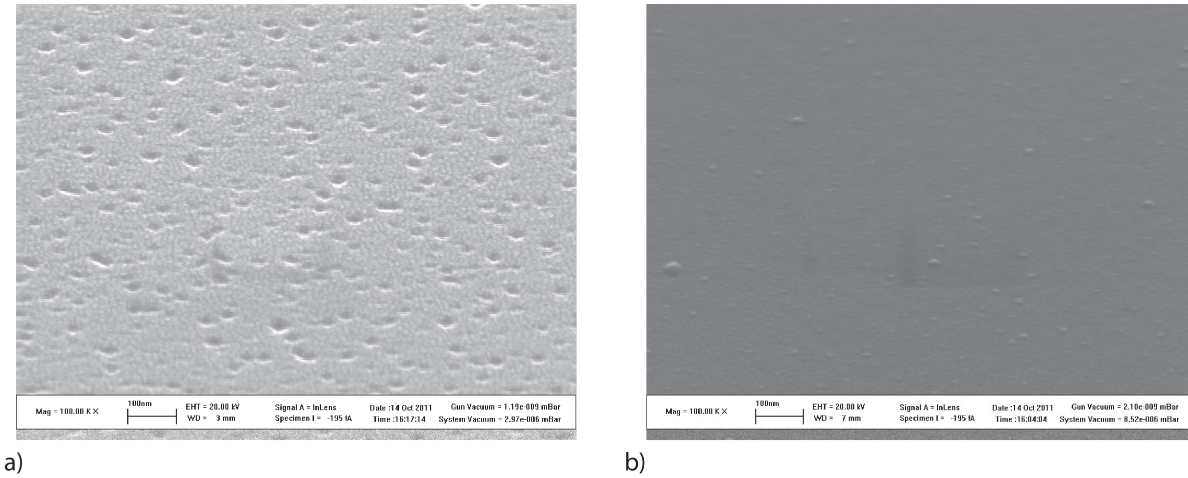


Figure 4.6: SEM pictures of GaAs:Si surface after oxide desorption without (a) and with (b) arsenic flux. Samples were afterward metalized in-situ with 1 nm Au for surface preservation.

CdTe (001) layer with the lowest FWHM value of the (004) reflex in the HRXRD-ω-scan as well the minimal AFM-RMS value of the surface. So as long as the CdTe layer is not thick enough, one can still detect by AFM the holes of the oxide desorption. This is shown in Fig.4.7. The holes are at least 15 nm deep and therefore it takes a certain time to overgrow of these holes. This is in agreement with the literature ($\approx$ 11 nm) [90] if there is the assumption that the CdTe growth does not change the surface considerably. On the surface of a 4 μm thick CdTe layer there is no evidence of these holes anymore (Fig.4.11 d)). Furthermore the oxide desorption serves as a substrate temperature calibration due to the fact of the well known thermal desorption temperature and the hole appearance is investigated as well [91]. In HRXRD measurements the FWHM of an ω-scan of the CdTe (004) reflection shows that the CdTe layers with a thickness of around 4 μm cooled down in Zn atmosphere show the lowest value so far. The following table shows the FWHM of the omega-scans of the CdTe layers which suffered three different GaAs:Si (001) substrate preparation techniques:

Sample	GaAs-Puffer	As-atmosphere	Zn-atmosphere	ω-FWHM$_{CdTe}$
CE22	no	yes	no	1063 arc sec
CE23	no	no	yes	806 arc sec
CE161	$\approx$ 250 nm	yes	no	178 arc sec
CE175	no	no	yes	150 arc sec

Table 4.1: Table for comparison of the GaAs surface preparation

The ω-FWHM values are the lowest respectively. Furthermore, it has to be mentioned that

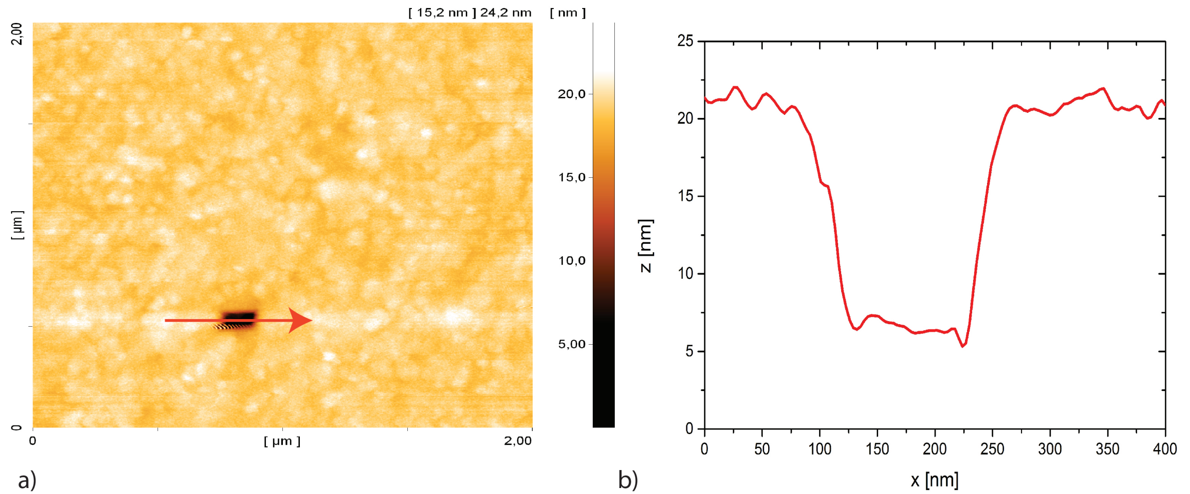


Figure 4.7: (a) AFM picture of a 100 nm thick CdTe buffer. (b) Elevation profile of hole shown on the left side.

after the first test runs (CE22 and CE23) the cool down in As-flux of the GaAs:Si substrate is given up because of the very high FWHM value. The research is then focused on the CdTe growth development and just after optimizing of that some cross-checks are executed (CE161). Summarizing the results, a cool down in As-flux increases the FWHM-value of the CdTe layer compared to a similar CdTe layer which received a cool down in Zn-atmosphere before starting the ZnTe layer growth ($FWHM_{As}$ = 1063 arc sec > $FWHM_{Zn}$ = 806 arc sec). The main difference between the samples CE22, CE23 and CE161,CE175 is the thickness of the CdTe layer. While CE161 and CE175 exhibits a CdTe layer thickness of around 4 μm, the samples CE22 and CE23 possess only a thickness of around 0.5 μm. This larger thickness decreases the FWHM-value drastically. However, for the thick CdTe layers a GaAs buffer is grown before the ZnTe start to smooth the initial, deoxidized GaAs:Si surface. Here, the difference of the FWHM-value is just around 30 arc sec but the result is still a little bit surprising because usually MBE layers grow layer by layer at its best when the lower layer is already two dimensional. So we assume that due to the presence of the holes the ZnTe layer which will instantaneously start to relax due to the large lattice mismatch grows three dimensional (spotty RHEED pattern) and therefore the holes even out these three dimensional growth at least a little bit. The two dimensional GaAs surface conditions generate through the ZnTe layer a rough three dimensional surface due to relaxation effects by reason of the large lattice mismatch. However, in the RHEED pattern one can not distinguish these low roughness differences. AFM measurements show an adulterated picture because the AFM is not in-situ and therefore the oxidization falsifies the surface roughness. Summing up all CdTe layers, grown with the rapid thermal oxide desorption start, show the lowest FWHM-values in ω-scans by HRXRD and lowest RMS-roughness by AFM so far. However, there is still plenty of room for improvement for the GaAs:Si substrate preparation and the following cool down in different particle fluxes.

4.2.2 ZnTe - Growth

Another important point for CdTe (001) growth on GaAs:Si (001) is the attendance of a ZnTe layer. As mentioned before, CdTe will grow on a GaAs (001) surface after complete oxide desorption in (111) direction [80]. Due to the growth temperature of around 300°C, the sticking coefficient of Cd is almost zero and no chemical reaction is on. Therefore Cd is not suitable for starting on such a interface condition, especially if there a transition from a III-V to a II-VI semiconductor. If Te now is hitting the GaAs surface first of all for our growth conditions, the sticking coefficient is not much higher than for Cd, but there occurs a chemical reaction between Te and the GaAs surface during the cool down process. Houston *et al.* [84] described in 2013 that they observed via a combination of high-angle annular dark field (HAADF) and energy-dispersive X-ray spectroscopy (EDS) the distance between the Ga and the Te atoms at the interface. This distance fits very well to the projected Ga and Te distance which exists in Ga_2Te_3. This leads to a hexagonal surface reconstruction which typically gives rise to further growth in the (111) direction. This is not desired because CdTe (001) is required for later Hg-based MBE grown heterostructures. So, ZnTe is commonly used as an inter layer which grows on GaAs (001) in (001) direction [82] and therefore forces the upper layer to grow in the same (001) direction. Only the ZnTe layer provides a complete and consistent growth of the CdTe layer in the (001) direction. All other methods can not supply comparable good and compelling results.

There are several CdTe samples with different ZnTe layer thicknesses, starting with a growth time of 15 seconds up to a growth time of 30 minutes. This is comparable with approximately 2 nm for 15 seconds and about 300 nm for 30 minutes. The thickness varies of course with the substrate temperature during growth. While the 15 second growth shows a spotty, three dimensional RHEED pattern, the ZnTe layer starts to overgrow the three dimensional surface structure and after around 5 minutes the RHEED pattern show a clear (2x1) reconstruction and the lines become longer and sharper in time. In table 4.2 characteristic data of certain CE-samples are listed:

Sample	t [s]	T[°C]	d_{CdTe} [nm]	ω-$FWHM_{CdTe}$	RMS_{AFM}
CE05	30	340	$\approx$ 1600	340 arc sec	5.19 nm
CE12	60	310	$\approx$ 1000	1332 arc sec	4.95 nm
CE18	1800	350	$\approx$ 1600	624 arc sec	4.92 nm
CE24	30	350	$\approx$ 1700	295 arc sec	5.54 nm
CE38	15	350	—	— arc sec	—
CE168	1200	315	$\approx$ 4000	209 arc sec	2.35 nm (Hg-growth)
CE170	2400	315	$\approx$ 4000	258 arc sec	2.53 nm (Hg-growth)
CE175	30	315	$\approx$ 4000	150 arc sec	3.85 nm

Table 4.2: Table for comparison of the ZnTe growth results. For CE168 and CE170 the RMS roughness is not measured of the CdTe layer because a HgTe-HgCdTe heterostructure was grown in-situ on top of it.

Here, the growth time is directly related to the ZnTe layer thickness because the ZnTe growth rate is approximately all the time the same. For this table the Zn/Te ratio averages around 0.88. The thickness of the CdTe layers is here estimated by the growth time and the growth rate. Due to the large CdTe FWHM values of the HRXRD-ω-scans and rough interface conditions, no thickness fringes are observable. As one can see the layer with the above described optimized growth design shows very suitable FWHM-ω-scan and AFM-RMS results. So a FWHM of around 150 arc sec is until now the lowest value which was able to grow in the (001) direction. For short growth times of ZnTe ($t < 20$ seconds), the RHEED pattern of the followed CdTe is not showing two dimensional indications as streaks. After 50 minutes of CdTe growth, a spotty RHEED pattern is still visible which is a evidence for three dimensional growth including a rough surface. Compared to all other CE-samples, which started with ZnTe growth longer than 20 seconds, the RHEED 2x1 reconstruction appears at least after four minutes including nice, long lines. So it is necessary that a certain ZnTe layer thickness is provided for CdTe growth in the (001) direction. Otherwise it is not beneficial growing ZnTe very thick. So different samples (CE18, CE168, CE170) feature thicker ZnTe buffer layer between GaAs substrate and CdTe layer. For this growth times, the ZnTe RHEED pattern show a nice, clear 2x1 reconstruction. But after CdTe growth, the FWHM of the CdTe layer has much larger values than the optimized CdTe structure. However, the CdTe thickness is smaller for the CE18 and with larger CdTe thickness the FWHM becomes smaller if the quality stays the same. But the measured RMS roughness (4.92 nm) via AFM shows that for CE18 the growth parameters provide space for improvements compared to CE175. Furthermore the FWHM of CE05 is halved due to the 30 second ZnTe growth compared to CE18 while the RMS roughness is in the same range of about 5 nm. In addition, the samples CE168 and CE170 show the smallest surface roughness with $\approx$ 2.5 nm. However, this is caused of the on top in-situ grown HgTe-HgCdTe heterostructure. The surface diffusion of the Hg atoms is very high at growth temperature due to the Hg vapor pressure and therefore

surface roughness can be flattened during this Hg growth. But the FWHM of this two samples show clearly that the crystalline quality decreases with increasing ZnTe thickness. So CE168 has a measured CdTe FWHM of 209 arc sec whereat the FWHM of CE170 is determined to 259 arc sec. This is a clear indication that a thicker ZnTe layer does not only trigger a higher quality CdTe layer but also downgrade the crystalline quality.

In Fig.4.8 HRXRD-ω-scans of the (004) reflection are shown for samples with different ZnTe thicknesses. Here, it is clearly visible that sample CE175 owns the lowest value of FWHM of around 150 arc sec. Furthermore, the quality of the sample is represented by the intensity of the HRXRD-scan. If the samples have the same thickness and the measurement is done with the same adjustments, a higher intensity is equal to a higher crystal quality. This occurs because more X-rays are diffracted at the crystal planes due to higher crystalline quality due to lesser scatter centers in the layer which attenuate the diffracted X-ray beam.

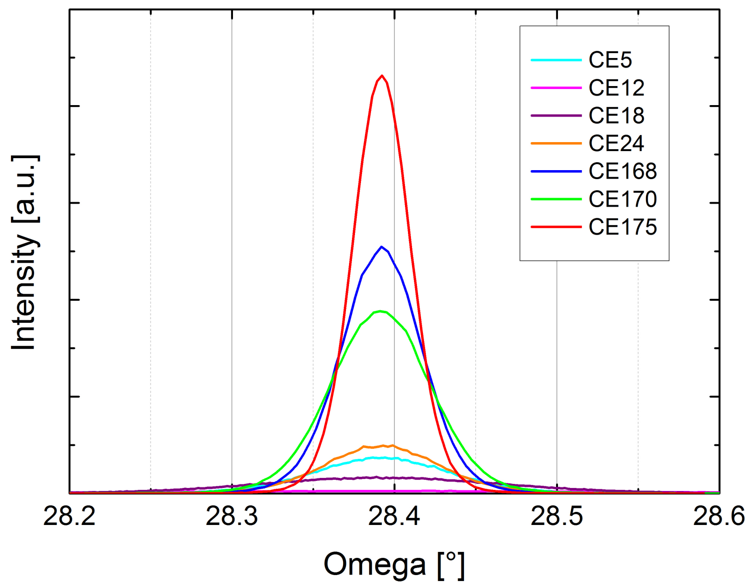


Figure 4.8: HRXRD-ω-scans of the (004) reflection of CdTe with different ZnTe growth conditions. The particular parameter are shown in table 4.2.

Furthermore, an ω-2Θ-scan of the sample CE170 is shown in Fig. 4.9. The (004) reflection of GaAs serves as a reference. GaAs is the used substrate with a wafer thickness of around 350 μm and cut off a large GaAs ingot. This provides that GaAs exhibits its natural lattice constant. The lattice constants of ZnTe and CdTe, which could be calculated from Bragg´s law, shows clearly that ZnTe and CdTe are fully relaxed as assumed by RHEED observations. Because of the Hg-based heterostructure, which were grown in-situ on the CdTe layer, there were still determined reflections of the HgTe quantum well and HgCdTe barriers as indicated. This scan serves however as evidence that the ZnTe layer is fully relaxed which was already

monitored by the change of the distance of the ZnTe RHEED streaks.

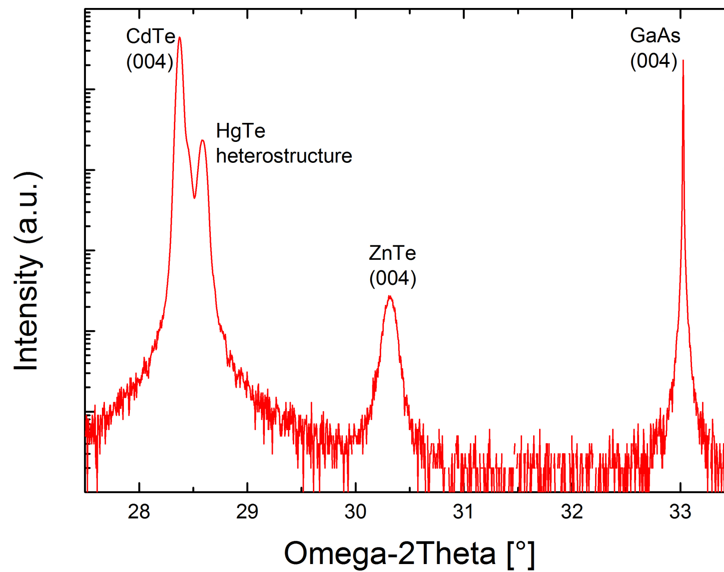


Figure 4.9: HRXRD-ω-2Θ-scan of CE170 (Q2808): the (004) reflection peaks of CdTe, ZnTe and GaAs are an indication for their lattice constants due to Bragg´s law. The GaAs peak serves here as the center of reference because GaAs as substrate has its natural lattice constant. The reflection angles of ZnTe and CdTe mark their lattice constants. This measurement shows that ZnTe as well as CdTe is fully relaxed.

So summing up, different ZnTe layer thicknesses do not particularly affect the surface roughness of the CdTe layer but importantly otherwise the FWHM becomes larger with thicker ZnTe layer and therefore the crystalline properties of CdTe fall off in quality.

4.2.3 CdTe - Growth

After investigating the underlying structures, the optimization of the CdTe growth on n-doped GaAs:Si in (001) direction required some different experiments. The optimized growth design of CdTe is listed in chapter 4.1 already. The main goal of this optimization is to minimize the surface roughness and the ω-full width at half maximum in XRD measurements. Based on the awareness of the GaAs surface preparation and the ZnTe buffer layer, the CdTe growth on top of this heterostructure is developed at first by finding the optimized substrate temperature, the Cd/Te- flux ratio and growth time.

First CdTe growth tests were performed through prior conversations with Prof. Dr. Grzegorz Karczewski from the Institute of Physics of the Polish Academy of Sciences. The growth temperature was recommended to T $\approx$ 350°C for 2D growth. In this thesis there will be only

focused on selected growth series for a clear arrangement. To increase the growth rate, the temperature has just to be decreased. So, first efforts show that for T $\geq$ 320°C the crystalline quality measured by HRXRD is insufficient. Simultaneously the migration-enhanced epitaxy (MEE) was introduced to optimize the crystalline quality. This technique supply originally the constituent atoms alternately and does not require saturation adsorption from both constituent species. So the saturation adsorption of one of the species is enough for MEE. This technology is based on the ALE process. Here the difference to MEE is that ALE requires self-limited adsorption for both constituent atom species which guarantees one complete monolayer coverage of the surface [93, 94, 95]. Here, the process is changed a little bit, so there is a simultaneous Cd and Te growth for 30 seconds and an annealing Cd process of 10 seconds. In these 10 seconds Cd is just deposited for one monolayer because Cd has a very high vapor pressure and therefore the sticking coefficient is almost zero at these growth temperatures. This can be observed via RHEED. During CdTe growth there is all the time a (2x1) reconstruction which is an indicator for a group VI rich surface (here Te). During the annealing phase the reconstruction changes immediately into a (2x2) reconstruction which represents a group II rich surface (here Cd) [96, 97, 98, 99]. This growth technique leads to a large drop of the value of the ω-FWHM in HRXRD measurement. In table 4.3 is shown a CdTe growth series in which the growth temperature was changed by 10°C respectively and the growth took place by an ALE 606 times cycle with 4 seconds of each Cd and Te sublimation and between these two a 0.5 second dead time. Due to the low thickness of the CdTe layers of this series, the ω-FWHM values are extremely high (> 1000 arc sec) and for this experiment not relevant. The focus on this temperature series is located on the surface roughness. This was measured

Sample	t [s] (Cd+Te)	T[$^\circ C$]	d_{CdTe} [nm]	Cd/Te	RMS_{AFM}
CE50	4+4	300	$\approx$ 100	1.5	2.86 nm
CE51	4+4	290	$\approx$ 100	1.5	3.24 nm
CE52	4+4	280	$\approx$ 100	1.5	1.66 nm
CE53	4+4	270	$\approx$ 100	1.5	1.74 nm
CE55	4+4	260	$\approx$ 100	1.5	0.82 nm

Table 4.3: Table for comparison of the substrate temperature for a CdTe growth series.

by AFM microscopy and visual observation by Nomarski microscopy. The RMS roughness as listed in table 4.3 point clearly that for lower temperatures the surface roughness decreases and reaches a minimum value of 0.82 nm at T = 260 °. Therefore it comes to the conclusion that lower growth temperatures decrease the surface roughness for CdTe. This occurs because at higher growth temperatures the Cd atoms does not stick very well to the surface. So there will be no monolayer which covers fully the surface. Otherwise, the sticking coefficient of Te is in this temperature range equal 1 during the first monolayer. Due to this self-regulating ALE process, there is at higher temperatures a slightly excess of Te which causes a higher surface roughness. At lower temperatures the sticking coefficient of Cd approaches 1 for the first monolayer which smooths the surface [100]. But due to this ALE growth process, the growth

rate of the CdTe is very small (≈ 0.2 Å/s). Furthermore, the ω-FWHM values are very large (> 1000 arc sec). Therefore, the growth process is changed from ALE to MEE where CdTe is grown by a 30 second simultaneously opening of the Cd and Te shutter and a 10 second Cd atmosphere annealing. This annealing in Cd vapor pressure is to fill up the empty Cd spots in the CdTe lattice [101]. The growth rate is increased due to this adjustment to ≥ 0.9 Å/s. A growth rate value of around 1 Å/s is common for MBE.

In a further growth series experiment, the flux ratio of Cd and Te was changed by starting at a ratio of 1. This led to poor growth quality indicated by spots in the RHEED pattern. Furthermore the ration Cd/Te was increased to 3. During RHEED observation there does not occur a noticeable change, so investigations could only be done by Nomarski microscopy, AFM and HRXRD measurements ex-situ. However, the closing examination took place by standard magneto transport measurements of the HgTe quantum well which were grown in-situ on the CdTe buffer. Not before the carrier mobility and density are in the required range, the quality of the CdTe layers on GaAs:Si is not sufficient.

The flux ratio of Cd to Te is selected that in the vapor phase there is measured a Cd excess. However, a Te-rich (2x1) RHEED reconstruction is observed on the layer surface. In table 4.4 a CE-samples growth series for different flux ratios is listed. All these samples were grown with the same recipe. Furthermore this was one of the first MEE tests. The growth recipe was structured like 30 seconds Cd and Te growth followed by 10 seconds of annealing in Cd atmosphere. For this Cd/Te ratio test, his cycle runs 200 times at the same temperature T = 280°C except CE82.

Sample	t [s]	T[$^\circ C$]	d_{CdTe} [nm]	Cd/Te	ω-$FWHM_{CdTe}$	RMS_{AFM}
CE76	6000	280	≈ 850	2.0	919 arc sec	0.982 nm
CE78	6000	280	≈ 850	2.5	824 arc sec	0.889 nm
CE79	6000	280	≈ 850	1.9	749 arc sec	0.985 nm
CE82	6000	320	≈ 850	2.0	630 arc sec	1.89 nm
CE85	6000	280	≈ 850	3.0	1338 arc sec	1.32 nm
CE86	6000	280	≈ 900	2.1	1115 arc sec	0.793 nm
CE88	6000	280	≈ 850	2.9	907 arc sec	1.27 nm

Table 4.4: Table for comparison of the flux ratio between Cd and Te.

By analyzing the data of table 4.4, on the one hand the RMS-roughness shows a slight minimum at a Cd/Te flux ratio of around 2.1. On the other hand, the ω-FWHM values present a insignificant different behavior. For high Cd/Te flux ratios (around 3) the FWHM is in the range of around 1000 arc sec. The ω-FWHM values decrease roughly with the flux ratio. Sample CE86 is a special case because the flux ratio indeed is 2.1 but the Te flux is raised. Indeed this causes a smaller RMS value but the ω-FWHM is increased clearly. Also the sample CE82 is to observe in a different way. The growth temperature is here not 280°C but 320°C. This effects the lowest ω-FWHM value but also the highest RMS surface roughness.

Therefore it is very obvious that there is not available an ordinary standard recipe for the CdTe MBE growth. All parameters like substrate temperature, flux ratio and growth time (correlated to the layer thickness) has to be in perfect combination to grow highest quality crystals.

After analysis of all these data sets, the optimized CdTe growth process is developed as described above (4.1). But all these CdTe growth optimizations are not useful if the $Hg_{1-x}Cd_xTe$ MBE heterostructures do not provide good results in magneto-transport measurements on these CdTe buffer. Magneto-transport results are presented in chapter 5 and 6 and show very nice outcomes relating to carrier densities n and mobilities μ. Furthermore, these results demonstrate that the carrier mobility μ and density n change just very slightly over a 1/4 wafer. Similar space dependent experiments were not performed on whole two inch wafers so far. This means that the production of comparable samples is now guaranteed much better than growing on commercial CdTe substrates. At the moment, just 9 magneto transport samples can be fabricated out of one 10x10 mm^2 wafer. Growing on 1/4 of an 2" GaAs wafer, more than 40 magneto transport samples with the same properties can be fabricated up to now. This leads to a big advantage if different groups want to do different measurements on the same sample material for a better comparison of the results.

Otherwise it has to be mentioned that the surface roughness of these CE-samples is larger than the surface roughness of commercial CdTe substrates. The optimized CE samples have an average RMS surface roughness of about 2.5 nm, while the commercial CdTe substrates exhibit a RMS surface roughness of around 0.35 nm. Fig. 4.10 shows two AFM picture of a commercial CdTe substrate and a CE-sample. This RMS surface roughness of the CE-sample

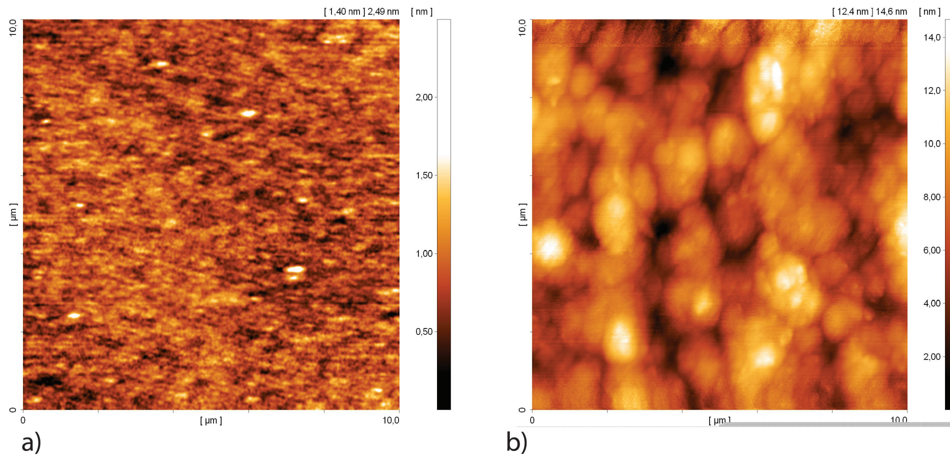


Figure 4.10: AFM picture of a) a commercial CdTe wafer surface and b) a CE sample surface grown with the optimized growth process.

seems to be very large on the first view. So, hills with elevations of around 15 nm characterize the surface roughness of these layers. This is huge difference compared to the atomically flat commercial CdTe substrate. However, these AFM pictures distort the point of view heavily. As those hills have elongations of over one micrometer, the elevation to elongation ratio is very small. Therefore, hill is maybe the wrong expression and it is more like a tiny uprising.

Nevertheless, HgTe quantum wells with a thickness of around 7 nm grown on top of these CdTe buffers can be affected by these tiny uprisings due to charge and defect accumulations. Furthermore, a top or back gate can not operate accurately because the HgTe quantum well is affected unequally due to the elevation differences.

Last but not least, there is to mention that the surface cleanliness is very high of these CE-samples because no chemical etching is used for removing native oxide. So, it is standard that there is no residual dirt on the whole wafer. Otherwise, the commercial CdTe substrates, which were etched by HCl for removing the oxide, show often a lot of residual etch chemicals and after growth large areas of flow marks which covers sometimes the whole 10x10 cm^2 wafer. This difference is shown in the Nomarski pictures in Fig. 4.11. So on the one hand, in a) and b) large areas are covered by flow marks and residual dirt which is indicated by the black points in the picture. Nothing similar is observable on the self grown CdTe buffer in picture c) and d). On the other hand, the flow marks occur due to the polishing by the selling factory and these roughness are not observable until the oxide is removed and another layer is grown on top of it. But in general, no large defect areas are identifiable on the CE samples. Furthermore, there is still visible that the roughness of the self developed CdTe buffer layers is higher than the roughness of the surface of the commercial CdTe substrates [Fig. 4.11 (d)].

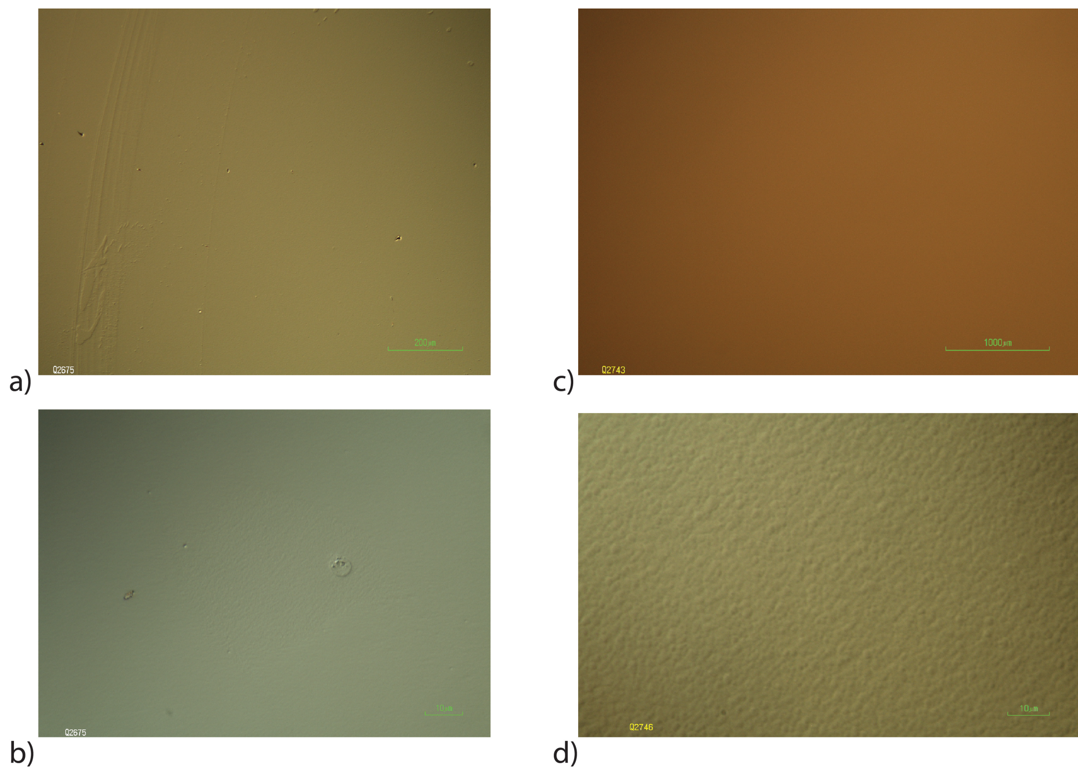


Figure 4.11: Nomarski pictures with different magnifications. a), b) Surface of a HgTe quantum well structure grown on a), b) a commercial CdTe wafer after HCL etching (Q2675) and c), d) after in-situ growth on a self grown CdTe buffer layer (Q2743).

4.2.4 Etch Pit Density

Furthermore, etch pit density (EPD) measurements were performed to compare the dislocation density of the self grown CdTe buffer on GaAs with commercial CdTe substrates. Etch pit density is a measure for the crystalline quality of semiconductors. An etch solution is disposed on the surface of the substrate where the etch illustrates dislocations of the crystal because the etch rate is increased at dislocations or defects of the crystal resulting in pits. The density of the etch pits is determined by differential interference contrast microscopy. Common semiconductor densities are i.e. for silicon wafers lower 100 cm^{-2} and for GaAs ≤ 500 cm^{-2} [102]. The used commercial CdTe wafer are listed by the manufacturer in the order of $\leq 1\times10^5$ cm^{-2} [103]. This is another indication that the CdTe crystalline quality is inferior to the quality of Si and GaAs, still for industry standards.

So after the first magneto transport measurements of a functional back gate, the breakdown voltage of these CdTe buffer as insulators are determined to a maximum of +20 V and -20 V. This will be described in detail later in chapter 5 and 6. However, on some samples the breakdown voltage is lower. Therefore it is not possible to do the desired transport experiments because the Fermi level is located in the band gap. Due to this breakdown voltage variations, there has to be done some research on this cause. To exclude the crystalline quality of the CdTe buffer as an insulator, there has to be done etch pit density measurements to determine dislocations which may cause leakage currents through the CdTe buffer. This leakage currents decrease the value of the breakdown voltage.

First etch pit density measurements were done by Inoue *et. al.* in 1961 [104]. His etch is still the only one which provides dislocations of CdTe (001). There are several other etching solutions but all these supply dislocations for other orientated CdTe substrates. The used etching solution of Inuoe [104] is showed in the following table:

Symbol	Composition	Amount	Etching action
E	Concentraded HNO_3	10 ml	Chemical polishing
	H_2O	20 ml	
	$K_2Cr_2O_7$	4 g	
EAg-1	E solution	10 ml	Etch pit formation
	$AgNO_2$	0.5 mg	
EAg-2	E solution	10 ml	Etch pit formation
	$AgNO_2$	10 mg	

Table 4.5: Etching reagents for CdTe (001).

This etching solution implies a chemical polishing part and an etch pit formatting part. So, the substrates are chemically polished before etching to remove damage or roughness of the surface. Therefore the used etching solution is E (c.f. Tabl. 4.5). Inoue described that these solutions are excellent for polishing the surface and obtaining microscopically mirror-like surfaces. For his etching experiments he used crystals which where cut from a CdTe single

crystal made by the Bridgman method. The self developed CdTe (001) layers provide still mirror-like surfaces after growth but due to comparability this chemical polishing solution is used. Therefore, together with silver nitrite ($AgNO_2$) etching solution E produces etch pits for CdTe(001). Inoue developed two etching solutions EAg-1 and EAg-2. In this thesis, only etching solution EAg-1 is used because the results are very sufficiently. First etching tests show already that the above in Tabl. 4.5 listed composition is very effective. So, these solution is useful for thick single crystals which were fabricated by Bridgman method. Therefore the etching solution has to be diluted for thin MBE grown CdTe layers by a factor of 10 with water. All samples were put for 2-5 seconds in this diluted etching solution which is heated to 80°C. After rinsing with ultra-pure water, the sample is analyzed by an optical microscope (see Fig. 4.12) and the defect density is determined by counting. In the following table, all analyzed samples are listed including their averaged etch pit density:

Sample	Thickness	T_{etch} [°C]	EPD
CE131	4.50 μm	80	8.5×10^3 cm^{-2}
CE142	4.50 μm	80	2.4×10^4 cm^{-2}
CE148	4.50 μm	80	9.5×10^3 cm^{-2}
AU 09112 (ID20.3)	800 μm	80	3.0×10^4 cm^{-2}

Table 4.6: Averaged etch pit density for several CdTe substrates.

At first, the most surprising result is that the commercial substrate AU 09112 ID20.3 offers the highest EPD of all measurements.However, this value is still under the specifications which is provided by the manufacturer JX Nippon ($\leq 1\times10^5$ cm^{-2} [Nakagawa etch]). However, the Nakagawa etch used by JX Nippon is only useable for the (111)A direction [15, 105]. All analyzed CdTe buffer layers grown on GaAs:Si show a lower EPD. For all samples several etching experiments were done with the same parameters and then the averaged value was estimated. While the samples CE131 and CE148 are grown exact identically, CE142 has a slightly different growth recipe. So CE131 and CE148 have these optimized growth design but with 400 times cycle instead of 300 times, CE 142 has these 300 times growth cycle with 60 seconds Cd + Te and 10 seconds Cd opened. Furthermore CE142 is grown at three growth temperature steps 315°C/310°C/300°C instead of 315°C/300°C/290°C. The layer thickness should therefore be in the same range and therefore comparably. While the two samples with the optimized growth design (CE131, CE148) show the two lowest EPD´s, the sample with the longer Cd and Te growth interval has a EPD nearly the same as the commercial substrate. This leads to the result that due to long growth times without annealing in Cd atmosphere and slightly raised growth temperature the crystalline quality of CdTe (001) is decreased.

Nitric acid has a tendency to affect one element (Cd) more than the other (Te) in CdTe compounds. The excess Te atoms deposit on the crystal surfaces as a polycrystalline layer. Before polishing chemically or etching, the deposited Te layer has to be removed from the surface necessarily. These mixed solution of nitric acid and potassium bichromate (E solution) might generate an oxidation reaction (TeO_2) by oxidizing action of $K_2Cr_2O_7$. Due to the

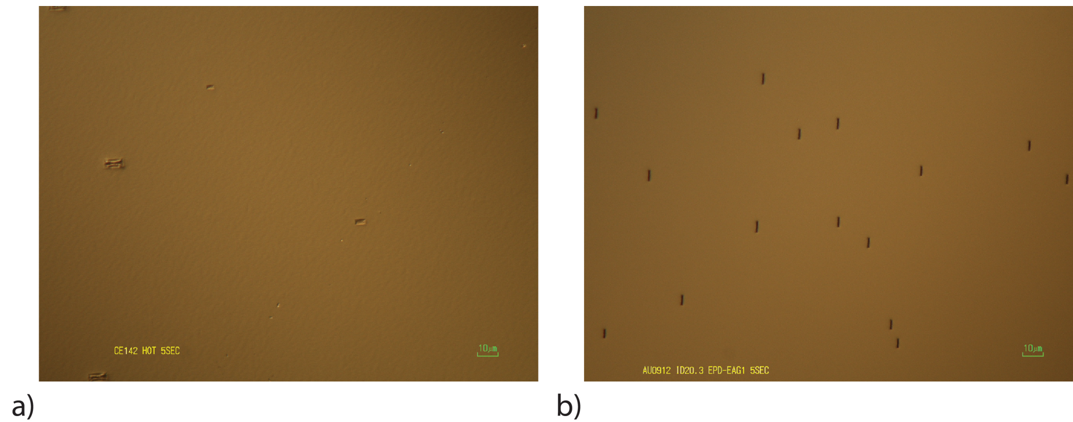


Figure 4.12: CE142 (a) and a commercial CdTe substrate (b) after 5 second etching with diluted EAg-1 at 80°C.

solubility of these resultant TeO_2 in an acidic solution, smooth dissolution of the CdTe surface should be caused without any deposition of Te layers. With the addition of Ag^+ ions into the E solution, etching actions such as dissolution rate and etch pit formation are remarkable controlled. Due to the much lower ionization tendency of Ag than that of Cd, silver ions in the etching solution tend to replace the cadmium atoms at their own lattice sites [104]. According to Iwanaga *et al.* [106] square etch pits were expected on the (001) surface. However as shown in Fig. 4.12, the pits seem actually to be rectangular. Their facets consist of two trapezoids and two triangles because the facets have different etching velocities. Furthermore, H. Iwanaga describes this etch pit density technique for HgTe as well. This could lead to further quality experiments in the future for HgTe.

In summary there is to mention that the crystalline quality due to EPD experiments is very high and comparable to commercial substrates of JX Nippon. But it should still be invented further EPD experiments on CdTe (e.g. EAg-2) to learn more about the CdTe growth parameters to optimize the quality forwards. In addition, these etch solutions can be used for additional characterization experiments for HgTe. However, a new etch solution has still to be invented for HgCdTe. A complete other approach is that the E solution can be used as a chemical polish to flatten the CdTe surface roughness after growth before Hg-based growth. This could lead to smoother surfaces and therefore lower vertical elevations. However, this would maybe induce residual chemicals on the surface which will then effect the Hg-based MBE growth and crystalline quality. The huge advantage of these in-situ grown heterostructure is then lost.

4.3 Summary

In this chapter, the MBE growth and optimization of undoped (001) CdTe on n-doped (001) GaAs:Si was presented. Due to the large lattice mismatch of CdTe and GaAs, a thin ZnTe layer

was introduced to provide growth in (001) direction and the best start of CdTe. Furthermore, the Zn plays an important role in substrate preparation. So, during the cooling down the Zn atmosphere after oxide desorption the GaAs surface remains protected against As desorption but at the same time small holes are left which provide best MBE growth of the following CdTe layer. The duration for best CdTe growth results was identified to around 30 seconds for ZnTe growth at a flux ratio of Zn/Te $\approx$ 1/1.2. For the CdTe growth, a optimized growth process was established which generates 4 μm thick (001) CdTe layers. Here, Cd and Te growth periods alternate with Cd annealing periods over complete growth time of around 14 hours. The Cd/Te ratio was determined to 2:1 for the optimized growth process. The FWHM values of the ω-scans does however not go below the 150 arcsec. The corresponding RMS surface roughness of the CdTe layer was determined to approximately 2.5 nm via AFM. Though, this result has to improved in further experiments to provide smoother start condition for the Hg-based MBE growth. The additional etch pit density experiment showed that the optimized (001) CdTe layer are still in the same quality range as the commercial substrates if just the crystalline surface property is explored. So, the etch pit density of MBE grown CdTe is measured under 5×10^4 cm^{-2} which is clearly located below the etch pit density specification of JX Nippon Materials (1×10^5 cm^{-2}).

5 Undoped HgTe - Quantum Wells

At the end of 2009, there was the decision to substitute the almost 30 years established Riber CMT MBE chamber for a new refurbished one. The reason for this replacement was that the new MBE chamber should deliver samples with higher crystalline quality. This means that the carrier mobility increases while the carrier density remains unchanged. Since the HgTe quantum wells were always doped to explore new physical effects like Rashba-Dresselhaus effect for example. By the discovery of the quantum spin Hall effect (QSHE) the request for samples with very low carrier density emerged. So, the arriving of a new clean chamber without any doping material inside provides a good start for growing undoped samples of high quality. In the following chapters, important results of undoped QWs will be showed and analyzed.

5.1 HgTe QWs on commercial CdTe

In this chapter the crystalline and physical properties of undoped HgTe quantum wells will be discussed and compared to prior samples which were all n-doped. The reason to switch to undoped QWs is that the prior gating method did not allow to tune the Fermi energy from the n-doped regime through the QHSE regime into the p-regime. Furthermore, the opinion was present that n-doped QWs were necessary to get a current leading channel from the QW to the gold contacts where the Fermi energy can not be tuned by the gate. But it turns out that undoped QWs can be contacted very well and by tuning the gate the Fermi energy can now be shifted from the n- into the p-regime. So, all HgTe QWs analyzed in this work thesis were grown on commercial CdTe substrate by default. Here, the substrate is etched by HCl prior to transferring into the UHV system [107]. This step has to be done because the CdTe substrate is covered with a protection oxide. From XPS measurements the oxide thickness is calculated to around 1.5 nm [108]. As it is not possible to remove the oxide by thermal desorption accurately, a chemical etch step has to be performed instead. After the etching procedure the substrate is mounted with liquid gallium (Ga) on a molybdenum block and transferred into the UHV system quickly to avoid re-oxidization. Between all HgTe layers which are put in this way an approximately 100 nm CdTe buffer layer is grown prior to the Hg-based layer at 315°C. The Hg-based layers are typically grown at a substrate temperature T_{sub} = 180°C.

First, it is important to check how the carrier density can be pushed down by not intentional doping the structure. Before this thesis started, the carrier density n of HgTe quantum wells was grown between $n = 5\times10^{11}$ cm^{-2} and a maximum of $n = 5\times10^{12}$ cm^{-2}. The carrier density is typically determined by normal Hall bar measurements (cf. 3.3). In Fig. 5.1 (a), the longitudinal resistance R_{xx} and Hall resistance R_{xy} of a 8 nm quantum well (Q2572) is

plotted against the magnetic field B. This sample exhibits a carrier density of $n = 0.2\times10^{11}$ cm^{-2} at zero volt gate voltage. The gate sweep which is plotted in fig. 5.1 (b) shows that the maximum resistance of R_{xx} is located near to the gate voltage $V_g = 0$ V. Furthermore, R_{xx} is already increasing at $V_g = 0$ V. This means that for this sample with that low carrier density the Fermi level is located within the energy band edge. For carrier densities $n > 1\times10^{11}$ cm^{-2} the Fermi energy lies above the conduction band gap. For most transport experiments the Fermi energy should lie inside the band gap to allow regulated carrier transport. A short compendium of samples with very low carrier density is listed in table 5.1. But this low carrier densities were not reached always. For undoped quantum wells averaging carrier densities of around $n = 2\times10^{11}$ cm^{-2} are achieved by MBE growth. Unfortunately, it is not well-understood if the determined carrier density corresponds to the originally density because a lot of chemical and physical reactions interact with the very sensitive Hg-based layers during lithography. So usually, the lithography process increases the carrier density slightly [65]. For further transport

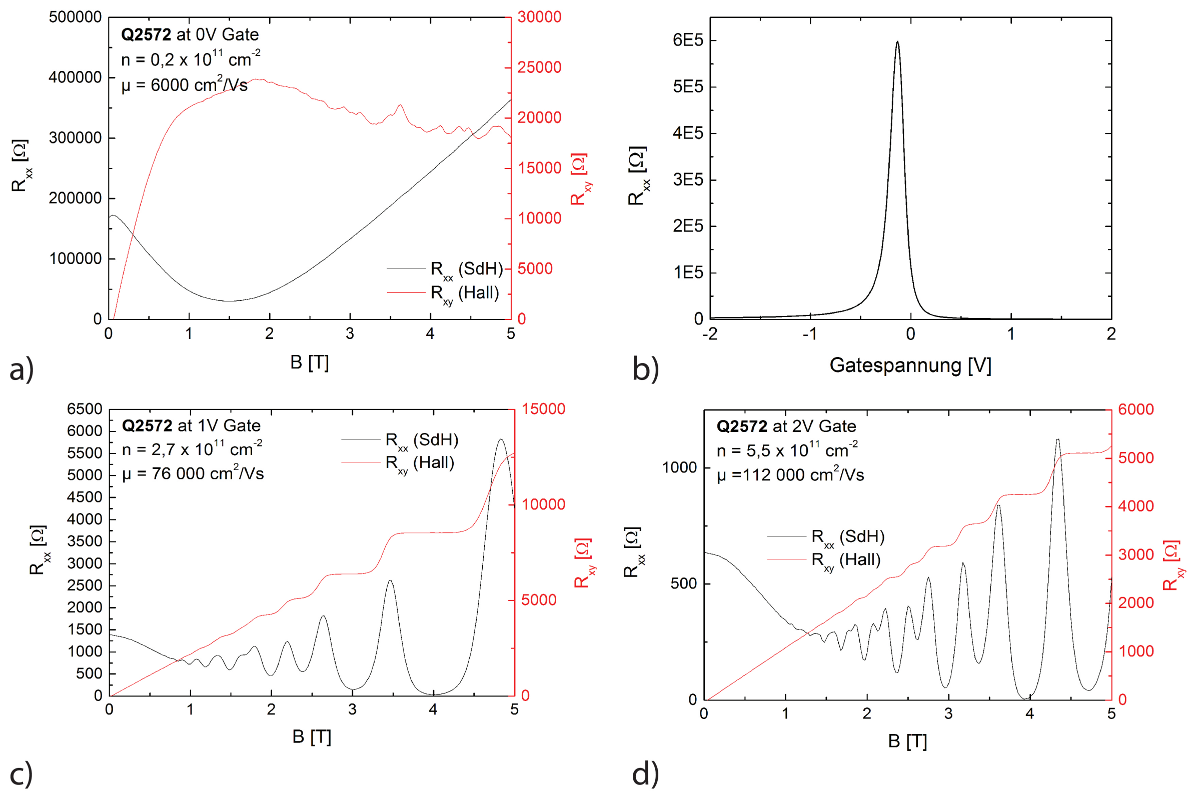


Figure 5.1: a) Standard Hall measurements: the red line indicates the Hall resistance R_{xy} and the black line the longitudinal resistance R_{xx}. b) Gate sweep measurement at zero magnetic field. c), d) Hall measurements for $V_g = 1$ V, 2 V.

analysis of the samples the carrier mobility μ provides information about the crystalline quality and the mean free path of the carrier in the HgTe layer. The larger the mobility the higher is

the quality and the longer the mean free path. The value of Q2572 shown in Fig. 5.1 (a) is around 6000 cm^2/Vs.

This small value is given by the fact that the Fermi energy is located in the band gap and therefore no electron transport through the layer is possible.

Although HgTe is a topological insulator it is expected that a finite longitudinal resistance R_{xx} = h/2e^2 is reached during the gate sweep [7, 31]. Due to the large Hall bar dimensions (600 x 200 μm^2) which are used for standard characterization measurements, there are still some growth defects, grain boundaries and gate influenced defects. These defects produce impurity traps by what the edge transport channels are influenced negatively. To measure the QSH effect, micro Hall bar or special H structures are necessary to have a high probability to probe a sample area without defects and impurities [27].

Sample	$d_{barrier}$ [nm]	d_{QW} [nm]	d_{cap} [nm]	n [$10^{11}cm^{-2}$]
Q2560	59	11	59	0.75
Q2570	200	10	25	0.2
Q2572	150	8	25	0.2
Q2605	72	8	72	0.8
Q2639	52	9	52	0.75
Q2684	141	8	141	0.89
Q2693	51	8	51	0.89

Table 5.1: Undoped HgTe quantum well heterostructures with very low carrier density n.

The carrier mobility is still a nice feature to characterize low density HgTe QWs. Here, the Hall measurement has to be done at gate voltage where the Fermi level is inside the conduction band. This is typically reached at V_g = 1 V. To compare the mobilities with other samples, the carrier density of different samples should be in the same region. In Fig. 5.1 (c) and (d) a standard Hall characterization measurement is shown for two different gate voltages V_g = 1 V (c) and 2 V (d). Here, the mobility increases with higher gate voltages. This matter of fact is true as long as a maximum is reached at a certain gate voltage which is usually far away from standard measurement conditions.

In summary, undoped HgTe quantum wells can be grown with very low carrier density n which is an order of magnitude lower than those grown doped in the previous MBE chamber. The measurement issues caused by the low density can be handled by a gate which is usually on top by default.

Symmetric quantum well structures

First, the analysis of quantum wells via HXRD were shown and discussed. Because a HgTe quantum well has an extent of several atomic layers ($\approx$ 6 - 10 nm), it is very difficult to

measure these small amount of HgTe accurately. The intensity of the diffracted X-ray beam depends on the atomic structure factor and on thickness of the layer. If the quantum well structure is grown with a thicker CMT barrier below than as a CMT cap, which is normally done, it is very difficult to determine the layer thicknesses of these layers by HRXRD ω-2Θ-scans of the used Philips diffractometer. So for calibrating the growth rate of HgTe quantum wells, the general procedure is that a symmetric quantum well structure is grown because the resulting HRXRD diffractogram is more precise to determine than an diffractogram with many different layer thicknesses. Common values are for the the CMT barrier and cap 50 nm, respectively, and for the HgTe a quantum well thickness in the inverted regime is aspired like 7 - 8 nm. The reason of the quantum well thickness is discussed later. The growth rate of HgTe bulk (> 50 nm) is not suitable because the growth start plays a enormous role in the MBE growth together with the used growth rates. Typically, growth rates of around 1 Å/s are aspired because this growth rate provides the lowest recovering rate of residual molecules and highest Hg-based growth quality. Here, the two CMT layers dominate still the HRXRD pattern so that the thickness of the HgTe quantum well can not be determined very precisely with the help of the thickness fringes. Three layer fits with different HgTe layer thicknesses are shown in Fig. 5.2 (a) including a ω-2Θ measurement of a quantum well structure. The barrier and cap dimensions are equal and the quantum well fit thicknesses are 6, 8 and 10 nm, respectively. The requirement of same barrier and cap layer thickness enables a more simplified access to the fit parameters. So according to the fits, there is no noticeable difference in the fringes near the main peaks.

But, for a very high resolving measurement there appears a beat at a certain reflection angle. Up to this beating, the scan shows usual thickness fringes and after that beating the fringes rise up again. The intensity decreases with higher orders of reflection angles due to the damping of impurities and finite dimensions of the sample. So, the quantity of thickness fringes is an indication for the crystalline and interface quality as well. The inset of Fig. 5.2 (a) illustrates the dependence of the quantum well thickness on the reflection angle in an ω-2Θ-scan. With this method it is possible to resolve the quantum well thickness with a precision of about 0.3 nm which corresponds to approximately two atomic monolayers. The ω-2Θ-scan measurements are not very suitable to determine further properties like interface roughness due to the low X-ray intensity. The new HRXRD diffractometer of *Bruker* which was installed in the last months of this thesis can maybe produce new results in the future.

For further analysis, transmission electron microscopy (TEM) can be used to determine the layer thickness or crystalline quality. Here, it was done by TEM specialist Dr. N. Tarakina. Due to the high contrast difference of Cd and Hg, the HgTe layer can be distinguished very clearly. As shown in Fig. 5.2 (b), the layer thickness is determined to 8.1 nm very precisely and matches very well HRXRD measured 8.0 nm. Moreover, the HgTe and HgCdTe layer exhibit a low density of impurity which demonstrates a high crystalline quality. Additionally, the composition of the HgCdTe layer is determined. For this quantum well there is slight variation from the standard grown composition $Hg_{0.7}Cd_{0.3}Te$. This little increase of Hg in the layer can be caused by the substrate temperature, which was to low during growth, or by the wrong flux ratio of Hg and Cd. This small shift in the composition does not play a notable role for transport experiments. The huge disadvantage for determining the QW thickness via TEM is that the preparation for one measurement takes several days. Therefore, it is not suitable for

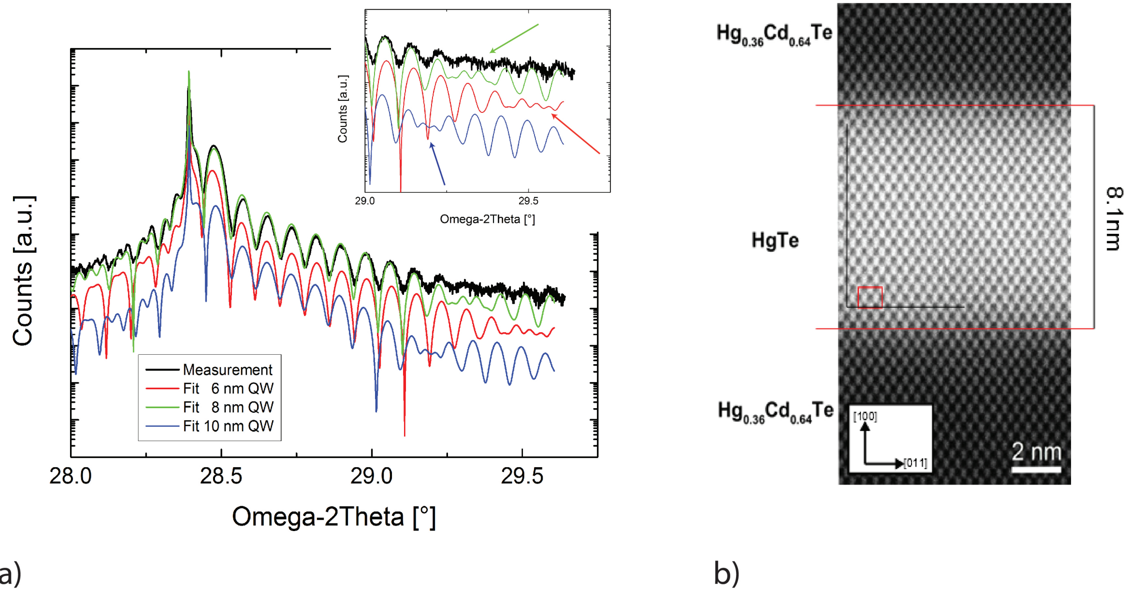


Figure 5.2: a) ω−-2Θ scan (blue) of a quantum well and 3 fits with different quantum well thicknesses. The inset shows the magnification of of the beating corresponding to the QW thickness and the arrows mark their respective beatings. b) TEM measurement of Q2623. The bright layer represents the HgTe quantum well and the dark the CMT layers (TEM by Dr. N. Tarakina).

standard characterization.

HgTe Quantum Well Thickness

Since it is very important to work with samples with high carrier mobilities for transport measurements, the general interest consists in for which QW thickness the mobility exhibits its highest value. In Fig. 5.3 (a) is shown a widespread listing of quantum well thicknesses and their corresponding mobilities. The barrier and cap layer thickness vary here from 25 to 200 nm. The red labeled dots indicate QWs with a carrier mobilities below 50 000 cm^2/Vs. So, the mobility is very low compared to the typical QWs which exhibit mobilities around 200 000 cm^2/Vs. The magenta labeled ones had serious growth problems under which the mobility suffers immensely. Problems are here unstable substrate temperatures, flux irregularities of the used Knudsen cells or relative high background pressure of the MBE chamber. The red line represents a linear fit over all data points. This leads to a distinct increase of the mobility over the quantum well thickness. So, the thicker the quantum well is the higher the mobility up to a certain point. The maximum mobility is confined by crystalline and interface quality. However, the impact of lithography is not to underestimate.

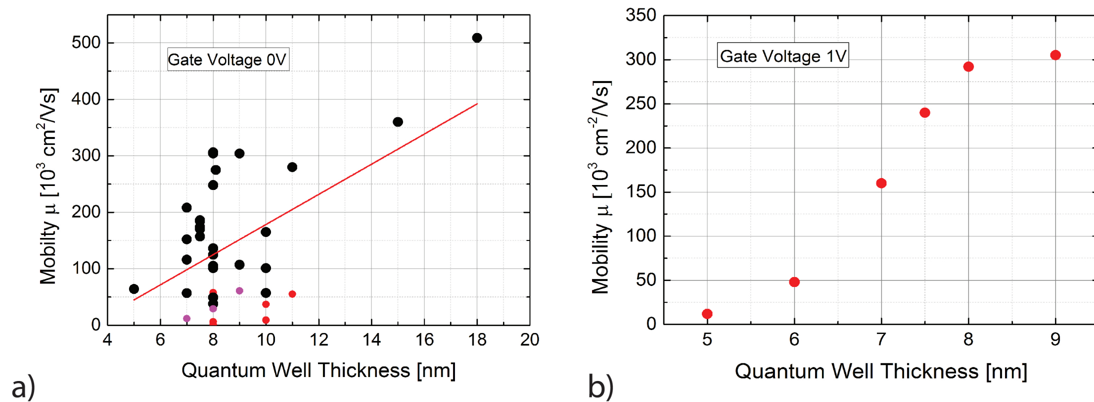


Figure 5.3: a) Statistical application of quantum well thicknesses from 5 to 20 nm and their associated carrier mobilities μ for zero gate voltage. The barrier and cap thicknesses differ randomly. The red line indicates the upward tendency. The magenta dots indicate QWs with growth trouble, the red ones show unusual transport results. b) Growth series with different quantum well thicknesses with consistent CMT layer thicknesses. The carrier mobility μ is plotted versus the quantum well thickness.

Another tendency of growing HgTe QWs by MBE is that the HgCdTe barrier should be not to thin (< 50 nm) to procure high mobilities. Additionally, the HgCdTe cap plays still a big role in terms of high mobilities due to surface protection. This will be more discussed in chapter (5.2) and (6.2).

Furthermore a growth series is shown in Fig. 5.3 (b). Here, during the growth series all growth parameter were not changed except the quantum well thickness. This growth series were executed within a short period of time, so all samples are comparable with regard to MBE, lithography and transport parameters. The carrier mobility is here also plotted against the quantum well thickness. The applied gate voltage is V_g = 1V to exclude to low carrier densities and therefore not meaningful mobilities. This growth series leads to the result that for high carrier mobility samples the HgTe layer should be thick but still in a two dimensional system which is generally around 20 nm for this material system. But for this large thickness values there appears a new problem because the indirect band gap closes at certain requirements which will be shown in the next section. The low mobilities for thin HgTe layers is caused by the quantum well interface. In the Hg-based growth there occurs interdiffusion between the CMT and HgTe layer [110] which generates no sharp edge between HgTe and HgCdTe but defects in the HgTe layer. Furthermore, the HgTe layer layer has to be at least 6.3 nm thick to be in the topological insulator regime. Due to the formation of the topological edge states, this leads to a lower longitudinal resistance and therefore to an increasing mobility.So, Fig. 5.3 (b) shows that the HgTe layer acts like a normal semiconductor and crystalline defects or impurities have a bigger impact on the conductivity. In summary, it is possible by tuning carrier mobility through varying the quantum well thickness. However, the thinner the quantum well is, the lower is the mobility of the 2DEG.

Indirect band gap opening

The rise of mobility is additionally limited by a second effect besides of growth defects and leaving the 2D regime. So this work described in this thesis started with MBE growth on commercial CdTe substrates. In the time before, HgTe lattice matched $Cd_{1-x}Zn_xTe$ (x $\approx$ 0.04) substrates were used as standard substrates. This substrate provides growth of the heterostructure without strain. The switchover to CdTe is founded due to the theoretical prediction of HgTe as a 3D TI. This system has to be grown strained which will be discussed later in chapter (6).

Several transport results of HgTe quantum wells grown on CdTe substrates show unusual low resistance maxima of the small µm - Hall bars fabricated by electron beam lithography [29]. So, first band structure calculations for HgTe quantum wells grown strained on CdTe show a very interesting result. In 2012, Olshanetsky *et al.* [109] shows for a HgTe (001) quantum well thickness of 20 nm that there is still a band gap open between the bands H1 and H2 for an unstrained heterostructure. This calculations based on the eight-band k·p Hamiltonian model. For this thickness there appears indeed a indirect band gap of around 4 meV and no overlap of the conduction H1 and valence H2 bands occurs. If tensile strain is now introduced in the system based on HgTe grown on CdTe, there is an overlap of about 1 meV [cf. Fig. 5.4 (b)]. The splitting of H2 which is indicated by the dashed and solid lines for larger k is based on the Rasba splitting [111, 112, 113].

Since the quantum well thickness did not exceed 15 nm, this calculation by Olshanetsky was not sufficient informatively in the case which is described here. So during his diploma thesis, L. Elsäßer worked out some band structure calculations which match the MBE grown heterostructures [29]. It started with sample Q2570 which should be intentionally grown with

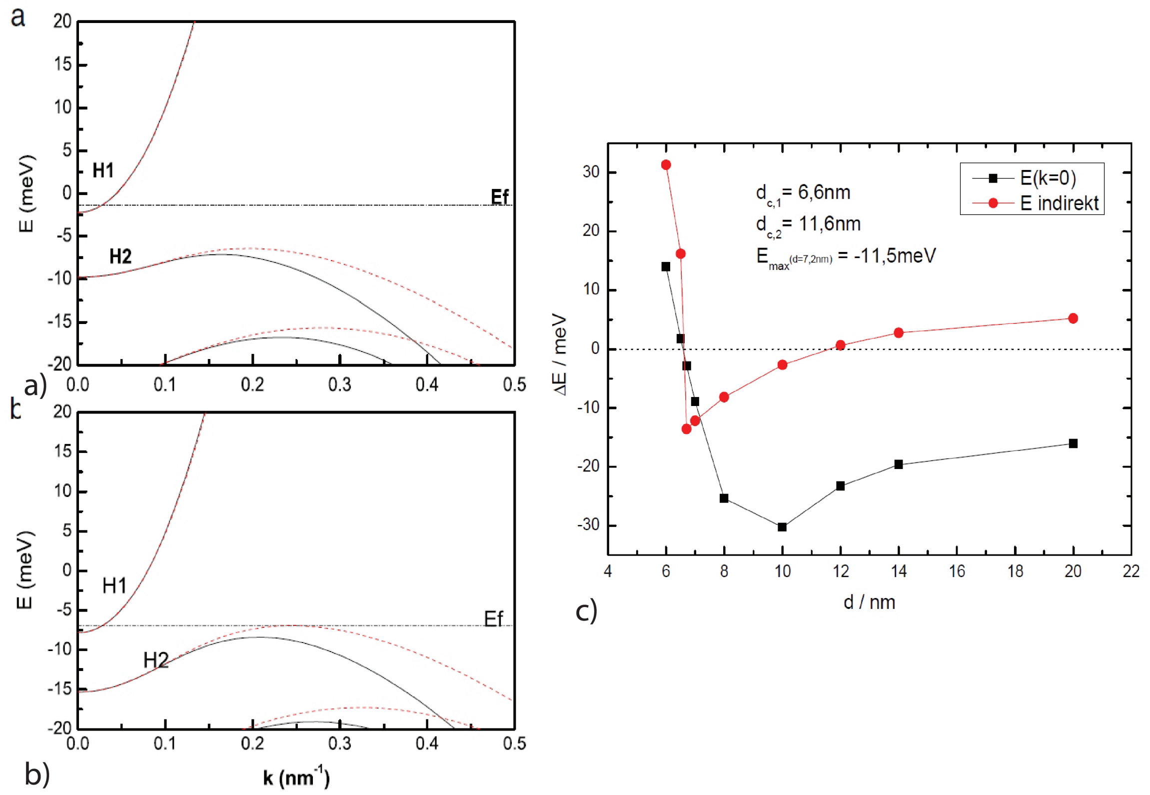


Figure 5.4: Band structure calculations around the Γ-point for a 20 nm HgTe (001) quantum well a) without and b) with strain [109]. In c) is shown: band gap calculations for different quantum well thicknesses. The black dots indicate the direct band gap at the Γ-point and the red dots the indirect band gap [29].

a 10 nm quantum well. Due to a huge difference in the CMT barriers, HRXRD measurement does not determine the thicknesses very precisely. First Hall measurements show an unusual low resistivity. Thereupon band structure calculations based on the 8×8-Kane model were carried out [114]. For Q2570 there occurred problems with the substrate heater so that the temperature was not stable during the growth process. A temperature difference of around ± 1°C happened during growth. Due to this temperature issue, band structure calculations were done for the estimated 10 nm QW and for a 12 nm QW to compare with the transport data. It becomes apparent that the band structure of the 12 nm QW fits more accurately to the experimental data than the 10 nm QW. For the 12 nm QW, the calculated band structure exhibits a inverted band gap of E_g = - 23 meV at the Γ-point. But more important is that the sub-band of H2 in (110) direction exceed the minimum of the H1 band in (011) direction for higher k-values (0.32 $nm^{-1} < k <$ 0.45 nm^{-1}). Therefore, band structure of a half-metal is existent at which the maximum of the H2 sub-band lies $E_{indirect}$ = 0.65 meV above the minimum of the H1 sub-band. For the 10 nm QW, the inverted band gap is E_g = - 30 meV at the Γ-point. However, the indirect band gap amounts a negative value $E_{indirect}$ = - 2.6 meV which represents still a semiconductor. For further research, band structure calculations were done for different QW thicknesses which were grown strained on CdTe substrates. The direct (Γ-point) and indirect band gaps were shown in Fig. 5.4 (c). This means that strained grown 2D HgTe heterostructures show two critical thicknesses for possible measuring the QSHE. On the one hand, the quantum well has to reach the thickness of 6.6 nm to own a inverted band structure and the resultant edge channels. On the other hand, the QW thickness does not have to exceed 11.6 nm because than the HgTe QW is no semiconductor anymore. Here, the maximum band gap of E_g = - 11.5 meV is achieved at a thickness of 7.2 nm. But for QWs thicker than 9 nm, the indirect band gap becomes too small and the sub-band H2 overlaps QSH-state in a large part. Therefore, the edge channel states can not be measured very properly [29].

5.2 Surface 2DEGs

In this chapter, the issue of surface or rather surface-near quantum wells will be discussed. There are two main reasons to grow this kind of QWs. First, there was the attempt that a decrease of the cap layer thickness would extinguish traps states and other impurities which were located in the CMT cap layer. These defects cause charging effects during gate usage and therefore the transport measurements are affected negatively. Furthermore, the gate is located nearer to the quantum well so the efficiency increases. Second, in terms of fundamental research the Majorana bound state is predicted to arise on a interface of a topological insulator and a s-wave superconductor. Therefore, the standard QW design with a CMT cap layer of around 25 to 50 nm has to be thinned and a high mobility QW with very good interface conditions can interact with the superconductor. Theory and first experimental results are written elsewhere [115, 116, 117, 118, 119].

So the topic of this thesis was to investigate the behavior of the quantum well with no CMT cap or with only a very thin cap which still allows to contact the surface states via tunnel junction. The MBE growth is the same as for standard HgTe QWs just with a thinner CMT

cap. Fig. 5.5 shows the carrier mobility of HgTe quantum wells with different CMT cap thicknesses at gate voltage V_g = 1 V. Here, the quantum well thickness differs and has to be taken into account for analysis. The reason for taking the data of 1 V gate voltage is that there is not the Fermi energy in the band gap as described in chapter 5.1. But it is clearly visible that with an increasing cap layer thickness the averaging mobility increases as well. In comparison, a standard HgTe quantum well exhibits a carrier mobility of 200 000 to 300 000 cm^2/Vs at a gate voltage V_g = 1 V. These quantum wells have a CMT cap of minimum 25 nm by default. The two samples with a 15 nm cap thickness reach this standard mobility. But for Majorana experiments this thickness is too large because the superconductor can not interact with the TI through such a big barrier. But in case of trapping states, a 15 nm cap suppresses here hysteresis in the gate sweep. Therefore, there is no sign for charging effects due to gating. The 10 nm cap shows a mobility of 100 000 cm^2/Vs. This is a significant drop but still useful for QSHE experiments.

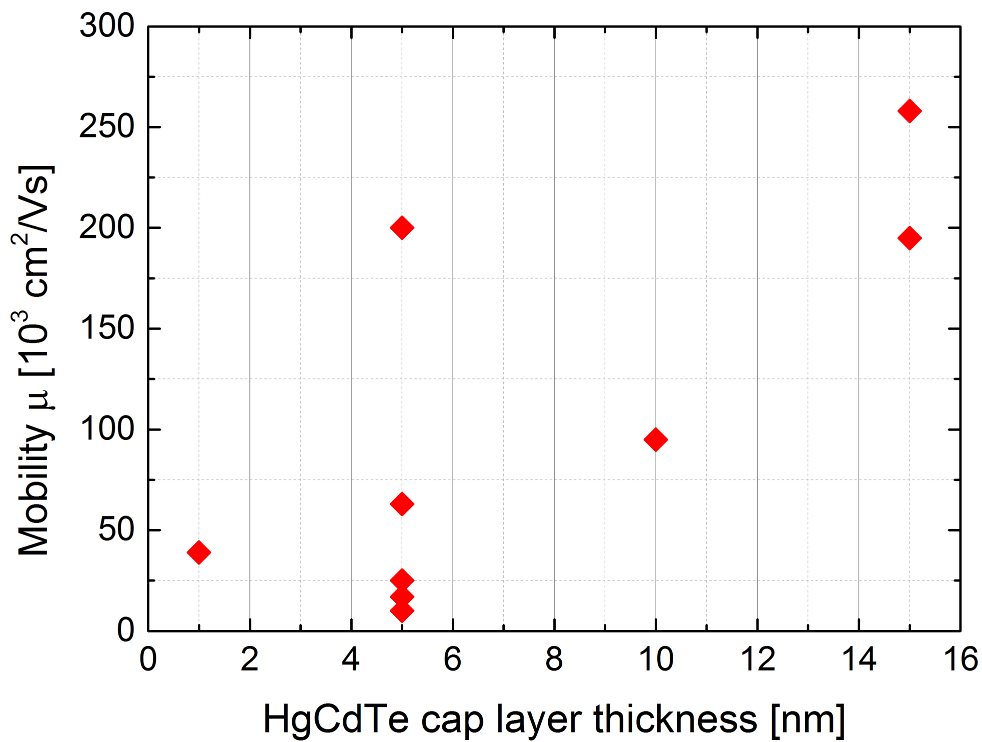


Figure 5.5: Carrier mobility of surface quantum wells is plotted versus HgCdTe cap layer thickness at gate voltage V_g = 1 V. The thickness of the quantum wells varies from 7 to 9 nm.

However, the cap layer thickness has to be further decreased for Majorana experiments. So, several quantum wells with a 5 nm, one with 1 nm and some with no cap layer were

grown by MBE. The Hall measurements of the QWs with no cap layer on top of it could not be evaluated to determine carrier mobility and density because the Hall measurements do not produce resonable data. This means that this samples are not useful for transport experiments due to very low mobility and unknown density. This is explainable due to possible impact to the active HgTe layer. For the following reasons, the sample is transferred out of the UHV system to atmospheric condition because the lithography process is developed for this condition. This allows on the one hand surface contamination and on the other hand oxidization of the HgTe layer. The longer the duration between transferring and starting the lithography process the bigger is the impact of this two effects. However, after a certain time the HgTe oxide operates as protective shield against oxygen. The contamination depends on the handling and the clean room class which is not to underestimate. The surface oxidization will be discussed more detailed in chapter (6.1). Second, the lithography process effects the HgTe layer as well [120, 121]. The resists, developers, sputter materials and temperature changes during the process can cause a decrease in crystalline and interface quality. So, until the lithography process is not transferred into an oxygen-free environment and the process is safe to almost 100 percent for HgTe, surface HgTe quantum wells with no cap layer are not usable for transport experiments.

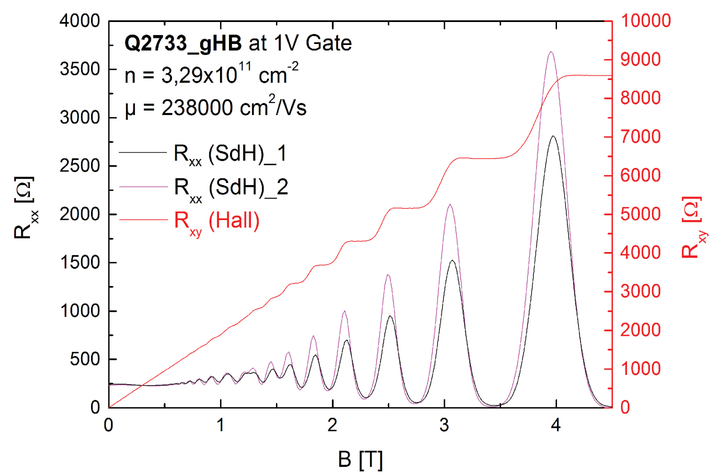
Based on this knowledge, some samples were grown with a cap layer thickness of 5 nm and one with nominal 1 nm. The HgTe surface quantum well with 1 nm cap shows a mobility of $\approx 40\,000$ cm^2/Vs at 1 V gate voltage. This value is comparable to uncapped HgTe bulk samples which were discussed later in chapter (6.1). This 1 nm CMT cap prevents the HgTe layer from intense contamination with reactive materials, but oxidization takes place anyway because the 1 nm is too thin for blocking the oxygen atoms [108]. This means that a 1 nm cap layer protects the HgTe insufficiently but for tests it is useable.

Furthermore, the HgTe QWs with a 5 nm CMT cap present data which are in a good agreement with the previous explanations. So, three samples show very low mobilities under 25 000 cm^2/Vs, one samples around 60 000 cm^2/Vs and another one 200 000 cm^2/Vs. This huge discrepancy in mobilities is however explainable if the quantum well thickness is considered. Just as described in chapter (5.1) the mobility correlates with the quantum well thickness which means that a thicker quantum well generates higher carrier mobility. But here the difference to the previous chapter is that a thicker HgTe layer together with a 5 nm CMT cap serves as a protective shield for the active layer. So, a surface-near part of the HgTe serves as a protection layer. The HgTe layer below which is not affected by surface reactions is getting thicker and therefore there is an increase in the carrier mobility. So the HgTe QW with the 200 000 cm^2/Vs mobility is nominally grown 12 nm thick. The 60 000 cm^2/Vs QW should be 10 nm thick and the three QWs with the very low mobility are 8 nm thick. For further analysis, there has to be performed band structure calculations of this layer structure. Due to this calculations, the real quantum well thickness can be determined.

Furthermore, there has to be done some further growth series where the cap layer thickness is changed by just a nanometer from zero to ten at constant quantum well thicknesses. This would lead to an optimized surface quantum well layer stack.

5.3 HgTe QWs on CdTe/GaAs:Si

As mentioned in chapter (4), the earthquake and the following tsunami caused a lot trouble in Japan and so the CdTe substrate supplier was affected heavily. So it was not possible to deliver CdTe substrates for the next year after the earthquake. This leads to the begin of investigating the CdTe growth on GaAs. During the optimization of the CdTe growth, several HgTe quantum wells were grown to check if the CdTe quality is sufficient for Hg-based heterostructure MBE growth. These HgTe quantum wells were analyzed afterward via Nomarski microscopy, HRXRD and Hall measurements. So as long as the carrier density and mobility of the HgTe QW is not satisfying, the quality of the CdTe is not high enough and a change from commercial CdTe substrates to self-grown CdTe buffer on GaAs substrates is not practical.



a) b)

Figure 5.6: a) Schematic layer stack of a HgTe layer embedded in HgCdTe grown on CdTe/GaAs:Si. b) Hall measurements of a HgTe quantum well (Q2733) grown on CdTe/GaAs:Si in-situ transferred from II-VI- into CMT - chamber.

In Fig. 5.6 (a), a sketch of an undoped HgTe quantum well grown on a CdTe buffer is shown. The proportions do not correspond to reality. The CdTe growth on GaAs is shown in chapter (4). The selection of n-doped GaAs is motivated in using the substrate together with the undoped CdTe buffer as a back gate. Back gating results will be shown in chapter (6). The Hall measurement which is shown in Fig. 5.6 (b) belongs to a HgTe quantum well which is grown on an optimized CdTe buffer. After reaching a satisfying CdTe buffer quality, the CdTe substrates were able to be transferred in-situ from the II-VI- into the CMT - chamber. The Hall measurement provides a low carrier density at 1 V gate voltage and a high mobility. The Hall plateaus reach nicely the expected ones and the SdH oscillations go down to zero longitudinal

resistance at the higher plateaus. However, there is a small difference in the amplitude of the both R_{xx}. This is caused by imperfections of the HgTe crystal in the Hall bar structure. These defects are generated by inhomogeneous MBE growth or defects in the CdTe buffer which continue in the Hg-based heterostructure.

In the following two sections, HgTe quantum wells were discussed which are grown on CdTe buffer. So firstly, it will be discussed the results for samples which were grown on HCl etched CE-substrates because the CdTe buffer was transferred out to atmospheric environment for analyzing the CdTe buffer. Secondly, after completion the CdTe buffer optimization on GaAs substrates the CE-samples were transferred in-situ into the CMT - chamber for Hg-based heterostructure growth.

Undoped quantum wells on HCl etched CE-substrates

During the optimization of the CdTe buffer on GaAs:Si, several HgTe quantum wells were grown on these CdTe buffer after analysis. Since the research is mainly under atmospheric conditions, the samples get oxidized and collect some contamination on the surface. The oxide can be removed by the standard HCl etch process. The samples are afterward mounted on a molybdenum block with liquid Ga. After that, the standard HgTe quantum well growth is performed. RHEED pattern during growth look comparable to HgTe quantum well growth on commercial CdTe substrates.

In table 5.2 all HgTe quantum well samples are listed which were grown on CdTe/GaAs:Si with a HCl etched CdTe surface. The CdTe thicknesses of the CE-samples differ from 1 to 4 μm and the method of the CdTe growth and therefore there is a certain time development of the CdTe quality included which is not directly listed in the table. Furthermore, the HgTe heterostructure vary in barrier, quantum well and cap layer thickness. This excludes the effect on the result of the heterostructure. Moreover, only the carrier density and mobility for zero gate voltage is shown because the Fermi energy is not in the band gap. Therefore, the mobility results are still meaningful at zero gate voltage.

The most important result of this samples series is shown in the carrier density n. Compared to the densities which were shown in chapter (5.1) these carrier densities are significantly higher. While n is often explicitly below 1×10^{11} cm^{-2} on the commercial CdTe substrates, which were etched before by HCl as well, all HgTe quantum wells show an average density of around 4×10^{11} cm^{-2} at zero gate voltage. By comparing the heterostructure, all samples demonstrate almost similar densities. The very high carrier density of sample Q2668 is caused by lithography problems (liftoff; evaporation of the gate structure). The slightly higher densities of Q2705-1 and Q2706-1 is probably a result of the CdTe buffer (CE96) which is grown in a different process than CE69. Furthermore, surface residuals of the HCl etch can affect the growth of the HgTe QWs and this would lead to a different density, respectively. Roughness measurements via AFM or HRXRD-ω-scans do not give further information on the density discrepancy. However, some contamination and etch residuals remain on the CdTe surface after transferring into the UHV system. This residuals may generate growth defects which will increase the carrier density.

Another point is to how the mobility is affected by the HCl etch before HgTe growth.

Sample	substrate	$d_{barrier}$ [nm]	d_{QW} [nm]	d_{cap} [nm]	n (0V)	μ (0V)
Q2506	CE3	55	8	55	1.31	101
Q2636	CE69	50	8	50	4.80	31
Q2653	CE69	300	8.5	25	4.20	73
Q2654	CE69	300	8.5	25	4.48	43
Q2655	CE69	200	8.5	25	3.20	57
Q2656	CE69	200	8.5	25	2.50	52
Q2657	CE69	100	8.5	25	3.60	39
Q2658	CE69	100	8.5	25	1.36	39
Q2668	CE78	100	7.5	25	7.90	28
Q2705-1	CE96-1	100	8	50	5.39	304
Q2706-1	CE96-3	100	8	50	6.19	306

Table 5.2: Undoped HgTe quantum wells grown on CdTe/GaAs:Si. The substrates were transferred out of the UHV system due to analysis. Before reentering the UHV for the Hg-based heterostructure, the CdTe/GaAs:Si is etched by HCl. The carrier density n is presented in 10^{11} cm^{-2} and the carrier mobility μ in 10^3 cm^2/Vs at zero gate voltage.

There are three different parts of mobility values. First, the two highest mobilities ($\approx$ 300 000 cm^2/Vs) were measured in quantum wells grown on CdTe buffers which were fabricated by nearly optimized growth process as described in chapter (4). This CE96 sample has a FWHM in the ω-scan of 210 arcsec. The CdTe buffer of sample CE3 shows a FWHM of 376 arcsec while commercial CdTe substrates exhibit a FWHM of around 20 arcsec. However, the difference in the FWHM values underlies partially the CdTe thickness ($d_{CE3} \approx 2$ µm; $d_{CE96} \approx 4$ µm; $d_{commercial} \approx 800$ μm). However, the crystalline quality of sample CE96 lowers more the FWHM. This slight difference leads to a decrease of the mobility of about 60 percent. The surface roughness of these two CdTe buffers differ notable (RMS_{CE3} = 3.56 nm; RMS_{CE96} = 2.16 nm) and this can also lead to a rise of the mobility from Q2506 to Q2705-1/Q2706-1. All other samples show almost similar mobilities and densities except the density of Q2668. The RMS measured via AFM show for all these samples the nearly the same value (RMS $\approx$ 0.75 nm). This nearly-smooth CdTe surface is generated by very short growth period of CdTe. As explained in chapter (4), this leads directly to very high FWHM values of around 830 arcsec. Besides of the thickness issue, this means that the crystalline quality of the CdTe layer is very low and the defects and grain boundaries may continue into the Hg-based heterostructure. This results in low carrier mobilities.

In summary, HgTe quantum wells grown on previously HCl etched CdTe/GaAs:Si substrates show a clear increase in the averaged carrier mobility. This is probably caused by etch or contamination residuals which have an impact on the heterostructure growth. The car-

rier mobility seems to be almost unaffected. However, the crystalline quality of the substrate represented by the FWHM value of an HRXRD-ω-scan is here more relevant to the carrier mobility μ. CE-substrates with high FWHM values provide low mobilities. Compared to the undoped quantum wells of section (5.1) which pass basically through the same Hg-based growth process starting with the HCl etching, the QWs on CdTe/GaAs:Si show higher average carrier densities while mobilities are comparable. The FWHM of the commercial substrates are around 15 arcsec. This leads to the result that the crystalline quality of the CdTe substrate influences still the carrier density in a certain way but the effect is too small in HgTe QWs grown on HCl etched CdTe/GaAs:Si substrates. In the next section, in-situ transferred HgTe quantum wells grown on CdTe/GaAs:Si deliver some new information about the HCl etch process and its disadvantages.

Undoped quantum wells on in-situ transferred CE-substrates

After optimization of the CdTe buffer growth on GaAs:Si, the substrates were transferred in-situ from the the II-VI chamber to the CMT - chamber. So, the samples do not see any atmospheric air which means no oxide is formed on the CdTe surface. So after entering the CMT - chamber, the samples do not need an additional CdTe buffer layer and the growth of the Hg-based heterostructure should be started instantly. An extra CdTe layer does not improve the quality of the surface observed by RHEED. So, stress of heating the sample again to T_{sub} = 315°C is avoided. The 2×2 reconstruction in RHEED which is generated by cooling down in Cd atmosphere in the II-VI chamber disappears at growth temperature T_{sub} = 180° again and the CMT growth starts on a 2×1 reconstructed CdTe surface. Therefore, the CdTe surface is Te terminated because Cd is very unstable at Hg-based growth temperatures. After the HgTe quantum well growth, the sample is transferred out of the UHV for analyzing.

While the commercial CdTe substrates are mounted by liquid gallium (Ga) on a molybdenum block, the Ga is not usable here. Because for thermal desorption of the oxide on the GaAs:Si substrates, temperatures up to nearly 640°C are required. Therefore, only indium (In) offers stability at these temperatures. Substrates mounted with Ga would drop off during this heating process. This change of glue does not influence the HgTe growth but afterward a problem occurs in matters of detaching the sample off the molybdenum block. Due to the temperature instability of HgTe, Hg-based samples should never see any temperatures over 80°C again after the growth. Therefore, Ga glue is very proper because the samples can be detached at a temperature of around 40°C. For detaching In glued substrates, temperatures are necessary around 200°C. As it is not possible to avoid this high temperatures until now, the sample is detached by a scalpel after around ten seconds at 200°C. The acquisition of a contact-less real-time temperature monitoring system (BandiT [122]) will here avoid these temperature stress in the future by glue-free mounting of the substrate.

Distinctive features of in-situ grown QW structures compared to the HCl etched samples are presented in Fig. 5.7. Nomarski pictures of two representative show in two different magnifications (a, b = 50× ; b, d = 1000×) important differences. So, HgTe quantum wells (Q2733) grown on HCl etched CdTe substrates show a lot of large defects and residuals (a). Round defects appear over the whole 10×10 mm^2 sample and get larger closer to the sample

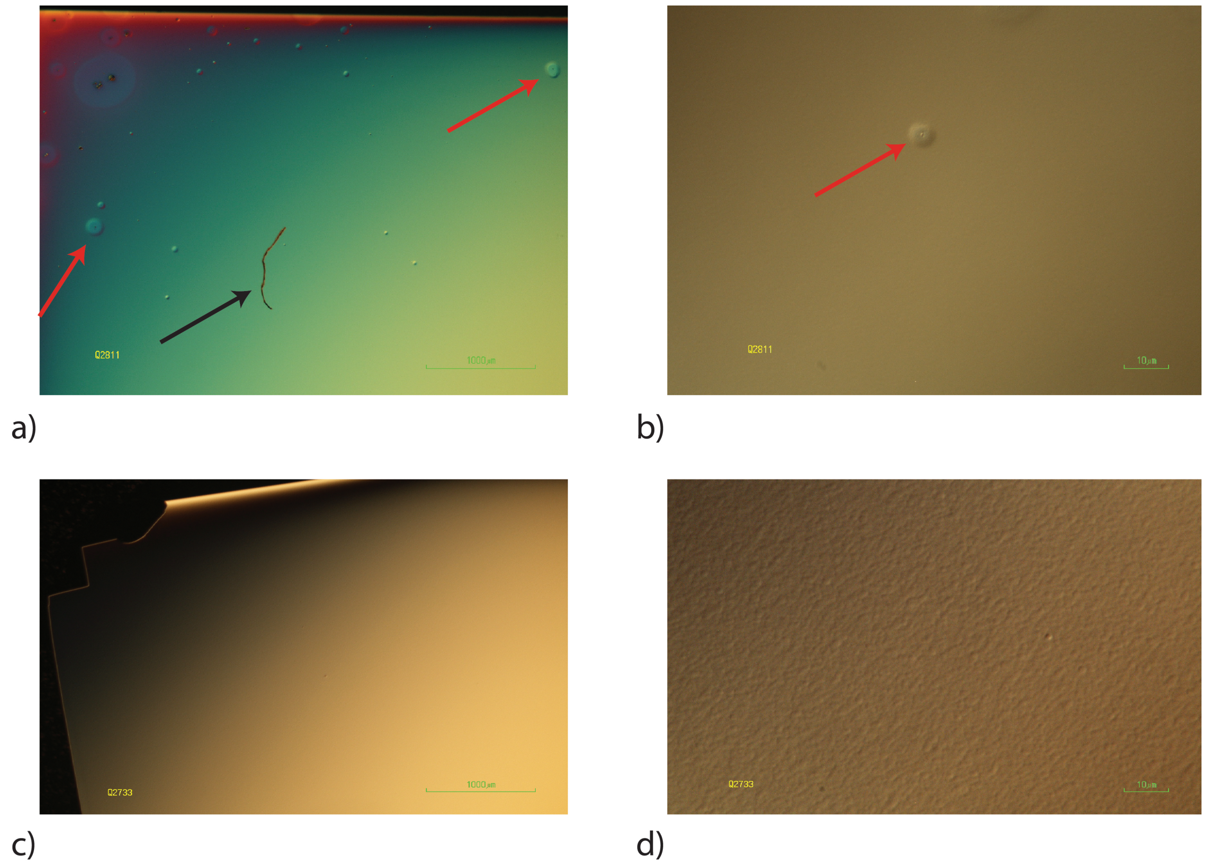


Figure 5.7: Comparison of a HCl (a, b) etched CdTe substrate and in-situ transferred (c, d) HgTe quantum well structure by Nomarski microscopy at different magnifications. The red arrows show some typical so-called volcano-defects which arise usually after HCl etching the substrate. The black arrow shows a etch residual.

edge. These round defects are called volcano defects due to their shape. The origin of these defects is not completely understood. First research results show that titanium (Ti) is detected by EDS at the center of the defect [10] which prevents HgTe growth within splitting distance. Furthermore, some large dirt particles can be found on the sample (Q2811) which is placed there due to the chemical etching and transferring at atmospheric air. If an in-situ transferred sample (c) is compared to a HCl etched one (a), no volcano defects, etching residuals or dirt can be determined by Nomarski microscopy. Furthermore, the samples transferred in-situ into the CMT - chamber show assimilable carrier densities and mobilities over the whole sample. Usually, the sample size of in-situ transferred HgTe quantum well samples is a quarter of a round two inch wafer. Fig. 5.7 (b) and (d) show the same samples as in (a) and (c), just in higher magnification. Here, the sample grown on in-situ transferred CdTe substrate exhibits a rough surface structure ($RMS_{AFM} \approx 2$ nm). In contrast, the sample grown on HCl etched commercial CdTe substrate is very smooth and flat without growth defects or similar ($RMS_{AFM} \leq 0.8$ nm). Only one small volcano defect is visible. This means that the crystalline quality of the Hg-based heterostructure is very high on a HCl etched commercial CdTe substrate except in the immediate vicinity of an volcano defect or an other residual. However, it is often very difficult to find an area suitable for the Hall bar structure without such a defect inside. The rough surface of the quantum wells grown on in-situ CE-substrates deduces to suspected low mobilities and high carrier densities induced by the growth defects. However, Nomarski microscopy is not a very precise method to determine crystalline quality.

Therefore, HRXRD measurements provides high quality analysis of the crystal. In Fig. 5.8 an ω-2Θ-scan of an in-situ transferred symmetric HgTe quantum well (Q2829) is illustrated with its corresponding fit. Compared to the measurement shown in Fig. 5.2 (a), this scan looks a little bit different. Due to the roughness of the CE-substrates, the interfaces are not very sharp and therefore the intensity of thickness fringes decreases rapidly. Furthermore, the CdTe CE-substrate peak is broader compared to the commercial CdTe peak which means that the crystalline quality of the CdTe buffer is not similar as the commercial CdTe substrates. This causes growth defects which originate in the CdTe buffer and sustain in the Hg-based heterostructure. The beating which usually indicates the quantum well thickness very precisely is not resolved even in an overnight scan with a very large integration time (23 seconds). So as a result, it is only possible to determine to some extent accurately the layer thickness of HgTe QWs grown on CE-substrates with low FWHM values ($\approx$ 150 arcsec) and with a long integration time during the scan ($\geq$ 15 seconds).

However, the characterization measurement with the most important statement is the transport Hall measurement. Standard Hall bar structures of these QWs were fabricated and characterized. The results are shown in table 5.3. All CE-substrates were grown with the optimized growth process described in chapter (4) except CE83 which just has one cycle of 300 times 30 seconds Te and Cd and 10 seconds just Cd. This can maybe explain slightly higher carrier density n and lower mobility μ compared to Q2688. These two samples are fabricated and measured within nearly the same time interval, so the lithography process did not change in that time range. This means that just the quality of the CE-substrate lowers the transport quality of the HgTe QW. Besides that, it is clearly visible that the carrier densities of the HgTe quantum wells lie much lower for the in-situ transferred QWs than the HCl etched ones. This is shown in particular in the comparison with samples Q2705-1 and Q2706-1. These two HgTe

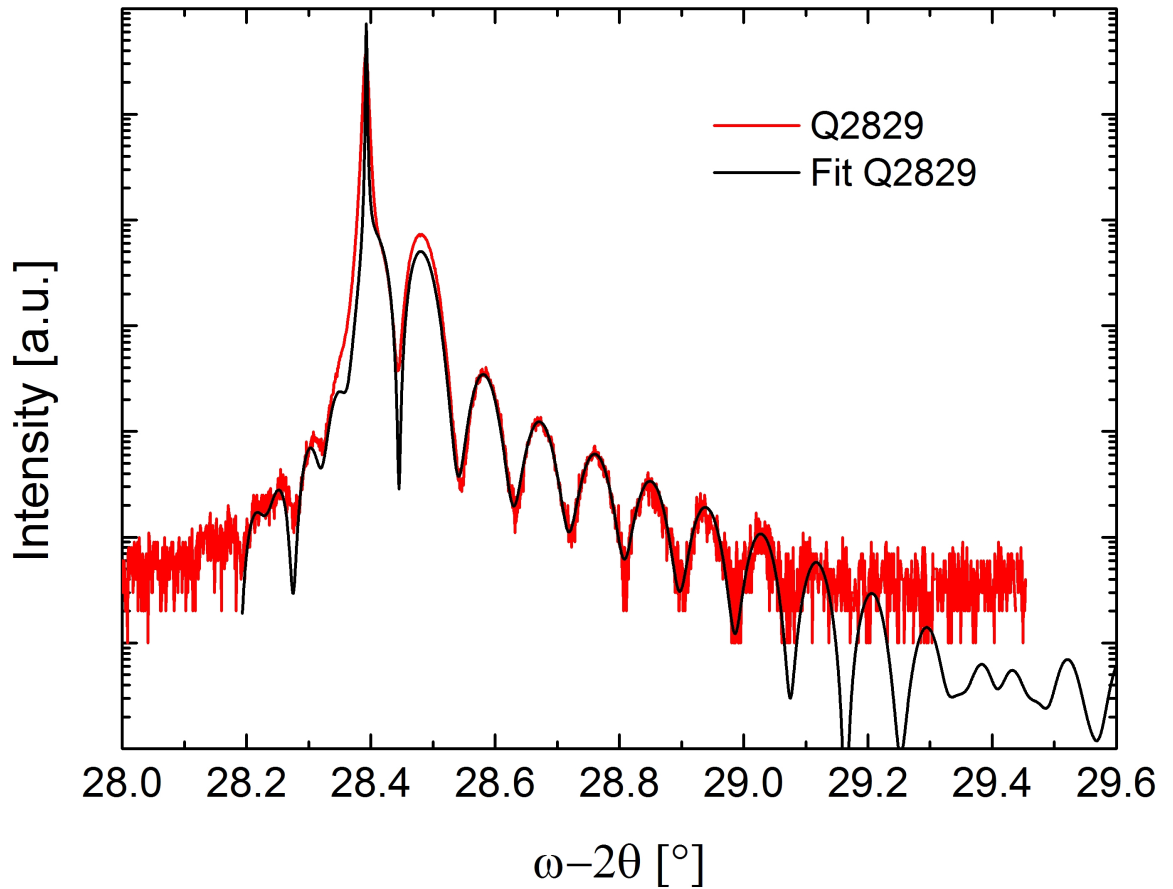


Figure 5.8: ω-2Θ scan of a symmetric HgTe quantum well (Q2829) on pregrown CdTe buffer on GaAs:Si transferred in-situ from the II-VI MBE chamber to the CMT - chamber without seeing atmospheric conditions.

samples were grown on comparable CE-substrates. While the mobilities exceed μ = 300 000 cm^2/Vs, the carrier densities of these two samples is double the value of the averaged mobility value (0.86) of the in-situ transferred samples. The outcome of this is that the in-situ transfer provides much lower carrier densities in HgTe quantum wells compared to HCl etched QWs also grown on CE-substrates.

Sample	substrate	d_b [nm]	d_{QW} [nm]	d_{cap} [nm]	n (0V)	μ (0V)	n (1V)	μ (1V)
Q2677	CE83	100	7.5	50	1.15	108	4	178
Q2688	CE89	100	7.5	50	0.63	278	1.8	428
Q2724	CE110	191	9	25	0.60	110		
Q2726	CE111	180	9	25	1.10	230		
Q2733	CE115	100	7.5	50	0.82	130	3.3	240
Q2737	CE120	100	5	50	0.45	0.7	2.36	12
Q2741	CE122	100	6	50	0.76	5.1	2.4	48
Q2743	CE123	100	7	50	0.86	93	3.35	160
Q2745	CE124	100	8	50	1.78	259	2.85	292
Q2746	CE125	100	9	50	0.70	195	1.9	305

Table 5.3: Undoped HgTe quantum wells grown on CdTe/GaAs:Si. The transfer out of the II-VI chamber into the CMT - chamber occurs in-situ so that chemical etching is not necessary. The carrier density n is presented in 10^{11} cm^{-2} and the carrier mobility μ in 10^3 cm^2/Vs.

The carrier mobilities, however, are not affected by in-situ transferring. So, high mobilities around 200 000 cm^2/Vs are reached for zero gate voltage. The low mobility values for Q2737, Q2741 and Q2743 are caused by the quantum well thickness. As shown in Fig. 5.3, the carrier mobility is dependent on the QW thickness. Furthermore, Landau-level fan charts show a reduction of the quantum well thickness of around 0.5 to 1.0 nm to the estimated thickness [123]. The estimated QW thicknesses is projected by former growth rates. This leads to the conclusion that the growth rates are different for growing on commercial CdTe and pregrown CdTe buffer on GaAs:Si and consequently the rates have to be adjusted to the substrate as well. Together with a Landau-level fan chart, the quantum well thickness can be calculated with the 8 $\times$ 8-Kane-model. Landau-level fan charts are Hall resistance R_{xy} measurements plotted in the derivative of the conductivity σ_{xy} with the magnetic field on x-axis and the gate voltage on the y-axis. The derivation value of the conductivity σ_{xy} is indicated by a color difference. Therefore, Landau-level fan charts demonstrate a good overview of the Hall plateaus and the band gap. Due to the high values of mobility μ, these in-situ transferred HgTe quantum wells grown on CdTe/GaAs:Si exhibit high crystalline quality with low defect density. Therefore, these HgTe QWs can keep up with the QWs grown on commercial CdTe substrates in matters of carrier density and mobility. However, the mobilities of quantum

wells grown on commercial CdTe substrates can reach values of μ over 1 000 000 cm^2/Vs [see Q2369 (not published)] whereas the mobilities here saturate at around 500 000 cm^2/Vs.

But this saturation of the carrier mobility μ is just one disadvantages of the HgTe quantum wells grown on CdTe/GaAs:Si substrates in contrast to many interests. So to increase the mobility, the quality of the crystal and surface of CdTe has to be improved. Furthermore, QWs grown on CdTe/GaAs:Si substrates involve some challenges relating to lithography and transport measurement. In lithography the CdTe buffer on GaAs is not fully comparable to commercial CdTe substrates because the growth of CdTe on GaAs causes some growth defects which open here preferential etch directions. Additionally, the resist and developer parameter have to be adjusted new due to the rough surface texture and temperature connection due to the GaAs substrate. So, a HgTe quantum well fabricated without lithography problems is a first sign to an efficient sample.

Another negative point of these quantum well structures appears during transport measurement indirectly. Due to the roughness of the surface, the insulator and gold top gate resume the hilly surface structure. This happens because the insulator is deposited by PECVD (plasma-enhanced chemical vapor deposition) and the gold gate via metallization. These two techniques do not only compensate the surface roughness but also deteriorate the surface. So, this roughness inducted gating problem occurs because the electric field of the gate influence the quantum well in-homogeneously. This leads to the case that somewhere the Fermi energy is in the band gap and somewhere other not. This would result in an unconvincing measurement. So in summary, HgTe quantum wells grown in-situ on CdTe/GaAs:Si show very nice Hall measurements with its associated carrier densities and mobilities. Furthermore, these two transport properties are very similar over a quarter of an two inch wafer. Compared with the 10×10 mm^2 commercial CdTe substrate, this leads to an almost quadrupled quantity of equal sample pieces. But due to the roughness of the CdTe buffer, the lithography and transport measurements need to be handled with care.

5.4 Pre-Growth Preparation: HF Etching

During the years of this thesis, there occurs consistently some etching problems of the CdTe substrates. Due to the natural oxide on the surface of CdTe, both commercial and pregrown CdTe substrates have to be treated with oxide-removing chemicals before transferring the substrate into the UHV system. Several years ago, a special etching procedure with HCl acid was developed and launched. However, this etch leads to volcano defects as described in the section before and other surface contamination which influence the MBE growth of the Hg-based heterostructures dramatically. The analysis of the problems of the HCl etch provides however no result. Therefore, the request of an alternative etching method appeared. So due to the well-known fact of etching oxides well, several tests were done with hydrofluoric acid (HF) as oxide etchant. A list of the sample properties is shown in table 5.4. Almost all HgTe heterostructres were grown on CdTe/GaAs:Si substrates except one which was grown on commercial CdTe substrates for comparison. There was grown also a capped HgTe bulk sample in this series. The etching result is not influenced by this other type of topological insulator which will be discussed more precisely in the chapter (6). Furthermore, the substrates of Q2705, Q2706 and Q2707 were divided in halves, so one part is etched with the old HCl method and the other part is etched 30 seconds just with undiluted HF (50%). Both substrates are mounted afterward rapidly next to each other in the middle of the same molybdenum block with liquid Ga. This secures same growth conditions and therefore the two samples are comparable at their best. The sample size is just 10×5 mm^2, so both substrates are in the optimized growth area of the molybdenum block. The CE-substrates are grown by the optimized CdTe/GaAs:Si design.

Sample Q	Substrate	Etch	d_b	d_{QW}	d_{cap}	n (0V)	μ (0V)	n (1V)	μ (1V)
2705-1	CE96-1	HCl	100	8	50	5.39	304 000	6.27	326 000
2705-2	CE96-2	HF	100	8	50	5.08	281 000	5.98	306 000
2706-1	CE96-3	HCl	100	8	50	6.19	306 000		
2706-2	CE96-4	HF	100	8	50	5.71	335 000		
2707-1	CE99-1	HCl	200	70	10	4.17	171 000	4.86	175 000
2707-2	CE99-2	HF	200	70	10	5.11	160 000	7.74	216 000
2713	Nikko CT	HF	52	11	52	3.17	362 000	4.25	411 000

Table 5.4: Listing of several HgTe QWs grown on pregrown CdTe/GaAs:Si and Nikko CdTe substrates. d_b, d_{QW} and d_{cap} indicate the barrier thickness, quantum well thickness and cap layer thickness in nanometer. The carrier density n and carrier mobility are shown for gate voltage 0 V and 1 V. The unit of n is 10^{11} cm^{-2} and of μ 10^3 cm^2/Vs.

First, the carrier density n changes again compared to the in-situ transferred HgTe quantum wells grown on CdTe/GaAs:Si. While these undoped in-situ grown QWs show low carrier

densities of $n \approx 1\times10^{11}$ cm^{-2}, both HCl and HF etched quantum wells exhibit higher carrier densities in which there is no tendency which etchant produces a higher density. So the average density is around 5×10^{11} cm^2 at zero gate voltage. This is a usual density of HgTe quantum wells grown on etched CdTe/GaAs:Si where the CdTe buffer is grown by the optimized growth design. Furthermore, the carrier density differs just slightly for each of the two samples mounted on the same molybdenum block together. Only the density of the quantum well grown on a commercial CdTe substrate shows a minor value than the density of the CdTe/GaAs:Si substrates. However, this is in a good agreement with the previous sections. In this sections the results show that the HgTe quantum wells grown on commercial CdTe substrates exhibit a lower carrier density on average than the quantum wells grown on etched CdTe/GaAs:Si substrates.

Moreover, for a complete electronic transport analysis the carrier mobility μ has to be checked. Here, all samples show carrier mobilities over 160 000 cm^2/Vs at zero gate voltage. Furthermore, the mobilities do not differ very far for the two samples which were mounted on the same molybdenum block and etched by different chemicals. In addition, this is also a nice evidence of a uniform growth on a larger sample size than 10×10 mm^2. The mobility of sample Q2713 is a little bit higher than the samples grown on CdTe/GaAs:Si substrates. This leads together with the lower density to the conclusion that HgTe quantum wells show better transport results on commercial substrates and it does not matter which etchant is used. So, for transport experiments it does not play a role whether HCl is used for oxide etching or HF.

However, defects which were mentioned in the prior section appear on samples grown on commercial CdTe substrates etched with HCl. The main reason to change from HCl to HF was to avoid this volcano defects and surface contamination with chemical residuals. Here, a big difference is that the substrate is not rinsed with ultra-pure water after the etch at the HF etching process. Here, the etched substrate is blow-dried by ultra-pure nitrogen.

The Nomarski pictures in Fig. 5.9 show the influence of both etching processes to the sample. Since the volcano defects appear randomly, all samples of this growth series do not present anything like that. Here, only some small dirt is ascertainable which is marked by the red arrows (cf. Fig. 5.9 (a), (c)). Because this dirt is located near the substrate edges, the suggestion is close that these dirt is caused by etching residuals or cleaving remains. Furthermore, this dirt does not affect the Hg-based growth compared to the volcano defects which extend over a large area. In addition, the close-ups in Fig. 5.9 (b) and (d) (magnification: 1000-times) show no transformation of the substrates. The HF and the HCl etched sample show the same rough surface structure (AFM).

Furthermore, both samples exhibit square-based growth defects. These pyramid-like defects are caused by MBE growth conditions slightly notwithstanding of the perfect ones in combination with substrate defects. The origin of these pyramid defects is discussed more in detail in the dissertation thesis of S. Oehling [48]. Moreover, the HF etched sample (Q2707-2) shows a little bit more of these defects which can be interpreted negatively. This may explain the slight increase in carrier mobility and a slight decrease in carrier mobility in this particular sample. This tendency attends similarly for samples Q2705-1 and Q2705-2. The HF etched sample (Q2705-2) shows more pyramid-like defects and exhibits a lower carrier mobility. For samples Q2706-1 and Q2706-2 a statement about defect quantity is not potential.

Additionally, HRXRD measurements were performed to check if there is any crystalline

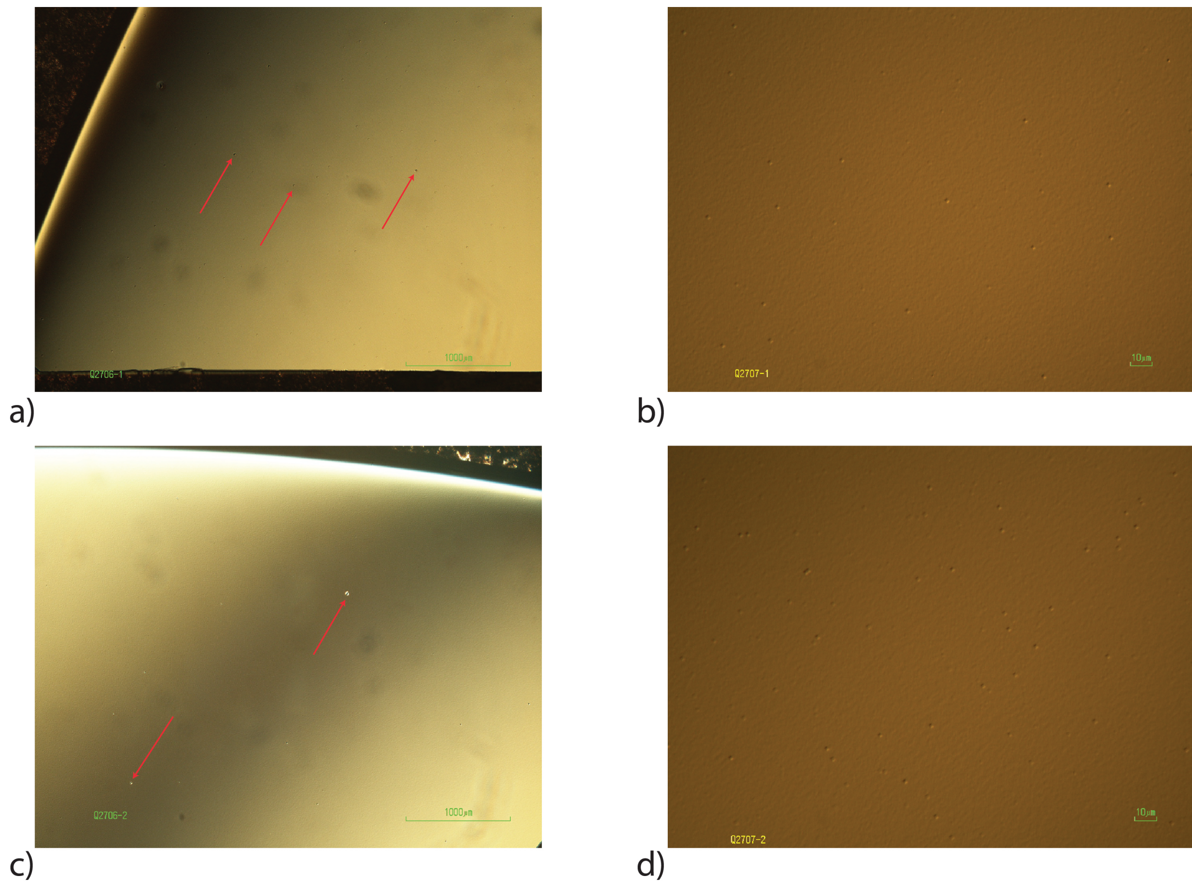


Figure 5.9: Comparison of HCl (a, b) and HF (c, d) etch at different magnifications by Nomarski microscopy. The red arrows mark some etching residuals or cleaving remains.

difference identifiable. So, Fig. 5.10 (a) shows the ω-2Θ-scans of samples Q2705-1 (blue) and Q2705-2 (magenta). As it can be seen clearly, booth scans do not distinguish. The small offset in intensity can be explained by a slight difference in adjustment for the scan and this is not to prevent. Therefore, there is no significant difference detectable by HRXRD which means that the two samples mounted on the same molybdenum block grew with the same quality independently of the etching chemical HCl or HF. So, this result matches with the transport data.

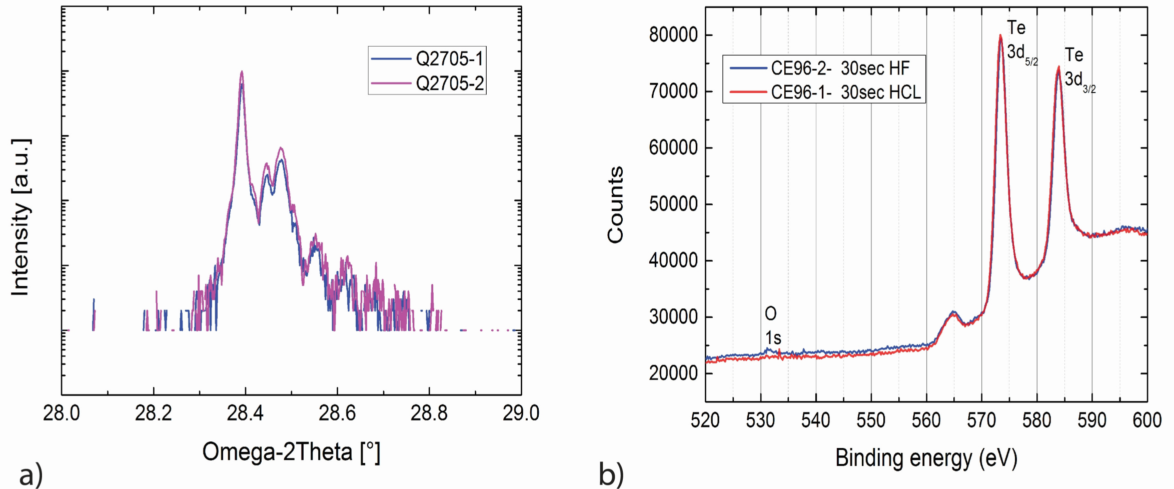


Figure 5.10: a) ω-2Θ scans of samples Q2705-1 und Q2705-2. b) XPS measurements of an HF (blue) and a HCl (red) etched CdTe substrate.

At least, the oxide contamination of the CdTe substrate was researched via XPS. The resulting data of substrates CE96-1 and CE96-2 are presented in Fig. 5.10 (b). A small area of the binding energy is sufficient to analyze the oxidization of CdTe. The binding energy of Te $3d_{5/2}$ and Te $3d_{3/2}$ in a CdTe crystal is located at $E_B \approx 572$ eV and $E_B \approx 582$ eV, respectively [124]. Oxidization of CdTe would lead to a shift for the $3d_{5/2}$-peak to $E_B \approx 576$ eV. The small difference of about 1.5 eV between theoretical and the experimental values is caused by the measuring setup. Furthermore, the oxygen peak can be found at $E_B \approx 531$ eV for a 1s-electron. So, both etchants provide a oxygen clean CdTe surface according to both Te peaks. Of course, there is still a finite quantity of oxygen at the surface but the resolution of the XPS is restricted. However, a small difference is measurable for the oxygen peak. Here, the HF etched substrate shows a small raising. Otherwise, the HCl etched CdTe substrate shows a perfect flat measurement. This result leads to the conclusion that the HCl etch removes oxide slightly more completely than the HF etch. However, both substrates were in atmospheric air during mounting on the molybdenum block after etching for a certain time. This time is around 20 seconds which can lead to a tiny surface re-contamination with oxygen. Here, a new process which is transferred into nitrogen atmosphere may lead to a cleaner CdTe surface and therefore it will avoid some crystal defects which occur due to these oxygen residuals. The HF etching process is not continued because no significant differences are detectable in

this testing period. Long-time tests may have to be done if volcano defects appear again.

5.5 Summary

This chapter has focused on the MBE growth of undoped HgTe quantum wells on CdTe substrates grown for the first time here at the EPIII and therefore new results were achieved. First, the carrier density could be decreased so far that the Fermi energy is located in the band gap. This can be controlled by a gate sweep and causes no clear Hall plateaus in the R_{xy}. Carrier densities of below 1×10^{11} cm^{-2} can be reached. Furthermore, it is shown that a very precise control of the layer thickness is possible by MBE which is proved by HRXRD and TEM measurements. Additionally, the dependence of the quantum well thickness to its mobility is analyzed and it can be shown clearly that with increasing QW thickness the mobility rises up averagely. However due to the strained growth on CdTe substrates, the band gap closes indirectly with increasing layer thickness at 11.6 nm. The maximum band gap is -11.5 meV at quantum well thickness of 7.2 nm. In addition, surface 2DEGs are analyzed to contact the topological edge states of HgTe quantum wells. For this purpose, the HgCdTe cap layer has to be below 10 nm. However, cap layer thicknesses below 5 nm show carrier mobilities which are to low to work with. Therefore, a compromise has to be made and only HgCdTe cap layer thicknesses between 5 and 10 nm are usable. This can maybe changed by doing the lithography in clean nitrogen atmosphere to avoid oxidization and contamination of the surface. A further huge innovation is the growth of HgTe quantum wells on CdTe/GaAs:Si substrates. Here, a increase in sample size by at least four times is possible. This leads to a larger amount of small samples with the same characteristic properties. In-situ grown HgTe QWs exhibit here comparable carrier densities around 1×10^{11} cm^{-2}. Furthermore, carrier mobilities of over 200 000 cm^2/Vs can be reached by growing on those optimized CdTe/GaAs:Si substrates. Due to the n-doping of the GaAs substrate and the thick insulating CdTe buffer, this combination can be used as a back gate and offers new options for investigating the surface at different carrier densities where the top gate prohibits the access to the surface. However, the roughness of the CdTe buffer layer is still to high and the gate does not influence the quantum well absolutely equal. Here, a further development is necessary. At last, a small project is discussed which deals with implementation of a new etching chemical to remove the oxide layer of the CdTe substrate prior to the MBE growth. Therefore, the etching behavior of high concentrated HF is tested and optical, HRXRD and transport results is compared to equal HgTe quantum wells which are etched with HCl by default. So, no significant difference is detectable and the standard HCl etch process is maintained. However, there was no comparison of long-time stability relating to volcano defect appearance. A repeated appearance of substrate contamination due to the HCl etch may cause a change to the HF etch.

6 HgTe - Bulk Structures

This chapter discusses the main part of this thesis: the research of HgTe as a 3 dimensional topological insulator from the MBE point of view. The theory of HgTe as a 3D TI is explained in chapter (2.5). This part contains the analysis of the crystalline properties of HgTe layers grown directly on CdTe substrates and the resulting effects on the transport properties. Furthermore, the growth and characterization of HgTe bulk layers embedded between HgCdTe layers is discussed.

6.1 HgTe directly on CdTe substrate

In 2007, L. Fu and C.L. Kane [3] published a theory paper which explains the transition from a 2 dimensional into a 3 dimensional topological insulator on the basis of the $\mathbb{Z}_2$ invariants. Furthermore, X. Dai *et al.* [41] discussed precisely the difference of helical edge states and surface states in HgTe quantum wells (2D) and bulk insulators (3D) in 2008. First experiments of Brüne *et al.* [37] confirmed these theories and showed very good results. So, ARPES measurements showed on a fully relaxed HgTe layer the dispersion of the surface state and bulk bands. In addition, this fully relaxed HgTe layer indicates its semi-metal character in transport measurements by zero visible plateaus in the Hall resistance. On the other side, a fully strained HgTe layer showed plateaus at quantized values at low temperatures (50 mK) which is a sign of 2D transport mechanism. This thesis contributes to these works and tries to improve and give a better understanding of crystalline properties, relaxation behavior and effects on the transport experiments.

The most important condition for working with HgTe as a 3D TI is that HgTe has to be grown laterally strained. This leads to a splitting of the Γ_8-subbands and therefore opens a band gap of calculated $E_g \approx 22$ meV by using an eight band $\mathbf{k}\cdot\mathbf{p}$ model if HgTe is grown fully strained on CdTe [37, 40]. The strain has to be laterally tensile because compressive strain would move the valence and conduction band maximum away from the Γ-point in the band structure [127]. Therefore, the only substrate which is readily available is CdTe. HgTe and CdTe are II-VI-semiconductors and crystallize both in zinc blende structure. The lattice constant of CdTe is slightly larger (a_{HgTe} = 6.4619 Å; a_{CdTe} = 6.4825 Å) [17, 18] and forces a maximum strain of around 0.32. This is another reason growing on CdTe substrates. So, CdZnTe substrates with around 4 % zinc content, which were normally used for lattice matched growth of HgTe quantum wells before this thesis, are not suitable anymore because of the required strain introduction in HgTe layers to open up a band gap.

The growth of HgTe bulk layers is performed almost equally to the quantum wells (see chapter 5). The substrates are etched by HCl solution and mounted with liquid Ga on a molyb-

denum block. After a rapid transfer into the UHV system, a CdTe buffer layer of around 100 nm is grown previously to flatten the surface. Then the HgTe bulk layer is grown at 180°C. During the cool-down process, the Hg cell is still open to anneal the HgTe layer and to prevent mercury sublimation from the layer. After that, the HgTe bulk sample is transferred out of the UHV and analyzed by Nomarski microscopy, HRXRD, AFM and standard transport characterization Hall measurements. As shown by Brüne *et al.* [37] a 70 nm HgTe bulk layer directly grown on CdTe is fully strained and exhibits a carrier density of around 4×10^{11} cm^{-2} for each surface and a carrier mobility μ = 34 000 cm^2/Vs. A 1 µm thick HgTe layer shows the Dirac-like surface bands but is already fully relaxed.

So, on the one hand the relaxation behavior of HgTe bulk layer grown directly on CdTe is analyzed to guarantee consistent transport experiments conditions because the band gap closes with relaxation and HgTe as a semi-metal is not usable as a TI. So, HgTe bulk should stay fully strained to provide the maximum band gap. Furthermore, the quality of the layers is analyzed. The strain and relaxation of the HgTe layers is determined by HRXRD. Here, ω-2Θ-scans and reciprocal space maps show very precise results for a good control of critical thickness point where the layer starts to relax. The crystalline quality of the layers is identified by an ω-scan. On the other hand, the dependence of the carrier mobility μ on the layer thickness is explored to find the best correlation of HgTe layer thickness and highest carrier mobility to provide best transport preconditions. Here, Hall measurements are done in a magnetic field up to 16 T at a temperature of 4 K. By finding a layer thickness which leads to a high carrier mobility, it would establish an optimal HgTe layer thickness for further experiments.

In Fig. 6.1 standard HRXRD measurements are displayed characterize the HgTe layer. In a) the ω-2Θ-scan shows the CdTe and HgTe (004) reflections and the thickness fringes of HgTe. With the help of the thickness fringes, the layer thickness is determined by a fit (red). The ω-scan in b) indicates the crystalline quality. A FWHM value of under 20 arcsec is achieved for nearly all HgTe bulk samples with a thickness less than 140 nm. Compared to the 150 arcsec of CdTe grown on GaAs:Si, this value is extremely low and points to a high crystalline quality of the HgTe layer. The nature of the lobes which are visible in the ω-scan is explained in [57, 126]. Here, strain fields of adjacent dislocations do not overlay in a layer with a low density of dislocations. A dislocation occurs at the interface between substrate and layer and so the strain field can propagate to the top edge of the layer without hindrance. The limitation by the layer thickness entrains a lateral limit of the strain field. The strain field around a dislocation is approximated as a defective building block in a perfect crystal. Since similar dislocations lead to commensurate building blocks, the lobes originate in the ω-scan perpendicular to the building blocks. Therefore, these lobes are an indication for strain induced defects. As the HgTe bulk layer is not grown lattice-matched to the CdTe substrate, these lobes are measurable. This effect occurs rather for thicker layers than for thin layers because thicker layer generate more intensity. But these lobes can also appear if the growth parameters are not adjusted correctly or other factors affect the growth and therefore produce dislocations during the growth. Since the temperature control is not very precise over the full growth period of a thick bulk layer because it is located on the backside of the molybdenum block and therefore a thick HgTe layer exhibits higher heat emission and the growth surface cools down with layer growth. This leads to dislocation nuclei during the growth and produces those defective building blocks but in a smaller size. Here, a surface sensitive temperature

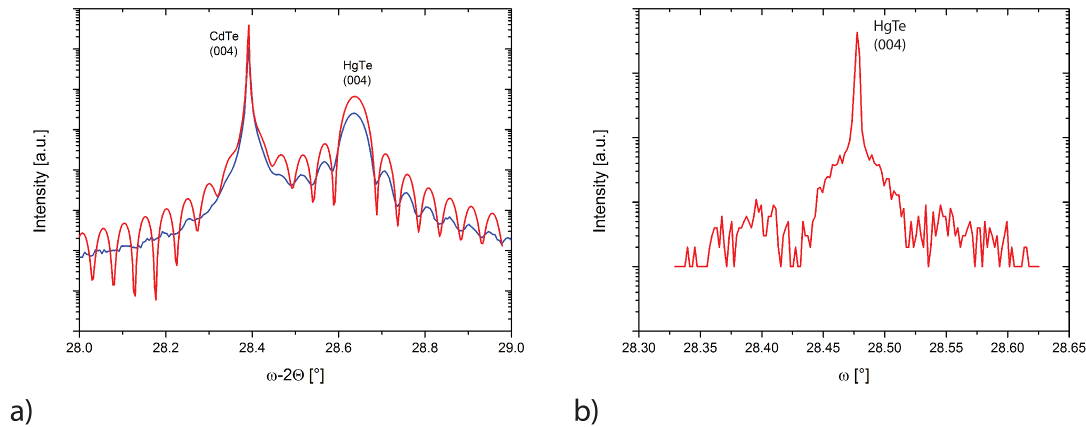


Figure 6.1: a) ω-2Θ- and b) ω-scan of Q2491, a 105 nm thick HgTe bulk layer grown directly on CdTe.

control system may find a remedy [122].

In the following, the characteristic transport properties like carrier density and mobility of the HgTe bulk samples will be discussed. Here, the same requirements are qualified as for the HgTe quantum wells in chapter (5). So according to theory, the HgTe bulk samples are expected to show low carrier density to shift the Fermi energy into the band gap and therefore, only the surface states are measurable and the bulk states do not contribute to the measurement. In addition, the carrier mobility should reach a very high value due to the high crystalline and interface quality of the layer. The carrier densities and mobilities of all HgTe bulk layers are shown in Fig. 6.2 (a) and (b) for the gate voltages U_g = 0 V and 1 V. These samples are grown directly on commercial CdTe substrates and feature a top gate. Both graphs show no clear increase of the carrier density and mobility respectively to the rising layer thickness. In the carrier density graph, the four data points at around 40×10^{11} cm^{-2} and the two data points at nearly 30×10^{11} cm^{-2} stand out conspicuously of the rest of the data points. These six data points correspond to three different samples measured at zero and one volt gate voltage. So, the sample at n = 30×10^{11} cm^{-2} is the second grown sample of the day. Due to many orders of bulk samples, two bulk samples had to be grown consecutively on the same day. After transferring the first sample out of the CMT - chamber, the titanium sublimation pump was activated several times. So the background pressure of the CMT - chamber dropped into the lower 10^{-9} Torr range. After pumping the CMT - chamber, the standard back ground pressure is usually located at almost 1×10^{-10} Torr. This difference in back ground pressure seems to affect the carrier density slightly. For HgTe quantum wells, no change of the carrier density is detectable in consecutive grown samples on the same day. This leads to the assumption that the bulk layer is maybe more affected due to growth time. While a standard HgTe QW is grown in around 70 seconds, the duration of this HgTe bulk layer growth is almost 2000 seconds. During this time, the MBE growth of the layer is of course longer influenced by the surrounding conditions. The defects associated with the higher back ground

pressure increase the carrier density. So, only one HgTe bulk sample should be grown per day to avoid unintentional low carrier mobility. Furthermore, the mobility of these samples, which were grown as second sample on a day, is very low (10 000 cm^2/Vs) due to these defects. The two samples with carrier densities of around 40×10^{11} cm^{-2} exhibit common HgTe bulk

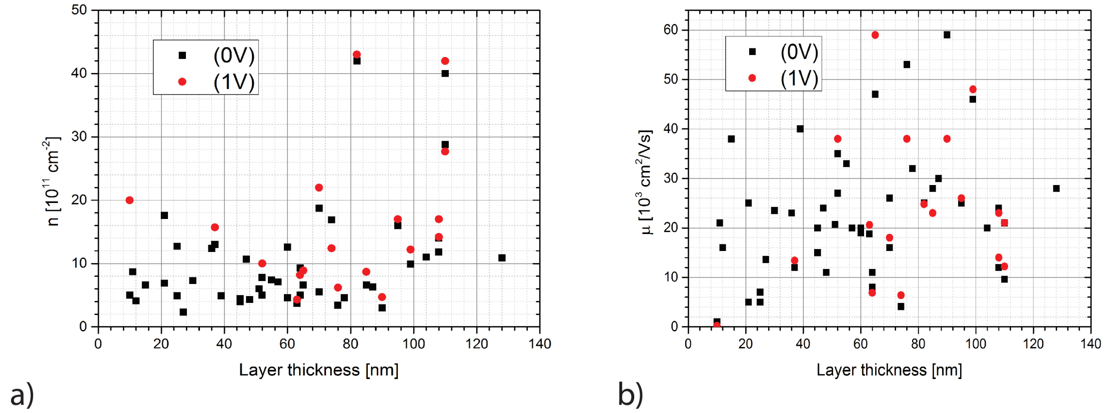


Figure 6.2: a) The carrier density and b) the carrier mobility of all HgTe bulk samples grown directly on commercial CdTe are plotted against the layer thickness for gate voltages $V_g = 0$ V (black) and 1 V (red). The best-fit lines of zero and one gate voltage rise up slightly for increasing layer thickness.

carrier mobilities of $\mu \approx 25\,000$ cm^2/Vs. But for these two samples, a new oxide etching method was executed. Here, the un-etched CdTe substrate was mounted with liquid Ga on a molybdenum block by default and transferred into a special load lock. This load lock was equipped with a hydrogen can. Together with a radio frequency (RF) generator the hydrogen plasma reacted with the TeO_2 to water (H_2O) and a H-passivated layer [128, 129, 130]. This etching technique removed the CdTe oxide completely. A more detailed discussion of this method is done by P. Leubner [131]. However, the two HgTe bulk samples which were etched by the H-plasma show remarkable high carrier densities. The mechanism behind that was unfortunately not analyzed closer because of missing analyzing techniques. So, this etching method is not continued and will not be described in detail.

Due to the lattice-mismatch of CdTe and HgTe it is not possible to rise the carrier mobility by increasing the layer thickness into infinity. It does not play a role if the layer is compressively or tensile strained. At a certain critical thickness the strained layer starts to relax and will ultimately take its natural lattice constant. As the band gap of the topological insulator HgTe bulk is related to the strain, the critical thickness is very important to know how to prevent relaxation. This ensures the maximum band gap for the layer and the transport measurement. To determine the relaxation process the HgTe bulk layers are analyzed by a reciprocal space map (RSM) of the asymmetric (115) reflection via HRXRD. In Fig. 6.3 (a) a RSM of a 300 nm thick HgTe layer grown directly on a CdTe substrate is shown. For a fully strained layer the reflection appears at the same reciprocal space coordinate Q_x for both materials while for

a fully relaxed HgTe layer the (115) reflection will appear on a line rotated by an angle of 15.79°. This angle is directed to the origin (000) of the reciprocal space. Relaxation angle and residual strain (RS) are directly proportional, so the relaxation process can easily be monitored [132]. The residual strain is quantified by the strain level:

$$RS = \frac{15.79^\circ - \alpha}{15.79^\circ}. \tag{1}$$

Using the model of Matthews and Blakeslee, the critical layer thickness d_c of HgTe on CdTe is calculated to 155 nm. This value has to be verified because the model uses several assumptions [57, 133, 134]. Therefore, series of different HgTe layer thicknesses were grown with thicknesses from 50 nm up to 1 µm directly on the CdTe substrate. The residual strain, determined by reciprocal space mapping, is shown versus the inverse layer thickness in Fig. 6.3 (b).Furthermore, HgTe bulk layers with thicknesses $d > d_c$ are included in an uncapped (blue) and capped (green) with 10 nm HgCdTe condition. The residual strain is calculated relating to the CdTe substrate reflection. Because of the thickness of the CdTe substrates, it is a matter of fact that the substrates own their natural lattice constants. But due to alignment differences in the HRXRD measurement process (bonding with glue, mounting on the rotator), the absolute values of the measured data are not always the same and therefore the CdTe reflection is very nice reference point. Here, the HgTe film is completely strained for layer thicknesses up to 155 nm. This is in a good agreement to the theoretical prediction by Matthews *et al.* For thicker layers the HgTe releases strain approximately linearly with inverse layer thickness down to 10^{-3} nm^{-1}, i.e. up to a layer thickness of 1 µm. As a reason for this could be the very flat interface conditions of the HCl etched substrate because his leads to a very flat and high crystalline quality start of the Hg based growth on the thin CdTe buffer which is determined by RHEED analysis.

As mentioned above, in the same graph the data for a HgTe layer uncapped (blue) and capped (green) with 10 nm of HgCdTe is shown. The capping layer is introduced to protect the surface against oxidization and contamination. XPS measurements show that under atmospheric air HgTe and HgCdTe gets oxidized and generates a thin oxide film. The thickness of this natural oxide layer is calculated to around 1.3 nm [108, 131]. In combination with a top gate, this oxide layer and surface contamination during the mesa structuring process will affect the electrical transport properties and influence the surface states, too. So usually, a 10 nm protection cap of HgCdTe leads to an immense boost of the carrier mobility [around 200 000 cm^2/Vs (see graph 6.9)]. However, in this case, the carrier mobility is only around 60 000 cm^2/Vs with the cap compared to around 25 000 cm^2/Vs without a cap. This result based on the partial relaxation which already occurs at layer thicknesses larger than 155 nm. This is explainable by this way that relaxation generates defects in the crystal and these defects reduce the crystalline quality of the grown layer and a lower crystalline quality provides usually lower carrier mobilities. Furthermore, it is worth mentioning that the critical layer thickness remains unchanged if the HgTe layer is capped with an additional HgCdTe layer. This 10 nm HgCdTe cap layer reduces already the relaxation rate ($r = dRS/\, d(LT)^{-1}$) [Fig. 6.3 (b)]. This observation indicates that the larger lattice constant of the $Hg_{0.32}Cd_{0.68}Te$ layer (a = 6.476 Å, see eq. 3) may compensate strain considerably in the interface region between the HgTe layer and the upper HgCdTe layer and probably extends to the whole layer.

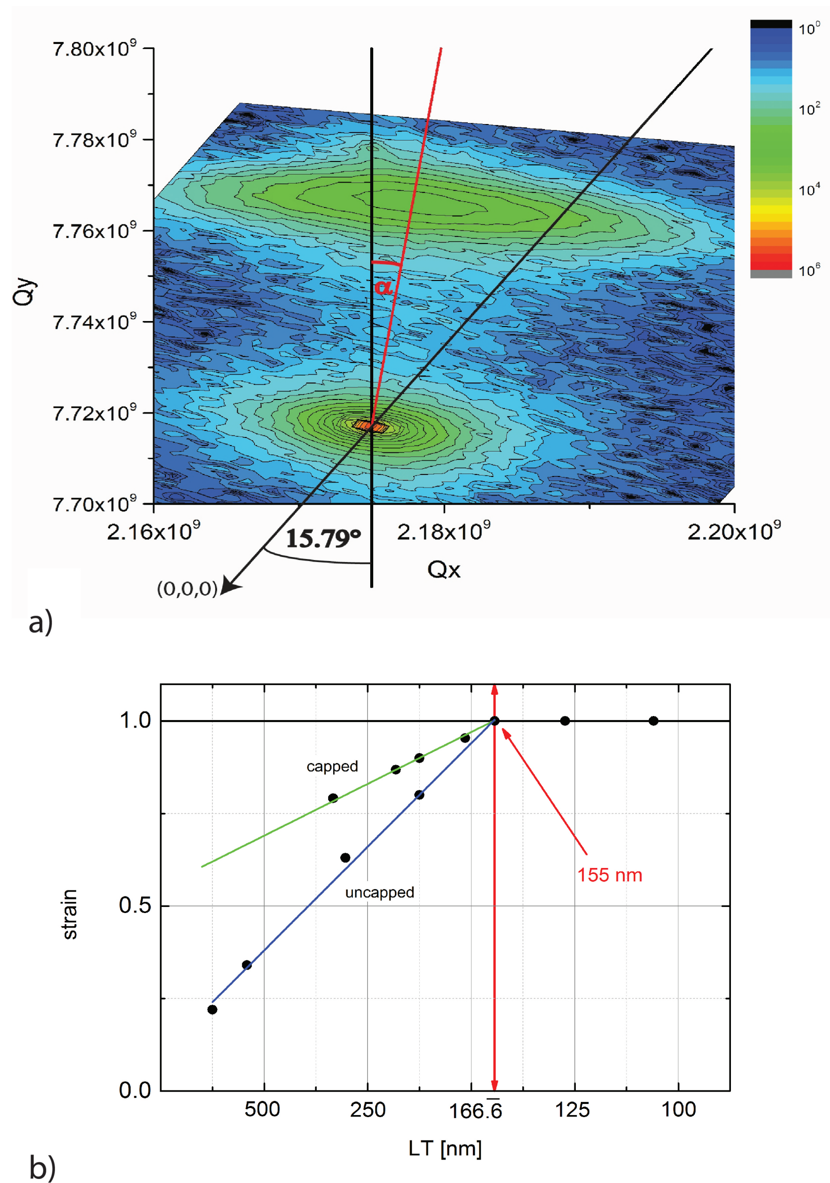


Figure 6.3: a) Exemplary reciprocal space map of the (115) reflection of CdTe substrate and HgTe layer (300 nm). Here, a small shift of the HgTe peak can be seen which is indicated by the red line. The two black lines represent the extreme cases of fully strained (vertical line) and fully relaxed (tilted line) layers. The angle between both lines gives the relaxation level. Q_x and Q_y are reciprocal space coordinates. b) The residual strain of uncapped and 10 nm - capped HgTe layers on CdTe substrates is shown. The layers are fully strained for a thickness thinner than 155 nm. The capped samples (green) relax slower than the uncapped samples (blue) but relaxation sets in at the same thickness. The layer thickness (LT) is plotted reciprocally but labeled regular due to faster understanding.

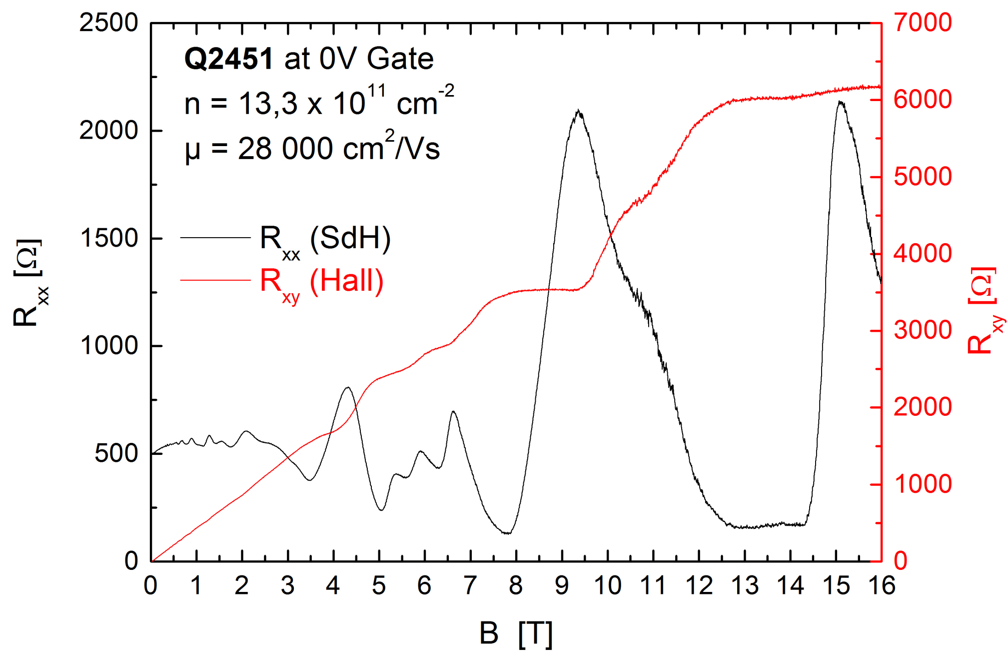


Figure 6.4: Transport measurements (Hall(red) and SdH(black)) of a 128 nm thick HgTe layer (Q2451) at gate voltage $U_g = 0$ V.

In Fig. 6.4 Hall measurements of a 128 nm thick HgTe layer (Q2451) is shown at gate voltage U_g = 0 V. The Hall plateaus and SdH oscillations are clearly visible. The carrier density n and mobility μ are determined to n = 13.3×10^{11} cm^{-2} and μ = 28 000 cm^2/Vs. These values are typical for HgTe bulk layers of the corresponding layer thickness as shown in Fig. 6.2 (a). However, the influence of the surface states at the sides of the bulk layer and how they contribute to the conductivity is not fully understood [135, 138]. Another point is that the theory of the quantum Spin Hall effect in 3D TIs is not completely decoded and therefore some effects may still contribute to the measurements. However, in addition the lithography after the growth influences the HgTe bulk layers as well due to surface treatments.

So, the growth and handling of HgTe bulk layers without a cap offers still room for improvements and further developments.

6.2 HgTe Bulk embedded in CMT Layers

To improve the electronic properties of HgTe bulk crystals, a new layer stack is evolved. So, the HgTe bulk layers are embedded in HgCdTe layers. This leads to a huge improvement of the electronic characterization results of the transport measurements. Here, the heterostructure is constructed similar to the quantum well structure with the exception that the HgTe is thicker. Furthermore, the whole HgTe bulk heterostrcuture has to be fully strained, while for HgTe quantum wells the HgTe lattice-matched growth is usually preferred (see chapter 5.1). However, new experiments of strained HgTe quantum wells are carried out [131]. Thus, the following investigation focuses on how a barrier of HgCdTe influences the relaxation process of HgTe and how the growth, quality and relaxation of the barriers is affected by the substrate material, becomes important. Here, the critical thickness of the HgCdTe on the CdTe substrate has to be determined to ensure that the subsequent topological insulator layer HgTe receives the full lattice mismatch and therefore has the theoretical predicted properties. HgCdTe layers are grown directly on commercial undoped CdTe or optimized CdTe/GaAs:Si substrates to investigate the influence of the different substrates. Due to the insulating property of CdTe, n-doped GaAs can also be used for backgating. This would allow more control of the bottom and top surface states in combination with a top gate. The grown HgCdTe samples are analyzed after growth via Nomarski microscopy, HRXRD, SEM and AFM. As the Nomarski and AFM inspections serve only as a first, fast control of the MBE growth, the main focus is on the relaxation progress of the HgCdTe layers. Here, Fig. 6.5 shows the residual strain plotted over the inverted thickness of HgCdTe layer grown on epi-ready CdTe (a) and on pregrown CdTe/GaAs:Si (b). The residual strain is determined by reciprocal space mapping of the (115) reflection as described in chapter (6.1). The growth series investigates barrier thicknesses ranging from 100 nm up to 3 000 nm. Based on the theoretical calculations of Matthews *et al.* [133], the critical thickness d_c of $Hg0.3Cd_{0.7}Te$ is expected to be 725 nm. The experimental results show that the HgCdTe layer grown on commercial CdTe substrates remains fully strained up to 850 nm (Fig. 6.5 (a)). The HgCdTe layers grown on the CdTe pre-buffered GaAs substrate are fully strained up to a thickness of about 250 nm. In the region between 250 nm and 700 nm a partial relaxation of less than 10 % is observed in some of the samples. For thicknesses larger than 725 nm (the theoretically expected d_c) the strain decreases linearly

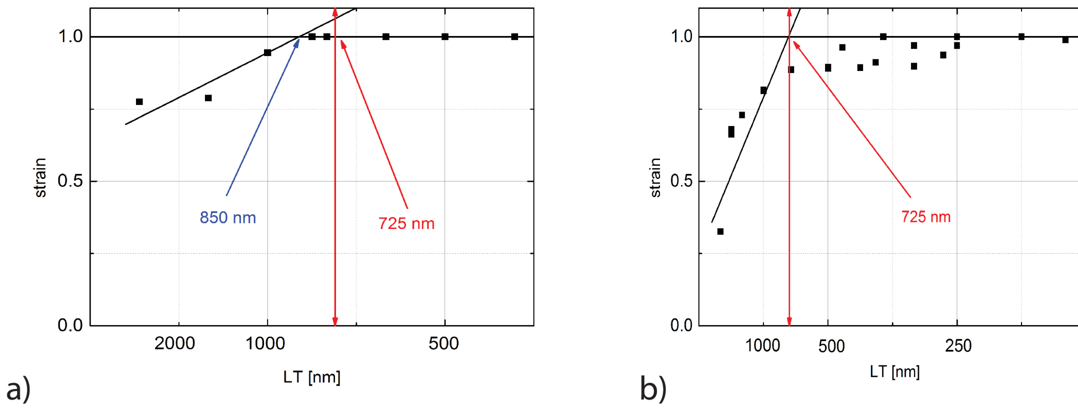


Figure 6.5: Residual strain is presented over the inverted thickness of HgCdTe layers grown on commercial CdTe (a) and on pregrown CdTe/GaAs:Si (b). The layer thickness (LT) is here plotted reciprocally but labeled regular due to faster understanding.

with the inverse layer thickness.

Moreover, the reciprocal space map in Fig. 6.6 (a) shows that the GaAs substrate, as well as the CdTe layer, are fully relaxed. Thus, the Hg-based layer possesses the natural lattice constant of CdTe. The inset shows the reflection of the lateral, fully strained HgCdTe layer exhibiting the same lateral lattice constant as CdTe. To further access of the crystalline quality, Fig. 6.6 (b) shows HRXRD-ω-scans of the commercial CdTe substrate (black) and the pregrown CdTe buffer (red). The FWHM amounts to around 15 arcsec for the commercial CdTe and around 150 arcsec for the optimized CdTe buffers. The large lattice mismatch between GaAs and CdTe leads to dislocations and crystal defects in the buffer layer (see chapter (4)). This difference in the CdTe substrate can also be seen by AFM measurements. The surface roughnesses of the HgCdTe layers are shown in Fig. 6.6 (c) and (d). In (c) the HgCdTe layer was grown on a CdTe/GaAs:Si substrate and in (d) the growth happened on a commercial CdTe substrate. The layer thickness occurs for both samples in the same range (365 nm for (c); 500 nm for (d)). For the AFM picture of the HgCdTe layer grown on CdTe/GaAs:Si it is notable that there are a lot of small hillocks with a size of 1 µm width and underneath a surface structure is still observable where widespread hillocks preform the surface structure. These hillocks have the width of about 4 µm and height of about 5 nm. The root mean square (RMS) roughness measured by AFM is determined for this sample to 3.11 nm. In contrast, the HgCdTe grown on a commercial CdTe substrate shows a RMS roughness of 0.837 nm. On this sample some small hillocks are still visible but no distinct structure underneath is observable. This points to an origin of these hillock structures in the HgCdTe layer.

Additionally, SEM pictures of a 1.5 µm thick HgCdTe layer are shown in Fig. 6.7 (a) and (b). The left SEM picture shows a lateral cut through two growth defects. These hillocks are detectable not before layer thicknesses larger than 1 µm by light optical microscope. HgCdTe layers on commercial CdTe substrates as well as on pregrown CdTe buffer layer show these

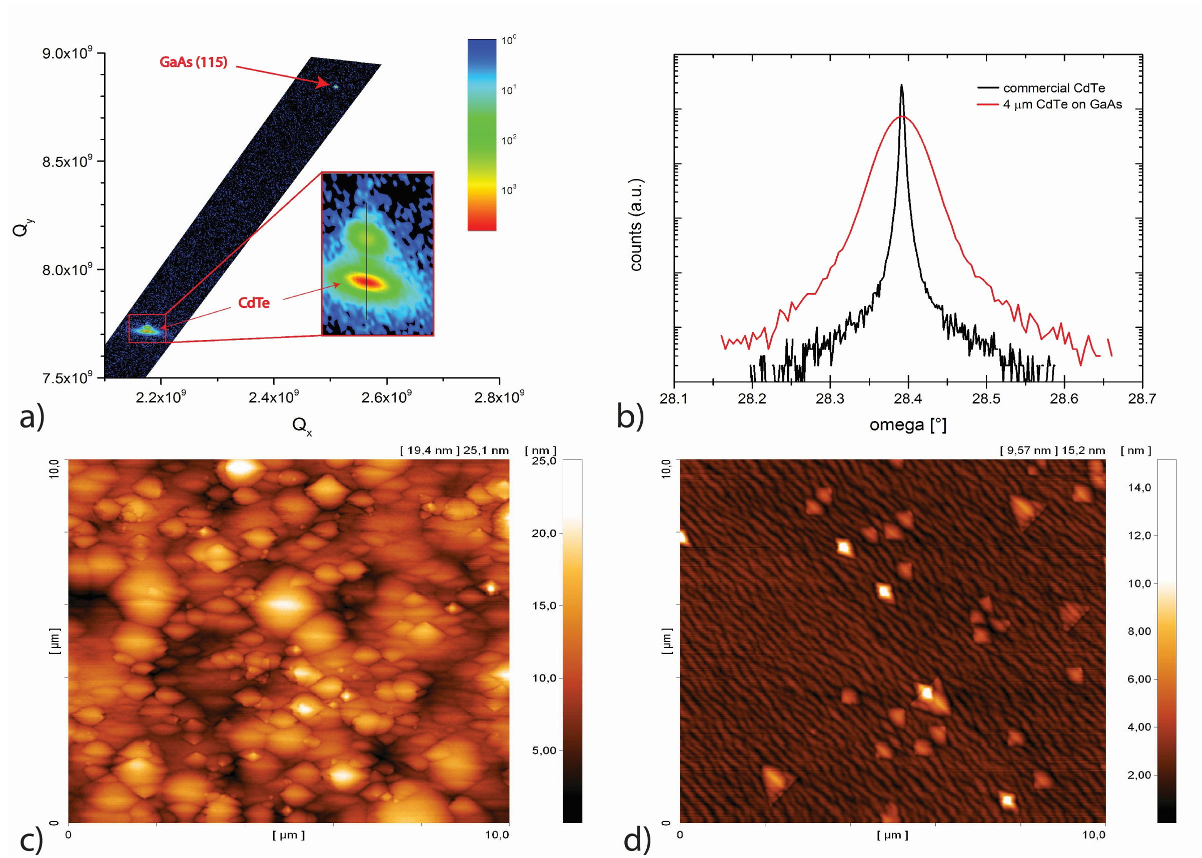


Figure 6.6: a) Reciprocal space map (RSM) of the HgCdTe (115) reflection on an n-doped GaAs substrate with an approximately 4 µm thick CdTe buffer. The inset shows a fully strained sample. b) HRXRD-ω-scans of commercial CdTe substrate and grown CdTe buffer on GaAs. c) AFM picture of HgCdTe on pregrown CdTe buffer and commercial CdTe substrate d).

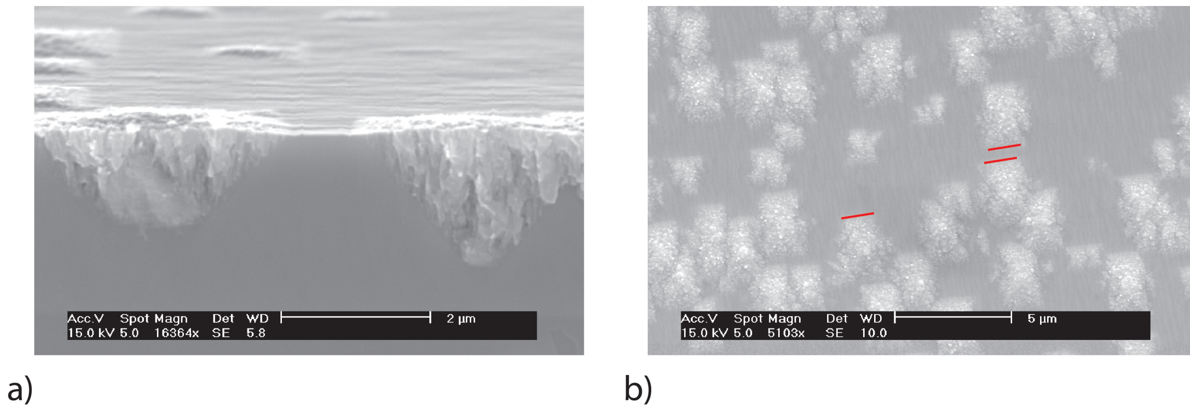


Figure 6.7: a) SEM pattern of a hillock in cross-section and top view b). The red lines in the top view indicate the sharp edges which were produced by the two (111)Cd planes.

hillocks. The right picture is from the top surface. The hillocks a clearly visible. Furthermore, they may show a slight tendency to generate two rough and two sharp sides as described in [141]. The sharp sides are indicated by red lines in Fig. 6.7 (b).

For HgCdTe grown on commercial CdTe substrates the results are qualitatively similar. Here the layer remains fully strained up to a certain critical thickness and then relaxation is in accordance with expectations [132]. The difference of the measured and predicted critical thickness is that many assumptions are included in this model. Moreover, there are still some confusion and controversy because of uncertainties and differences in the exact magnitudes of some factors incorporated into the Matthews and Blakeslee model (described by Hull and Bean [139]). Furthermore, it is not known if the Hg may diffuse into the CdTe buffer below. So there is maybe a bigger exchange of atoms between HgCdTe and CdTe as between HgTe and CdTe because HgCdTe and CdTe are more similar. This could lead to a larger interface region combined with an smooth transition from CdTe to HgCdTe. This could explain the critical thickness of 850 nm instead of the expected 725 nm.

The relaxation of HgCdTe grown on CdTe/GaAs:Si shows the three previously mentioned regions. However, the region between 250 nm and 725 nm shows a very extraordinary relaxation behavior. The relaxation fluctuates between 0% and 10 %. Since this behavior is only observed on CdTe/GaAs substrates, a reason for this partial relaxation may originate from the crystalline and surface properties of the CdTe buffer grown on GaAs substrates. So, the CdTe buffer surface exhibits a lot of crystalline defects in (001) growth direction due to the large lattice-mismatch (cf. chapter 4). A rougher surface produces more dislocation and growth defects than a smooth, flat surface. This is evident from the ω-scan of commercial CdTe and pregrown CdTe on GaAs and their representative AFM pictures (Fig. 6.6). The pregrown CdTe buffer layers exhibit in HRXRD-ω-scans FWHM-values of around 150 arcsec and these are an order of magnitude larger than the FWHM-values of commercial CdTe substrates. Furthermore, the AFM pictures look different because the CdTe/GaAs:Si substrate provides a RMS roughness of around 2.5 nm. This roughness is produced by structures

with large in-plane expansions (radius $\approx 5\mu m$). Due to the low growth temperature, atoms on the HgCdTe surface do not have sufficient kinetic energy to diffuse over long distances. The simple overgrowing process results in an increasing roughness with rising layer thickness. Furthermore, there are small hillocks visible on these long-range hillocks (see Fig. 6.6). These smaller structures correspond to the HgCdTe growth. They may originate due to crystalline defects on these long-range structures and due to different growth preferences which are existent for $Hg_{1-x}Cd_xTe$ growth on different CdTe facets. The MBE growth of HgCdTe and HgTe is developed in (001) direction. For other growth directions, growth conditions like substrate temperature and material fluxes have to be adjusted. MBE growth of HgTe around CdTe nano-wires shows this effect very nicely [140]. In contrast to the rough HgCdTe growth on CdTe/GaAs:Si an AFM picture of a comparable HgCdTe layer grown on commercial CdTe substrate is presented aside [Fig. 6.6 (d)]. There is just a very smooth substrate structure measurable and only a few HgCdTe hillocks arise. This means that there are much less interface defects on the CdTe surface which results in fewer dislocations.

In contrast, the huge hillocks which are presented in Fig. 6.7 have a different origin. So, in 1988 Koestner *et al.* [141] described that these hillocks arise from twin lammellae which already exist in the CdTe buffer or substrate underneath the HgCdTe. From there, two (111)Cd and two (111) Te planes, which equally incline by 55° from the growth surface, subsist in the (001) oriented growth direction. Here, only the (111)Cd planes serve as twinning planes. This twin operation results in a $(22\bar{1})$Te surface orientation of the lamellae. From there the hillock growth starts because the Hg flux, which is used to grow (001) HgCdTe, is in excess of needed to grow a single crystalline HgCdTe $(22\bar{1})$Te layer. The defect formation inside the lamella produces another twin to appear along the opposing (111)Cd plane. These two (111)Cd planes create the sharp edges found on the hillocks (red lines in Fig. 6.7 (b)). As the other set of opposing edges of the hillocks are blurred, one can draw the conclusion that twinning is clearly less favorable along the inclined (111)Te planes. These hillocks can also be found on HgCdTe samples grown on CdTe/GaAs:Si substrates as well as on commercial substrates and therefore, an improvement of the CdTe buffer is needed. That hillocks are only visible at layer thicknesses larger than 1000 nm, it does not mean that the twinning planes do not exist in thinner layers. This could not be proved by HRXRD measurements and only TEM measurements may bring clarity of the crystalline structure inside the crystal. So this twinning can lead to impurities or trap states which could therefore influence the transport characteristics of the HgTe/HgCdTe layer structure.
Another interesting fact is that the depth of the hillocks´ nuclei is in the range of the critical thickness d_c. The hillock in Fig. 6.7 (a), which is almost cut in the middle, is only approximately 100 nm smaller at its deepest point than the theoretical prediction of the critical thickness. Therefore, it becomes obvious that layer thicknesses larger than d_c trigger the formation of these dislocations out of the lamella.

However, the most important result for analyzing the HgTe layer quality is given by standard Hall measurements. Here, carrier density and mobility show the final electronic characteristics after growth and lithography at 4K. In Fig. 6.8 a Hall measurement is presented at a top gate voltage U_g = 1 V. The sample (Q2696) is composed of a 73 nm thick active HgTe layer and a 75 nm HgCdTe bottom and cap barrier, which is grown on a commercial CdTe substrate. The mesa and top gate is processed in the same way as the quantum well structures. So, the

longitudinal resistance R_{xx} shows clear SdH oscillations and the Hall resistance reaches some Hall plateaus. For U_g = 1V, the carrier density n is calculated to n = 3.1×10^{11} cm^{-2} and the mobility to μ = 831 000 cm^2/Vs. However, mobility increases immensely by over an order of magnitude, while without HgCdTe barriers the mobility of HgTe bulk layers does hardly exceed 40 000 cm^2/Vs. This allows to see effects of the measured layer much clearer. So in high mobility HgTe bulk samples, an oscillating feature with top gate independent frequency can be found for R_{xx} and R_{xy} for low magnetic fields (B < 1T). This can be explained by a third carrier species with low carrier density and high mobility. So far the origin of this feature is unkown, but a more detailed analysis can be found in C. Thienel [138, 142].

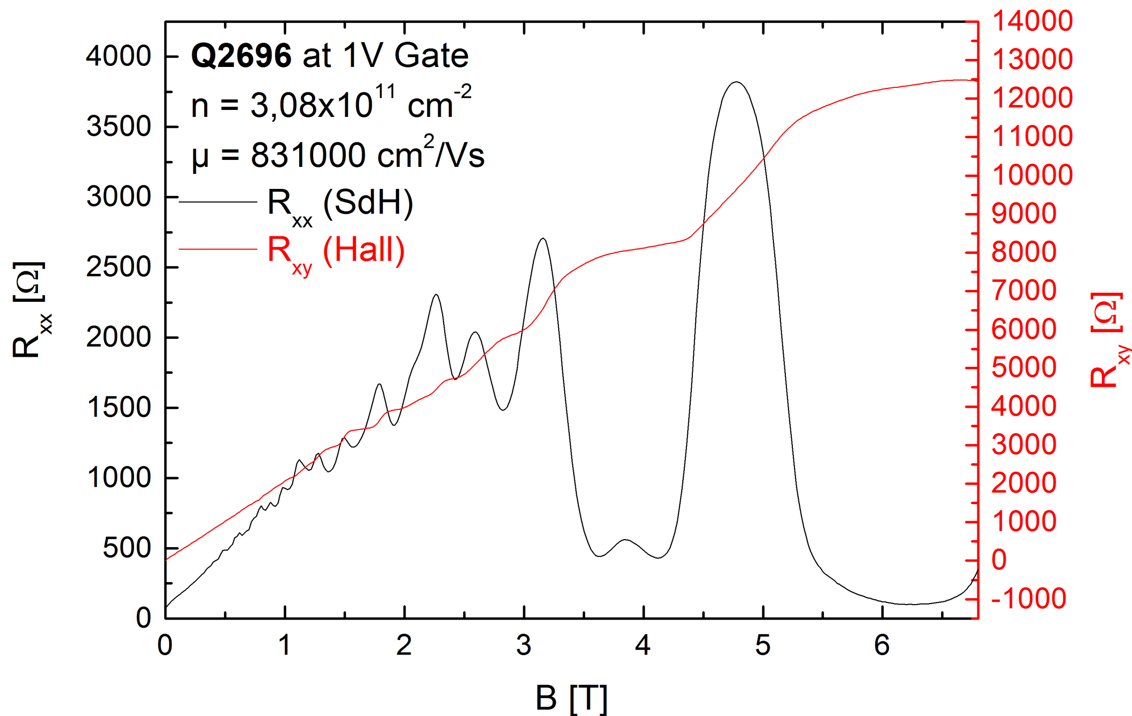


Figure 6.8: Transport measurements (Hall(red) and SdH(black)) of a 73 nm HgTe bulk layer with a 75 nm CMT barrier and a 75 nm CMT cap at top gate voltage U_g = 1 V.

For HgTe bulk layers embedded in HgCdTe barriers grown on CdTe/GaAs:Si, there does not exist many data up to now but first samples show nice Hall measurements. The averaged carrier mobility μ is determined to around 200 000 cm^2/Vs. This value is a little bit smaller than the averaged carrier mobility of the same layers grown on commercial CdTe substrates. The carrier density is however comparable and in the low 1×10^{11} cm^{-2} region. Furthermore, it is notable how the HgCdTe cap layer thickness influences the carrier density and mobility of HgTe bulk layers. In Fig. 6.9 the densities (a) and mobilities (b) are plotted against the cap

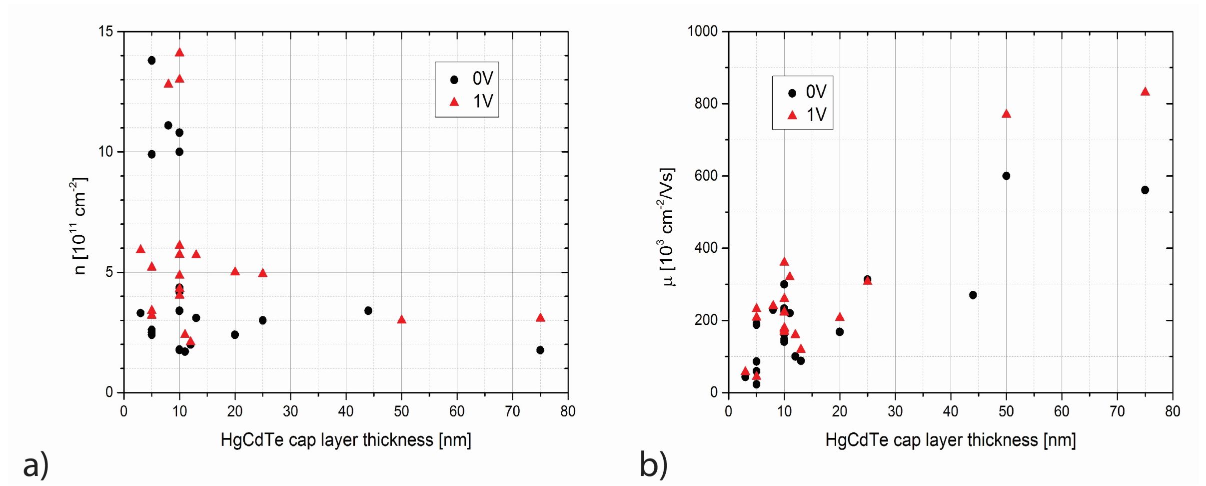


Figure 6.9: a) Carrier densities n and b) carrier mobilities μ plotted against the HgCdTe cap layer thickness for gate voltages U_g = 0 V and 1V.

layer thickness. Here, a slight trend is visible that with increasing cap layer thickness the carrier density of the HgTe bulk layer decreases in average and in contrast the mobility increases with rising cap layer thickness. The decreasing carrier density can be attributed to lesser influence of lithography chemicals. So the HgCdTe cap acts like a protective layer, which also includes a protection against oxidization. So the HgTe layer is more protected the thicker the cap layer is. This tendency is observable for HgTe quantum wells,too (cf. chapter (5.1)).For the mobility trend, a suggestion is that here the interface between the HgTe bulk layer and the HgCdTe layer is the cleaner the thicker the cap layer is. A thin cap layer (< 10 nm) may let diffuse some oxide atoms and may result in oxidization related defects near the surface of HgTe which reduce the carrier mobility of the HgTe bulk surface states. Furthermore, the HgTe layer is highly unstable against temperatures above 80°C. So, lithography can rise the temperature locally in the crystal and therefore, Hg diffusion starts. If the HgCdTe cap layer is thick enough, it serves as a diffusion barrier for oxide atoms. The HgTe layer remains nearly unaffected. However, the both HgCdTe layer plus the HgTe layer are not allowed to exceed the critical thickness of the whole layer stack because relaxation will generate crystalline defects in all layers and also decrease the maximum band gap value of the HgTe.

Transport measurements on the strained HgTe bulk show that the top gate influences the carrier densities of the top and bottom surface unequally [38, 138]. Here, the investigation of the samples with insulating (001) CdTe on n-doped (001) GaAs:Si opens further possibilities to investigate this behavior. Now, it is possible to tune the carrier densities of the bottom and top surface of the HgTe layer grown on CdTe/GaAs:Si separately by using the n-doped GaAs substrate in combination with the insulating thick CdTe buffer as a back gate. This provides a good possibility to analyze the HgTe bulk layer and its surface states more precisely. Fig. 6.10 (a) shows a standard Hall measurement of a capped 75 nm HgTe bulk sample grown in-situ on CdTe/GaAs:Si. At 3 V top gate voltage Hall plateaus are hit accurately together

with good SdH oscillations. The carrier density n is here 5×10^{11} cm^{-2} and the mobility is computed to 150 000 cm^2/Vs. If now the GaAs:Si substrate is connected to a voltage source, Hall measurements are done at 3 V top gate voltage with different back gate voltages, shown in Fig. 6.10 (b). Here, the back gate clearly influences the Hall plateaus and changes the carrier density. Furthermore, it is now possible to tune the Hall plateaus at a certain magnetic field. This can be seen on the Hall plateaus ν = 4, 5, 6 and 7 at R_{xy} = 1/4 h/e^2, 1/5 h/e^2, 1/6 h/e^2 and 1/7 h/e^2.

A detailed explanation is given in [138]. Furthermore, due to the thick CdTe buffer layer (4 µm), the applied voltage of the back gate is higher than the top gate which is separated by a 100 nm insulator. Moreover, the dielectric constants of the back and top gate insulators are different. To sum up, this leads to a change in density of 2.5×10^{11} cm^{-2} per volt for the top gate influence. The back gate changes the carrier density by 0.1×10^{11} cm^{-2} per volt. Since the back gate breaks through at around ± 20 V, it is possible to change the carrier density by $\Delta n \approx 3\times10^{11}$. This is absolutely sufficient for standard transport measurements.

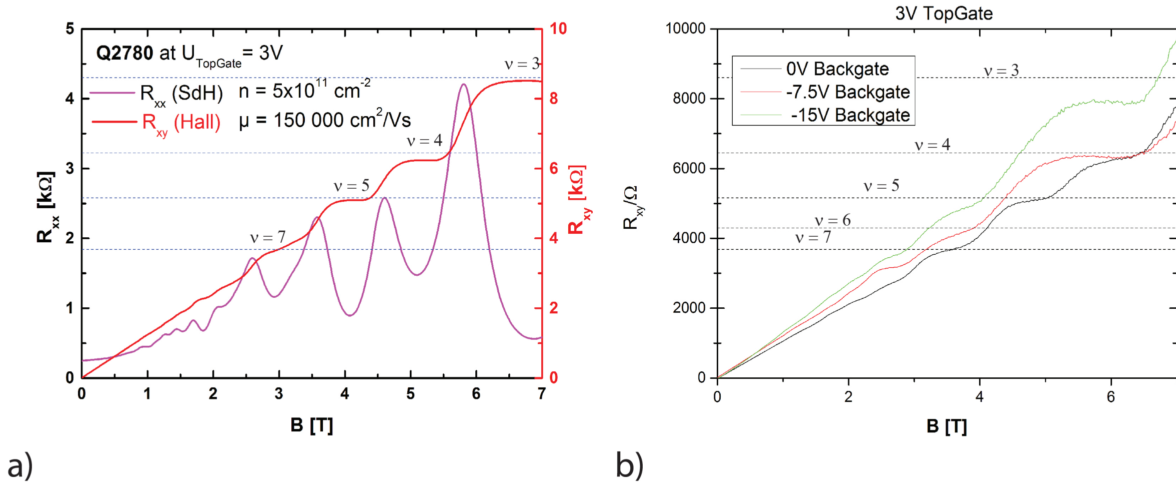


Figure 6.10: a) Transport measurements (Hall(red) and SdH(black)) of a HgTe bulk layer embedded in CMT layers at top gate voltage U_g = 3 V. b) Hall resistance R_{xy} measurements for three different back gate voltages U_{bg} at a constant top gate voltage.

6.3 Summary

In this chapter, the presented results establish the strained HgTe bulk layer as a three dimensional topological insulator. Previous findings are confirmed and developed further. So, the dependence of the carrier density and mobility to the layer thickness is pointed out. This leads to a slight gain of density and mobility with increasing layer thickness if the HgTe layer is grown directly on the (001) CdTe substrate. Furthermore, a critical thickness of HgTe on

CdTe is measured to 155 nm via reciprocal space mapping by HRXRD. This allows to grow high quality, fully strained HgTe layers which provides the same band structure. Furthermore, the growth of the HgTe bulk layer embedded in HgCdTe barrier layers opens new possibilities, because this innovation increases the carrier mobility to over an order of magnitude. Here, carrier mobilities of HgTe bulk samples can reach the 1 000 000 cm^2/Vs mark and the density remains still at a low level (around 2×10^{11} cm^{-2}). As the whole Hg-based heterostructure shall remain fully strained, additionally the relaxation behavior of HgCdTe on two different CdTe substrates is determined by AFM, SEM and HRXRD. It turns out that the interface of the CdTe substrate is extremely relevant for the relaxation of the upcoming HgCdTe layer. Furthermore, for HgCdTe layers thicker than 1 μm, hillocks are generated by twin lamellae of the CdTe and in the depth of the critical thickness. Moreover, the effect of the HgCdTe cap layer thickness shows how the carrier density and mobility of the HgTe layers depend on the cap layer thickness. This is in good agreement with XPS and former quantum well measurements. In the end, first results of the usage of the CdTe/GaAs:Si as a back gate are demonstrated. Here, it can be seen easily that a new field of HgTe bulk analysis opens up by combining a top and back gate.

7 Summary

In the present thesis the MBE growth and sample characterization of HgTe structures is investigated and discussed. Due to the first experimental discovery of the quantum Spin Hall effect (QSHE) in HgTe quantum wells, this material system attains a huge interest in the spintronics society. Because of the long history of growing Hg-based heterostructures here at the Experimentelle Physik III in Würzburg, there are very good requirements to analyze this material system more precisely and in new directions. Since in former days only doped HgTe quantum wells were grown, this thesis deals with the MBE growth in the (001) direction of undoped HgTe quantum wells, surface located quantum wells and three dimensional bulk layers. All Hg-based layers were grown on CdTe substrates which generate strain in the layer stack and provide therefore new physical effects. In the same time, the (001) CdTe growth was investigated on n-doped (001) GaAs:Si because the Japanese supplier of CdTe substrates had a supply bottleneck due to the Tōhoku earthquake and its aftermath in 2011.
After a short introduction of the material system, the experimental techniques were demonstrated and explained explicitly. After that, the experimental part of this thesis is displayed. So, the investigation of the (001) CdTe growth on (001) GaAs:Si is discussed in chapter 4. Firstly, the surface preparation of GaAs:Si by oxide desorption is explored and analyzed. Here, rapid thermal desorption of the GaAs oxide with following cool down in Zn atmosphere provides the best results for the CdTe due to small holes at the surface, while e.g. an atomic flat GaAs buffer deteriorates the CdTe growth quality. The following ZnTe layer supplies the (001) growth direction of the CdTe and exhibits best end results of the CdTe for 30 seconds growth time at a flux ratio of Zn/Te $\approx$ 1/1.2. Without this ZnTe layer, CdTe will grow in the (111) direction. However, the main investigation is here the optimization of the MBE growth of CdTe. The substrate temperature, Cd/Te flux ratio and the growth time has to be adjusted systematically. Therefore, a complex growth process is developed and established. This optimized CdTe growth process results in a RMS roughness of around 2.5 nm and a FWHM value of the HRXRD ω-scan of 150 arcsec. Compared to the literature, there is no lower FWHM value traceable for this growth direction. Furthermore, etch pit density measurements show that the surface crystallinity is matchable with the commercial CdTe substrates (around 1×10^4 cm^{-2}). However, this whole process is not completely perfect and offers still room for improvements.
The growth of undoped HgTe quantum wells was also a new direction in research in contrast to the previous n-doped grown HgTe quantum wells. Here in chapter 5, the goal of very low carrier densities was achieved and therefore it is now possible to do transport experiments in the n - and p - region by tuning the gate voltage. To achieve this high sample quality, very precise growth of symmetric HgTe QWs and their HRXRD characterization is examined. Here, the quantum well thickness can now determined accurate to under 0.3 nm. Furthermore, the

transport analysis of different quantum well thicknesses shows that the carrier density and mobility increase with rising HgTe layer thickness. However, it is found out that the band gap of the HgTe QW closes indirectly at a thickness of 11.6 nm. This is caused by the tensile strained growth on CdTe substrates. Moreover, surface quantum wells are studied. These quantum wells exhibit no or a very thin HgCdTe cap. Though, oxidization and contamination of the surface reduces here the carrier mobility immensely and a HgCdTe layer of around 5 nm provides the pleasing results for transport experiments with superconductors connected to the topological insulator [119]. A completely new achievement is the realization of MBE growth of HgTe quantum wells on CdTe/GaAs:Si substrates. This is attended by the optimization of the CdTe growth on GaAs:Si. It exposes that HgTe quantum wells grown in-situ on optimized CdTe/GaAs:Si show very nice transport data with clear Hall plateaus, SdH oscillations, low carrier densities and carrier mobilities up to 500 000 cm^2/Vs. Furthermore, a new oxide etching process is developed and analyzed which should serve as an alternative to the standard HCl process which generates volcano defects at some time. However, during the testing time the result does not differ in Nomarski, HRXRD, AFM and transport measurements. Here, long-time tests or etching and mounting in nitrogen atmosphere may provide new elaborate results.

The main focus of this thesis is on the MBE growth and standard characterization of HgTe bulk layers and is discussed in chapter 6. Due to the tensile strained growth on lattice mismatched CdTe, HgTe bulk opens up a band gap of around 22 meV at the Γ-point and exhibits therefore its topological surface states. The analysis of surface condition, roughness, crystalline quality, carrier density and mobility via Nomarski, AFM, XPS, HRXRD and transport measurements is therefore included in this work. Layer thickness dependence of carrier density and mobility is identified for bulk layer grown directly on CdTe substrates. So, there is no clear correlation visible between HgTe layer thickness and carrier density or mobility. So, the carrier density is almost constant around 1×10^{11} cm^{-2} at 0 V gate voltage. The carrier mobility of these bulk samples however scatters between 5 000 and 60 000 cm^2/Vs almost randomly. Further experiments should be made for a clearer understanding and therefore the avoidance of unusable bad samples.But, other topological insulator materials show much higher carrier densities and lower mobility values. For example, Bi_2Se_3 exhibits just density values around 10^{19} cm^{-2} and mobility values clearly below 5000 cm^2/Vs. The carrier density however depends much on lithography and surface treatment after growth. Furthermore, the relaxation behavior and critical thickness of HgTe grown on CdTe is determined and is in very good agreement with theoretical prediction (d_c = 155 nm). The embedding of the HgTe bulk layer between HgCdTe layers created a further huge improvement. Similar to the quantum well structures the carrier mobility increases immensely while the carrier density levels at around 1×10^{11} cm^{-2} at 0 V gate voltage as well. Additionally, the relaxation behavior and critical thickness of these barrier layers has to be determined. HgCdTe grown on commercial CdTe shows a behavior as predicted except the critical thickness which is slightly higher than expected (d_c = 850 nm). Otherwise, the relaxation of HgCdTe grown on CdTe/GaAs:Si occurs in two parts. The layer is fully strained up to 250 nm. Between 250 nm and 725 nm the HgCdTe film starts to relax randomly up to 10 %. The relaxation behavior for thicknesses larger than 725 nm occurs than linearly to the inverse layer thickness. A explanation is given due to rough interface conditions and crystalline defects of the CdTe/GaAs:Si compared to the commercial CdTe substrate.

HRXRD and AFM data support this statement. Another point is that the HgCdTe barriers protect the active HgTe layer and because of the high carrier mobilities the Hall measurements provide new transport data which have to be interpreted more in detail in the future. In addition, HgTe bulk samples show very interesting transport data by gating the sample from the top and the back. It is now possible to manipulate the carrier densities of the top and bottom surface states almost separately. The back gate consisting of the n-doped GaAs substrate and the thick insulating CdTe buffer can tune the carrier density for $\Delta n \approx 3\times10^{11}$ cm^{-2}. This is sufficient to tune the Fermi energy from the p-type into the n-type region [138].
In this thesis it is shown that strained HgTe bulk layers exhibit superior transport data by embedding between HgCdTe barrier layers. The n-doped GaAs can here serve as a back gate. Furthermore, MBE growth of high crystalline, undoped HgTe quantum wells shows also new and extended transport output. Finally, it is notable that due to the investigated CdTe growth on GaAs the Hg-based heterostructure MBE growth is partially independent from commercial suppliers.

Zusammenfassung

In der vorliegenden Dissertation wurde das MBE-Wachstum von HgTe Strukturen erforscht und die anschließende Probencharakterisierung durchgeführt und diskutiert. Durch die erste experimentelle Entdeckung des Quanten-Spin-Hall-Effekts (QSHE) in HgTe Quantentrögen hat dieses Materialsystem großes Interesse im Gebiet der Spintronics erfahren. Aufgrund der langen Wachstumshistorie von quecksilberbasierenden Heterostrukturen am Lehrstuhl Experimentelle Physik III der Universität Würzburg sind die Voraussetzungen ausgesprochen gut, um dieses Materialsystem sehr ausführlich und auch in neue Richtungen hin zu untersuchen. Da vor dieser Doktorarbeit fast ausschließlich dotierte HgTe Quantentröge auf verschiedenen Substratorientierungen gewachsen wurden, beschäftigte sich diese Dissertation nun mit dem MBE-Wachstum von undotierten HgTe Quantentrögen, oberflächennahen Quantentrögen und dreidimensionalen Volumenkristallen. Alle quecksilberbasierenden Schichten wurden hierzu auf CdTe Substraten gewachsen, welche tensile Verspannung in den Schichten erzeugten und lieferten daher neue physikalische Effekte. In der selben Zeit wurde weiterhin das Wachstum von (001) CdTe auf n-dotiertem (001) GaAs:Si erforscht, da der japanische Zulieferer der CdTe Substrate eine Lieferengpass hatte aufgrund des Tōhoku Erdbebens und seinen verheerenden Folgen im Jahr 2011.
Die Erforschung des MBE-Wachstums von (001) CdTe auf (001) GaAs:Si wird im Kapitel 4 behandelt. Zuerst wurde hier die Oberflächenvorbereitung des GaAs:Si Substrates durch thermische Desorption untersucht und ausgewertet. Es stellte sich heraus, dass schnelle, thermische Desorption des GaAs - Oxides mit anschließendem Abkühlen in Zn Atmosphäre die besten Ergebnisse für das spätere CdTe durch kleine Löcher an der Oberfläche liefert, während zum Beispiel ein glatter GaAs Puffer das CdTe Wachstum verschlechtert. Der folgende ZnTe Film verschafft die gewünschte (001) Wachstumsrichtung für CdTe und weist bei 30 Sekunden Wachstumszeit bei einem Flussverhältnis von Zn/Te $\approx$ 1/1.2 die besten Endergebnisse für CdTe auf. Jedoch war die Haupterneuerung hier die Optimierung des CdTe Wachstums. Dafür wurde ein komplexer Wachstumsprozess entwickelt und etabliert. Dieser optimierte CdTe Wachstumsprozess lieferte Ergebnisse von einer RMS Rauigkeit von ungefähr 2.5 nm und FWHM Werte der HRXRD ω-Scans von 150 arcsec. Die Defektätzdichte-Messung zeigte weiterhin, dass die Oberflächenkristallinität vergleichbar mit kommerziell erwerbbaren CdTe Substraten ist (um 1×10^4 cm^{-2}). Des Weiteren ist kein niedrigerer Wert für die Halbwertsbreite des ω-Scans in der Literatur für diese Wachstumsrichtung aufgeführt. Dies spiricht ebenfalls für die hohe Qualität der Schichten. Jedoch ist dieser Wachstumsprozess noch nicht endgültig ausgereift und bietet weiterhin noch Platz für Verbesserungen.
Das Wachstum von undotierten HgTe Quantentrögen war ebenso eine neue Forschungsrichtung im Gegensatz zu den dotierten HgTe Quantentrögen, die in der Vergangenheit gewachsen wurden. Das Ziel hierbei, die Ladungsträgerdichte zu verringern, wurde erreicht und daher ist

es nun möglich, Transportexperimente sowohl im n- als auch im p-Regime durchzuführen, indem eine Gatespannung angelegt wird. Des Weiteren experimentierten andere Arbeitsgruppen mit diesen Quantentrögen, bei denen die Fermi Energie in der Bandlücke liegt [143]. Außerdem wurde das sehr präzise MBE Wachstum anhand von symmetrischen HgTe Quantentrögen und ihren HRXRD Charakterisierungen behandelt. Daher kann nun die Quantentrogdicke präzise auf 0,3 nm angegeben werden. Die Transportergebnisse von verschieden dicken Quantentrögen zeigten, dass die Ladungsträgerdichte und Beweglichkeit mit steigender HgTe Schichtdicke zunimmt. Jedoch wurde auch herausgefunden, dass sich die Bandlücke von HgTe Quantentrögen indirekt bei einer Dicke von 11.6 nm schließt. Dies wird durch das verspannte Wachstum auf CdTe Substraten verursacht. Überdies wurden oberflächennahe Quantentröge untersucht. Diese Quantentröge besitzen keine oder nur eine sehr dünne HgCdTe Deckschicht. Allerdings verringerte Oxidation und Oberflächenverschmutzung hier die Ladungsträgerbeweglichkeit dramatisch und eine HgCdTe Schicht von ungefähr 5 nm lieferte ansprechende Transportergebnisse für Supraleiter, die den topologischen Isolator kontaktieren. Eine komplett neue Errungenschaft war die Realisierung, via MBE, HgTe Quantentröge auf CdTe/GaAs:Si Substrate zu wachsen. Dies ging einher mit der Optimierung des CdTe Wachstums auf GaAs:Si. Es zeigte sich, dass HgTe Quantentröge, die in-situ auf optimierten CdTe/GaAs:Si gewachsen wurden, sehr schöne Transportergebnisse mit deutlichen Hall Quantisierungen, SdH Oszillationen, niedrigen Ladungsträgerdichten und Beweglichkeiten bis zu 500 000 cm^2/Vs erreichen. Des Weiteren wurde ein neues Oxidätzverfahren entwickelt und untersucht, welches als Alternative zum Standard-HCl-Prozess dienen sollte, da dieses manchmal vulkan-artige Defekte hervorruft. Jedoch ergab sich kein Unterschied in den Nomarski, HRXRD, AFM und Transportexperimenten. Hier könnten vielleicht Langzeittests oder Ätzen und Befestigen in Stickstoffatmosphäre neue, gewinnbringende Ergbnisse aufzeigen.

Der Hauptfokus dieser Doktorarbeit lag auf dem MBE Wachstum und der Standardcharakterisierung von HgTe Volumenkristallen und wurde in Kapitel 6 diskutiert. Durch das tensil verpannte Wachstum auf CdTe entsteht für HgTe als Volumenkristall eine Bandlücke von ungefähr 22 meV am Γ Punkt und zeigt somit seine topologischen Oberflächenzustände. Die Analyse der Oberfächenbeschaffenheit, der Rauigkeit, der kristallinen Qualität, der Ladungsdrägerdichte und Beweglichkeit mit Hilfe von Nomarski, AFM, XPS, HRXRD und Transportmessungen ist in dieser Arbeit anzutreffen. Außerdem wurde die Schichtdickenabhängigkeit von Ladungsträgerdichte und Beweglichkeit von HgTe Volumenkristallen, die direkt auf CdTe Substraten gewachsen wurden, ermittelt worden. So erhöhte sich durchschnittlich die Dichte und Beweglichkeit mit zunehmender HgTe Schichtdicke, aber die Beweglichkeit ging selten über $\mu \approx 40\,000$ cm^2/Vs hinaus. Die Ladungsträgerdichte n hing jedoch sehr von der Litographie und der Behandlung der Oberfläche nach dem Wachstum ab. Des Weiteren wurde das Relaxationsverhalten und die kritische Dicke bestimmt, welches sehr gut mit den theoretischen Vorhersagen übereinstimmt (d_c = 155 nm). Das Einbetten des HgTe Volumenkristalls in HgCdTe Schichten brachte eine weitere große Verbesserung mit sich. Ähnlich wie bei den Quantentrögen erhörte sich die Beweglichkeit μ immens, während sich die Ladungsträgerdichte bei ungefähr 1×10^{11} cm^{-2} einpendelte. Zusätzlich wurde auch hier das Relaxationsverhalten und die kritische Schichtdicke dieser Barrierenschichten ermittelt. HgCdTe, gewachsen auf kommerziellen CdTe Substraten, zeigte ein Verhalten ähnlich zu dem Erwarteten mit der Aus-

nahme, dass die kritische Schichtdicke leicht höher ist als die Vorhergesagte (d_c = 850 nm). Auf der anderen Seite findet die Relaxation von HgCdTe auf CdTe/GaAs:Si zweigeteilt ab. Bis 250 ist die Schicht noch voll verspannt. Zwischen 250 nm und 725 nm beginnt die HgCdTe Schicht willkürlich bis zu 10 % zu relaxieren. Das Relaxationsverhalten für Dicken über 725 nm findet dann wieder linear zur invers aufgetragenen Schichtdicke statt. Eine Erklärung wurde durch das raue Interface der Schichten und der Defekte im Kristall von CdTe/GaAs:Si gegeben, im Vergleich zu den kommerziellen CdTe Substraten. HRXRD und AFM Ergebnisse belegten diese Aussage. Die HgCdTe Barrieren schützen die aktive HgTe Schicht und daher liegen nach Hall Messungen aufgrund der hohen Ladungsträgerbeweglichkeiten neue Transportergbnisse vor, welche in der Zukunft ausführlicher interpretiert werden müssen. Darüber hinaus zeigten HgTe Volumenkristalle neue, interessante Transportergebnisse durch das gleichzeitige Benutzen eines Top- und Backgates. Es ist nun möglich, die Ladungsträger der oberen und unteren Oberflächenzustände nahezu getrennt zu verändern und zu ermitteln. Das Backgate, bestehend aus dem n-dotierten GaAs:Si Substrate und dem dicken isolierenden CdTe Puffer, kann die Ladungsträgerdichte um ungefähr $\Delta n \approx 3\times10^{11}$ cm^{-2} varieren. Das ist ausreichend, um die Fermi Energie vom p- in den n-Bereich einzustellen [138].
In dieser Dissertation wurde also gezeigt, dass verspannte HgTe Volumenkristalle durch das Einbetten in HgCdTe Barrieren neue Transportergebnisse liefern. Das n-dotierte GaAs konnte hierbei als Backgate genutzt werden. Des Weiteren zeigte das MBE Wachstum von hochkristallinen , undotiereten HgTe Quantentrögen ebenso neue und erweiterte Transportergebnisse. Zuletzt ist es bemerkenswert, dass durch das erforschte CdTe Wachstum auf GaAs das MBE Wachstum von quecksilberbasierenden Heterostrukturen auf CdTe Substraten teilweise unabhänigig ist von kommerziellen Zulieferbetrieben.

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List of publications

Full papers - published

* FABRICATION OF SAMPLES FOR SCANNING PROBE EXPERIMENTS ON QUANTUM SPIN HALL EFFECT IN HGTE QUANTUM WELLS.
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Erklärung

Hiermit erkläre ich, dass ich die vorliegende Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel verwendet habe. Die Arbeit wurde keiner anderen Prüfungsbehörde zur Erlangung eines akademischen Grades vorgelegt.

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