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Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors

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In organic thin-film transistors (TFTs) fabricated in the inverted (bottom-gate) device structure, the surface roughness of the gate dielectric onto which the organic-semiconductor layer is deposited is expected to have a significant effect on the TFT characteristics. To quantitatively evaluate this effect, a method to tune the surface roughness of a gate dielectric consisting of a thin layer of aluminum oxide and an alkylphosphonic acid self-assembled monolayer over a wide range by controlling a single process parameter, namely the substrate temperature during the deposition of the aluminum gate electrodes, is developed. All other process parameters remain constant in the experiments, so that any differences observed in the TFT performance can be confidently ascribed to effects related to the difference in the gate-dielectric surface roughness. It is found that an increase in surface roughness leads to a significant decrease in the effective charge-carrier mobility and an increase in the subthreshold swing. It is shown that a larger gate-dielectric surface roughness leads to a larger density of grain boundaries in the semiconductor layer, which in turn produces a larger density of localized trap states in the semiconductor.

1. Introduction

Organic thin-film transistors (TFTs) are promising devices to be employed in future flexible, large-area electronics applications, such as active-matrix displays and sensor arrays.[1–3] The possibility to deposit organic semiconductors at relatively low temperatures makes it possible to fabricate organic TFTs on unconventional substrate materials, such as glass,[4,5] plastic foils,[6–8] textiles,[9] or paper.[10,11] The use of these substrate materials offers opportunities for a variety of novel applications, but they are usually characterized by a larger surface roughness than conventional substrate materials, and this can have detrimental effects on the performance of the devices.[12–26]

In this work we study the impact of the surface roughness of the gate dielectric on the electrical performance of bottom-gate organic TFTs. As model organic semiconductor, we employ the small-molecule semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT[27]), since its unique combination of electrical performance and long-term stability makes it ideally suited for this investigation.[28–31]

Since the current–voltage characteristics of organic TFTs depend on various parameters other than the surface roughness,[32,33] it is important that the only parameter we vary in our experiments is the surface roughness, as simultaneous changes in other parameters might obscure the effect we intend to investigate. All TFTs were thus fabricated using the same materials, the same layer thicknesses, and the same process conditions, with one exception, namely the substrate temperature during the deposition of the aluminum gate electrodes (in order to analyze the impact of the surface roughness) or the substrate temperature during the deposition of the organic semiconducting layer (in order to disentangle the relations between the surface roughness of the gate dielectric, the grain density of the semiconductor layer, and the density of trap states in the organic-semiconductor layer). By varying the substrate temperature during the aluminum deposition we are able to tune the surface roughness of the gate electrode and thereby the surface roughness of the gate dielectric over approximately one order of magnitude without having to change any other process parameters, so that any differences observed in the TFT

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performance can be safely ascribed to differences in the gate-dielectric surface roughness. By varying the substrate temperature during the DNTT deposition we can control the density of grain boundaries in the DNTT layer independent of the gate-dielectric surface roughness.

2. Results and Discussion

2.1. Gate-Dielectric Surface Roughness

To fabricate TFTs with different degrees of gate-dielectric surface roughness, we prepared a set of eight substrates in which we modified the surface roughness of the aluminum gate electrodes by controlling the substrate temperature during the aluminum deposition. The surface of the aluminum was then oxidized by brief exposure to an oxygen plasma, and the resulting aluminum oxide layer (AlO_X) was then covered with an alkylphosphonic acid self-assembled monolayer (SAM). Due to the fact that the formation of these layers proceeds in a conformal manner, the surface roughness of the aluminum translates directly into the surface roughness of the AlO_X/SAM gate dielectric, as will be shown. A schematic cross section of the TFTs and the chemical structures of *n*-tetradecylphosphonic acid and DNTT are shown in **Figure 1**. The composition of the AlO_X in the gate dielectric is discussed in Section S1, Supporting Information.

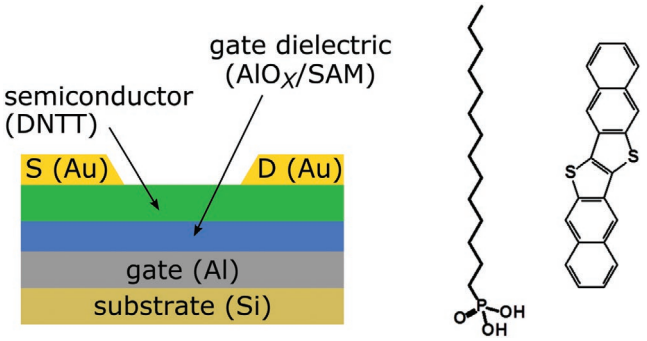

Figure 1. Schematic cross-section of the organic TFTs and chemical structures of *n*-tetradecylphosphonic acid for the gate-dielectric SAM and the organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT).

Using atomic force microscopy (AFM), we measured the surface roughness of the aluminum gate electrodes and of the AlO_X/SAM gate dielectrics. **Figure 2**a–c shows AFM images of AlO_X/SAM gate dielectrics fabricated on aluminum gate electrodes deposited at substrate temperatures of 20, 70, and 110 °C. As can be seen, the substrate temperature during the deposition of the aluminum gate electrodes has a significant influence on the morphology of the aluminum films and hence on their root-mean-square surface roughness R_{RMS}. With increasing substrate temperature, both the lateral aluminum grain size and the surface roughness increase. In Figure 2d, the measured surface roughness is plotted as a function of the

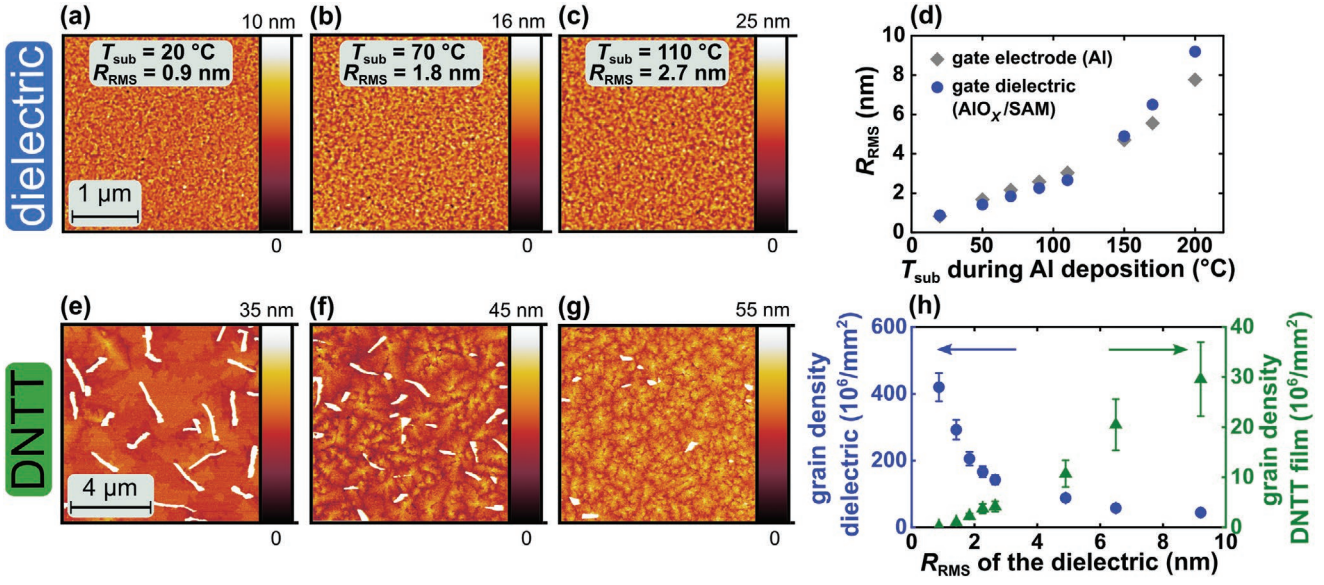

Figure 2. a–c) AFM images of AlO_X/SAM gate dielectrics fabricated on aluminum gate electrodes deposited at substrate temperatures of 20, 70, and 110 °C. d) Root-mean-square surface roughness of aluminum gate electrodes (gray symbols) and AlO_X/SAM gate dielectrics (blue symbols) plotted as a function of the substrate temperature during the aluminum deposition. A higher substrate temperature results in a larger surface roughness of the aluminum which translates directly into a larger gate-dielectric surface roughness. e–g) AFM images of DNTT films deposited onto the gate dielectrics shown in panels (a)–(c) at a substrate temperature of 60 °C. A larger surface roughness of the gate dielectric leads to a terrace structure of strongly reduced terrace size in the DNTT films and a larger grain density. The tall, elongated features seen in the AFM images are crystalline structures with a height of several tens of nanometers that form spontaneously during the organic-semiconductor deposition.[45] h) Grain densities of the aluminum gate electrodes and of the DNTT films plotted as a function of the surface roughness of the gate dielectric. The grain density was determined using the Watershed Algorithm implemented in the AFM analysis software Gwyddion.

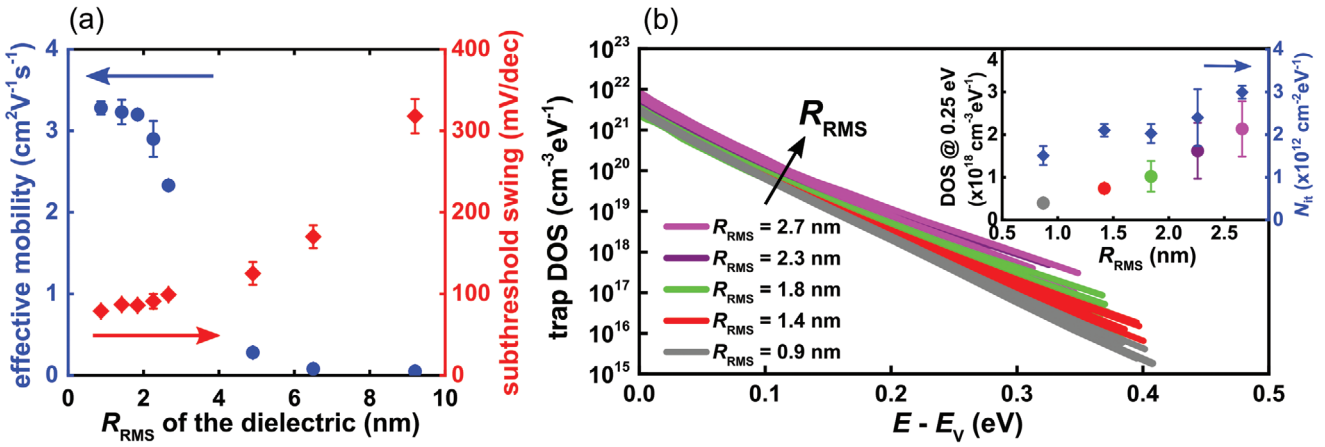

Figure 3. a) Effective charge-carrier mobility extracted in the linear regime of operation and subthreshold swing of the DNTT TFTs plotted as function of the surface roughness of the gate dielectric. b) Density of trap states (trap DOS) in the organic semiconductor plotted as function of the energy above the valence-band energy E_V. The inset shows the value of the trap DOS at an energy of 0.25 eV above the valence-band energy as a function of the surface roughness of the gate dielectric as well as the interface trap density, N_{it}, calculated from the subthreshold swing.

substrate temperature during the aluminum deposition for the complete set of substrates. The gray and blue data points represent the surface roughness R_{RMS} of the aluminum gate electrodes and of the AlO_X/SAM gate dielectrics, respectively. As can be seen, the surface roughness of the gate dielectric is essentially identical to that of the aluminum gate electrode on which the gate dielectric is fabricated, which confirms that the formation of the AlO_X/SAM gate dielectric occurs in a correlated manner. The surface roughness of the gate electrodes and the gate dielectric increases monotonically from 0.9 to 9.2 nm as the substrate temperature during the aluminum deposition is increased from 20 to 200 °C. A similar relation between the surface roughness of aluminum films and the temperature during the aluminum deposition was previously reported by Z. Li et al. during the deposition of significantly thicker aluminum films by electron-beam evaporation for the fabrication of high-quality Echelle gratings.[34]

The observed dependence of the surface roughness of the aluminum films on the substrate temperature during the aluminum deposition can be explained by considering the processes of nucleation and coalescence of the aluminum atoms on the substrate surface. During deposition, the aluminum adatoms rapidly reach thermal equilibrium with the surface, diffuse on the surface, and interact to form immobile polyatomic clusters which will act as seeds for the subsequent formation of the aluminum grains.[35,36] A higher substrate temperature enhances the surface diffusion of the adatoms, which results in the requirement for a larger critical size of the stable nuclei, resulting in a larger surface roughness.[34,37,38] The plasma-generated aluminum oxide layer and the alkylphosphonic acid SAM follow the surface topology of the aluminum films, as is evident from the correlated surface roughness seen in Figure 2d. With this simple approach, the surface roughness can be tuned continuously over approximately an order of magnitude without the need to vary any other process parameters. In particular, it is not necessary to use different materials or to perform any post-process modifications to any of the layers in order to produce different degrees of surface roughness, which is an important benefit, because such modifications might affect the TFT performance in other ways and thereby obscure the surface-roughness effect of interest.

2.2. Electrical TFT Characteristics and Trap-State Density

On each substrate, DNTT TFTs with the same dimensions were fabricated. Their transfer and output characteristics are shown in Figures S2 and S3, Supporting Information. The extracted effective charge-carrier mobilities and subthreshold swings are summarized in **Figure 3**a. With increasing surface roughness, the effective mobility decreases substantially from (3.3 ± 0.8)cm^2 V^{-1} s^{-1} on the smoothest substrate to (0.05 ± 0.01)cm^2 V^{-1} s^{-1} on the roughest substrate. The subthreshold swing increases from (79 ± 3)mV dec^{-1} on the smoothest substrate to (320 ± 21)mV dec^{-1} on the roughest substrate. We have applied the extended Grünewald method to extract the density of trap states (trap DOS) in the organic-semiconductor layer from the measured transfer curves of the TFTs in the linear regime of operation.[39] We were able to apply this method only to the TFTs on the five smoothest substrates, since the TFTs on the three rougher substrates do not meet the criteria for a meaningful extraction of the trap DOS from the transfer curves of the TFTs. The results are summarized in Figure 3b where the trap DOS in the semiconductor is plotted as a function of the energy relative to the valence-band edge for the five smoothest substrates. The characteristic decay of the trap DOS into the band gap is in agreement with other reports on vacuum-deposited films of the organic semiconductor DNTT.[40,41] The results in Figure 3b show a clear correlation between the surface roughness of the gate dielectric and the density of trap states in the organic semiconductor layer. **Figure 4** illustrates the general view of how the roughness of the underlying surface (in this case of the gate dielectric) affects the growth and morphology of the organic semiconductor layer by increasing the degree of structural disorder.

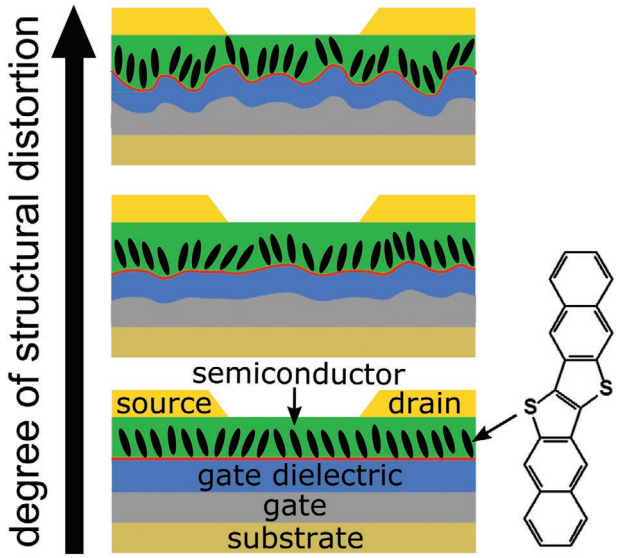

Figure 4. A rough gate electrode correlates with a rough gate dielectric and introduces structural distortion in the semiconductor film. This structural distortion, represented mainly by grain boundaries and their density, leads to the formation of transport barriers and trap states that have a detrimental effect on the electric characteristics of the TFTs.

2.3. Organic-Semiconductor Morphology

As initially proposed by Anderson, among the factors that can cause the localization of charge carriers in a semiconductor is structural disorder.[42] In organic semiconductors, intermolecular interactions are comparatively weak and the transfer integrals are typically small and susceptible to small differences in molecular position or orientation, so these materials are especially prone to the formation of trap states due to structural disorder. One manifestation of the degree of structural disorder in organic semiconductors is the density of grain boundaries. The influence of the gate-dielectric surface roughness on the thin-film morphology and the grain density of the vacuum-deposited DNTT films can be seen in Figure 2e–g: Depositing the DNTT onto a smooth gate dielectric leads to a step-flow growth and thus to an extended terrace-like structure, which is the structure typically reported for many small-molecule organic semiconductors deposited by vacuum sublimation,[43–45] whereas a rough gate dielectric hinders this growth mode and thus induces less extended terrace-like structures correlated with a larger density of smaller domains. This trend is in agreement with observations reported previously for other small-molecule organic semiconductors, such as pentacene, and can be ascribed to a smaller diffusion length of the molecules when deposited onto a rougher surface.[46] The larger grain density in the semiconductor layer observed on rougher surfaces corresponds to a larger density of grain boundaries. In organic semiconductors, grain boundaries are the most important type of structural defect at the micrometer and sub-micrometer length scale. Energy barriers emerging at the grain boundaries and trap states located there are often reported to be a major obstacle for efficient charge transport.[47–51] We have also observed that the effective charge-carrier mobility and the subthreshold swing correlate with the density of grain boundaries imaged by AFM, but it should be noted that AFM reveals only the surface of the organic semiconductor layer, whereas the charge transport occurs mainly in the first molecular monolayer near the interface to the gate dielectric, that is, at a depth that cannot be probed directly by AFM and where structural or chemical inhomogeneities on smaller length scales affecting the charge transport might exist. Due to the weak van der Waals bonding, organic semiconductors are susceptible to imperfect molecular packing and local defects.[52] It has been calculated that even in macroscopically ordered regions of an organic-semiconductor film, local defects induced along the less strongly bound molecular gliding planes lead to the formation of shallow trap states that significantly impede charge transport.[53–56]

In order to disentangle the influence of the density of grain boundaries in the semiconductor layer on the TFT characteristics from the influence of other types of structural disorder, we fabricated a second set of substrates in which we tuned the grain density in the DNTT layer independently of the surface roughness of the gate dielectric. All four substrates in this series were fabricated at the same substrate temperature during the aluminum deposition (20 °C), so that all substrates have the same small gate-dielectric surface roughness. During the DNTT deposition, the substrate was held at a temperature of 20, 40, 60, or 80 °C in order to obtain a different grain density on each substrate. As can be seen in **Figure 5**a, the influence of the substrate temperature during the DNTT deposition on the grain density is quite similar to that of the surface roughness of the gate dielectric. By comparing the electrical characteristics of the TFTs from the first set of substrates (for which the grain density was tuned indirectly by manipulating the surface roughness of the gate dielectric) with those from the second set of substrates (for which the grain density was tuned directly by adjusting the substrate temperature during the DNTT deposition), the importance of the density of grain boundaries relative to other types of disorder induced, for instance, by the gate-dielectric surface roughness can be analyzed in more detail. As seen in Figure 5b,c, the trends and absolute values of the effective mobility and of the subthreshold swing coincide remarkably well for both sets of substrates. We also applied the extended Grünewald method to the TFTs from the second set of substrates to extract the trap DOS. Figure 5d shows that the relation between the grain density and the trap DOS is very similar for the two sets of substrates. These results suggest that the grain boundaries are indeed the most important type of structural defect in DNTT films, regardless of whether they are induced by the surface roughness of the gate dielectric or by the substrate temperature during the DNTT deposition. Contributions by other types of structural imperfections cannot be ruled out, but appear to be less significant.

To quantify the influence of the gate-dielectric surface roughness on the microstructure of the DNTT films in more detail and, complementary to the local AFM analysis, in an integral manner, we have performed X-ray diffraction (XRD) measurements on DNTT films deposited onto AlO_X/SAM gate dielectrics with a surface roughness of 1.0, 2.2, 4.9, and 7.0 nm, respectively. The results are shown in **Figure 6**; Figure S8, Supporting Information. The first-order Bragg peak is located at a reciprocal scattering length of 0.385Å^{-1}, which is in agreement with the value expected for DNTT and its (001) out-of-plane

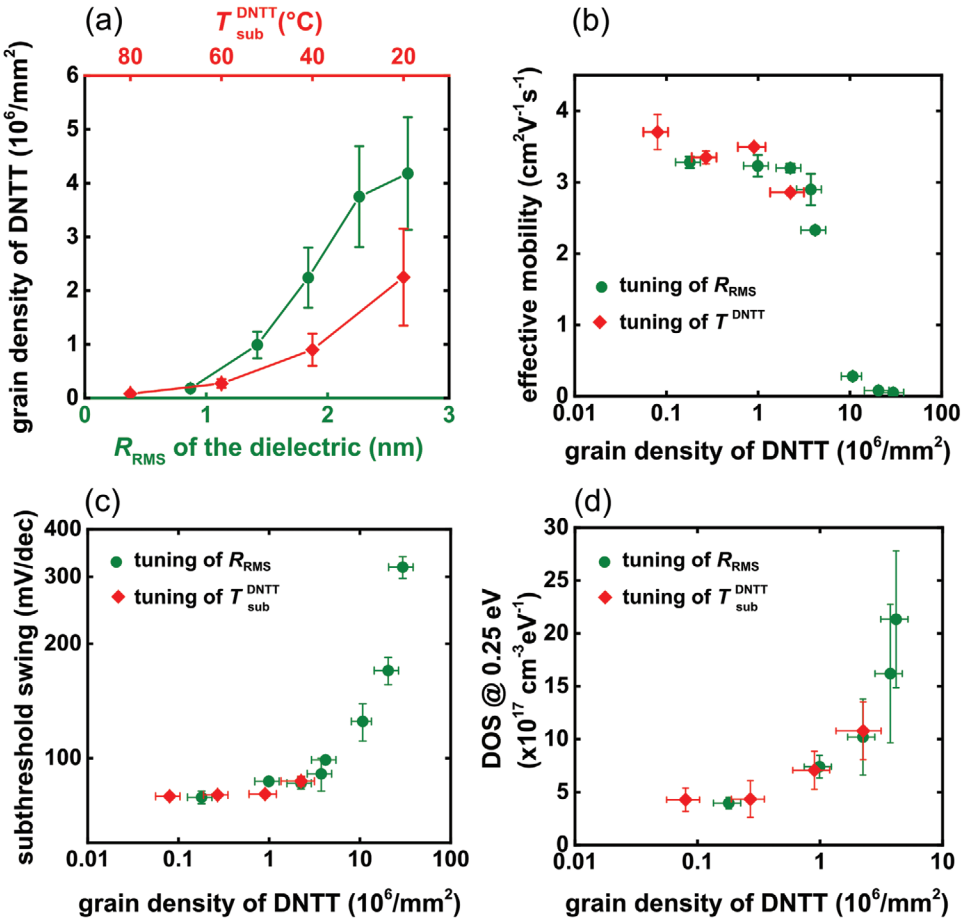

Figure 5. a) Grain densities of DNTT films plotted as a function of the roughness of the gate dielectric and as a function of the substrate temperature during the DNTT deposition. b) Effective carrier mobility and c) subthreshold swing of the TFTs of the two sets of substrates in which the grain density of DNTT was tuned by two different methods. d) Trap DOS at an energy of 0.25 eV above the valence-band edge, determined by the extended Grünewald method. The increase of the trap-state density with increasing grain density is analogous for both sets of substrates.

lattice spacing of 16.19Å.[57] With increasing gate-dielectric surface roughness, the absolute intensity of the first-order Bragg peak decreases monotonically. In order to analyze the influence of the gate-dielectric surface roughness on the angular orientation of the DNTT domains within the DNTT layer, we have evaluated rocking scans of the first-order Bragg reflections. As seen in Figure S8 the rocking scans reveal a sharp specular Bragg intensity at their center and a broad superimposed background originating from diffusive scattering by structural imperfections.[58] The rocking width of the specular Bragg component in the rocking scan is typically associated with the average tilting of the crystalline grains towards the out-of-plane direction, known as mosaicity spread.[57] Hardly any difference in the rocking width of the Bragg peaks is observed in our measurements, suggesting that the surface roughness of the gate dielectric has no measurable influence on the tilting angle of the grains in the vacuum-deposited DNTT layers, which means that the mosaicity spread has no measurable effects on the charge-transport properties. Likewise, there is essentially no variance in the intensity ratio between the area under the Bragg peak and the area under the total spectrum, which suggests that the degree of structural disorder within the grains is not significantly affected by the gate-dielectric surface roughness.[59,60] In summary, the XRD analysis confirms independently that the surface roughness of the gate dielectric does not have a significant impact on the internal morphology of the DNTT grains, which suggests that the TFT characteristics are determined exclusively by the density of grain boundaries along the lateral transport channels within the DNTT layers.

3. Conclusion

In this study we investigated the relation between the surface roughness of the gate dielectric and the electrical characteristics of bottom-gate organic TFTs based on the small-molecule semiconductor DNTT. By controlling the substrate temperature during the deposition of the aluminum gate electrodes, we were able to systematically vary the degree of surface roughness of the gate dielectric over approximately one order of magnitude. We found that the effective charge-carrier mobility decreases and the subthreshold swing increases significantly with increasing surface roughness. We reported a correlation between the gate-dielectric surface roughness and the

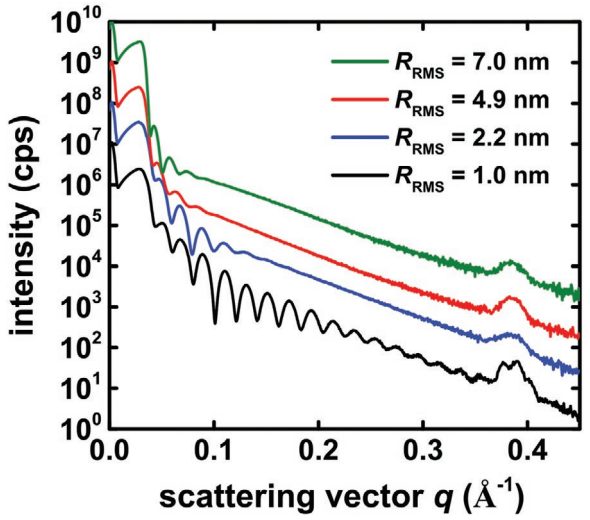

Figure 6. XRD intensities for DNTT films deposited onto gate dielectrics with different surface roughness. The curves are displaced with respect to each other for sake of clarity. The XRD signal from the DNTT film deposited onto the smoothest gate dielectric shows Kiessig oscillations up to high momentum values, which indicates that this DNTT film has a very homogeneous thickness related to the extremely small correlated interface roughness. With increasing roughness the Kiessig fringes are rapidly damped. The (001) Bragg peaks are located at a reciprocal scattering length of 0.385Å^{-1}.

experimentally measured trap density of states in the organic semiconductor. This analysis indicates that grain boundaries, induced by the surface roughness of the gate dielectric, severely hinder charge transport in the organic-semiconductor layer. Our results emphasize the importance of a small surface roughness of the gate dielectric for bottom-gate organic TFTs.

4. Experimental Section

Sample Fabrication: All TFTs were fabricated on doped silicon wafers in the inverted staggered (bottom-gate, top-contact) device structure. As the gate electrode, a 30-nm-thick layer of aluminum was deposited by thermal evaporation in vacuum using a deposition rate of 1.8 nm s^{-1}. The nominal thickness of the metal and organic-semiconductor layers was monitored using a quartz crystal microbalance. For the first part of this study, we fabricated a set of eight substrates in which we tuned the surface roughness of the gate dielectric by performing the aluminum deposition at different substrate temperatures. For this purpose, the substrate was held at a constant temperature T_{sub} of 20, 50, 70, 90, 110, 150, 170, or 200 °C during the aluminum deposition. One substrate was fabricated for each of these eight different substrate temperatures. (In addition, one substrate was prepared on which the aluminum was deposited at a substrate temperature of −24 °C. However, this deposition required the use of a different evaporation system in which the deposition rate is limited to 1Å s^{-1}. At this smaller deposition rate, the aluminum surface roughness is significantly larger.) The aluminum gate electrodes were not patterned. The aluminum surface was briefly exposed to an oxygen plasma to increase the thickness of the native AlO_X layer to 3.6 nm.[61,62] The substrates were then immersed into a 2-propanol solution of *n*-tetradecylphosphonic acid to form a SAM with a thickness of 1.7 nm. The hybrid AlO_X/SAM gate dielectric has a total thickness of 5.3 nm and a unit-area capacitance of 0.7 µF cm^{-2}. Subsequently, a 25-nm-thick layer of the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich) was deposited by thermal sublimation in vacuum using a deposition rate of 0.03 nm s^{-1}. For the eight substrates employed in the first part of this study, the substrate was held at a constant temperature of 60 °C during the DNTT deposition. For the second part of this study, we fabricated a set of four substrates in which we tuned the microstructure of the DNTT layer by performing the DNTT deposition at different substrate temperatures. On these four substrates, the deposition of the aluminum gate electrodes was performed with a constant substrate temperature of 20 °C in order to obtain the same surface roughness for all four substrates, but during the DNTT deposition, the substrate was held at a temperature of 20, 40, 60, or 80 °C. The final process step for all substrates was the deposition of a 30-nm-thick layer of gold through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the source and drain contacts on the surface of the organic-semiconductor layer. The gold was deposited with a rate of 0.03 nm s^{-1}. All TFTs had a channel length of 100 µm and a channel width of 200 µm. The vacuum depositions were performed at a base pressure of 10^{-6} mbar.

Sample Characterization: AFM was performed using a Bruker Dimension Icon system in tapping mode in ambient air. The XRD measurements were carried out with a Seifert/General Electric XRD 3003 T/T diffractometer using monochromatic Cu-Kα_1 radiation with a wavelength of 1.5406 Å. The electrical measurements were performed in ambient air at room temperature using a manual probe station and an Agilent 4156C Semiconductor Parameter Analyzer. The transfer characteristics of the TFTs were measured at a drain-source voltage of −0.1 V and by sweeping the gate-source voltage in steps of −50 mV. The effective charge-carrier mobility was calculated by fitting the following equation to the measured transfer curves:

$$\mu_{\text{eff}} = \frac{L}{WC_{\text{diel}}V_{\text{DS}}}\frac{\partial I_{\text{D}}}{\partial V_{\text{GS}}} \tag{1}$$

where L is the channel length, W the channel width, C_{diel} the unit-area capacitance of the gate dielectric, V_{DS} the drain-source voltage, I_D the drain current, and V_{GS} the gate-source voltage. The subthreshold swing was calculated by fitting the following equation to the subthreshold region of the measured transfer curve:

$$S = \frac{\partial V_{\text{GS}}}{\partial\left(\log_{10}\left(I_{\text{D}}\right)\right)} \tag{2}$$

The measured subthreshold swing can be used to estimate the trap density at the semiconductor/dielectric interface[63]:

$$N_{\text{it}} = \frac{C_{\text{diel}}}{e^2}\left[\frac{eS}{k_{\text{B}}T\ln(10)}\right] \tag{3}$$

where e is the elementary charge, T the temperature and k_B the Boltzmann constant.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

grain boundaries, organic thin-film transistors, surface roughness

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