Effects of structure, sub-micrometer scaling, and environmental conditions on π-conjugated organic semiconductors in OFET devices.

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Chapter 1

Introduction

The world of electronic applications is based on silicon technology and will last for more than just a while. Parallel to this the fast-paced development of technologies since the end of World War II has also created the entrance of more and more artificial materials in daily life. E.g. when in the middle of the last century nylon was still a luxury product the chemical industry soon made it commodity. Plastics became omnipresent. The large variety and usability of these carbon based products let them enter the human society of the 20^{th} century like no other family of material. It can be discussed which of the two had the biggest impact on human society: electronic technologies (computers, communication, etc.) or plastics. As the words say: plastic electronics combines these technologies. This thesis is an approach to understand a little more of the world of organic semiconductors for plastic electronics.

Although the physical properties of organic crystals had been observed early at the same time as for the inorganic materials in the 19^{th} century (e.g. the optical character of anthracene and anthraquinone derivatives by Sir George Gabriel Stokes [1]), the further development was focusssed on the inorganic materials for more than a century. Thus, the intensified research on the electrical properties of the organic materials is still a young field of research. The pioneer investigations of A.G. Mac Diarmid, A. J. Heeger and H. Shirakawa on the conductive organic material of polyacetylene, rewarded by the Nobel price [2] in the year 2000 date back to 1977. This triggered a new materials research which combined a variety of scientific disciplines like material chemistry, quantum chemistry, physics of condensed matter, device physics to name a few. Soon the advances in the three classes of electrical conductance, the conductive, the isolating and the semiconducting organic materials created the vision of plastic electronics in the mind of scientists, engineers and businessmen. After these 30 years of research and development plastic electronics are on their jump to market in many areas. Since the outstanding properties of silicon technologies can not be challenged, on the one hand low-cost mass applications, and on the other hand niche products are planned in various fields of application. In this context four main fields should be mentioned: the organic light emitting diode (OLED) has developed

a cost and energy efficient light source which is technically mature for applications in conventional LED lighting and display technology. Organic photovoltaics (OPV) in 3^{rd} generation solar cells are envisioned to surpass the maximum efficiency limit of crystalline solar cells[1](1. generation solar cells) by maintaining the cost-efficient performance of conventional thin film solar cells (2. generation) [4]. Although these high performance of all organic solutions in photovoltaics, is still a future perspective, even mediocre efficiencies in combination with a low-cost and high-volume production should offer many opportunities for research and business. Organic materials are also candidates in sensor applications due to a variety of properties like their tunability of electronic properties via chemical synthesis, compatibility with mechanically flexible substrates, low-cost manufacturing, and facile integration with chemical and biological functionalities [5]. This means either the direct application of the OSC as optical or electrical sensors or a sensor application using OSC devices. The fourth field are the integrated circuits of organic material which benefit from low-cost manufacturing (printed electronics), the use of mechanically flexible substrates, and from the transparency of some organic material.

In the world of electronics the transistor is the main workhorse of integrated circuits. It defines their logics and thus their way of working. Therefore, the organic field effect transistor (OFET) or in other words (nearer to the layer by layer manufacturing method): the organic thin-film transistor (OTFT) has attracted the biggest attention of research among the organic semiconducting devices.

The aim of this thesis is twofold: on the one hand it is dedicated to the physics of organic semiconductors investigated with the OFET device. On the other hand in some parts the thesis analyses more the device physics of the OFET itself - the placing of the objectives makes the small difference. Many of the oncoming experimental results and the conclusions drawn from them evolved in the context with projects in the Fifth and Sixth Framework Programme of the European Union and the “DFG Schwerpunkt OFET”, sponsored by the German Research Society. To name also the European projects: this work has benefited a lot from the NAIMO project (“Nanoscale integrated processing of self organizing multifunctional organic materials”) and its predecessor MONA LISA (“Development of novel conjugated molecular nanostructures by lithography and their transport scaling aspects“). The subject of these projects can be subsumed in one sentence: to acquire knowledge on organic semiconductors for certain applications by investigating their inherent properties, structure and manufacturability. The projects once more have proved the need for interdisciplinary research among different kinds of partners not only regarding their scientific disciplines but also regarding their way of working. The latter is defined by a partner’s interests in the field which might be different among industrial, research institutes, and university partners.

After this motivating passage the attention should be drawn to the oncoming subjects of the thesis. In the following chapters organic semiconductors of different structure and transport properties will be discussed. Furthermore the influence of structural ordering

[1] Up to 40% depending on material, for Si up to 30% [3]

of the organic semiconductors is monitored by their inherent electrical properties accessible by various applied methods, and by the scaling behaviour of the main OFET device parameters. Different ordering within the same material will be induced by varying the deposition method. Besides developing the methods, the equipment, and the processes for depositing different films of organic semiconductors on OFET templates, the application of various lithographic methods was a second technological challenge which had to be faced before achieving the results. The thesis can roughly be outlined in three parts: first the theoretical considerations, secondly the experimental results and conclusions, and thirdly more process and technology based subjects which will be treated in several appendix chapters.

Part I: The true experimental physics approach is to explain the nature of observations. Sometimes a basic understanding of a problem helps the researcher to know where and how to search for the observation. Maybe therefore theory most of the time comes first. The theoretical part shall give a basic understanding of the physics underlying the organic semiconductors and the OFET device under investigation. It gives the background and information to understand the oncoming topics in the experimental results. More detailed theoretic considerations will additionally be given there in order to explain and conclude the experimental findings.

- The part mainly dealing with theory starts with chapter 2 on the nature of the organic semiconductors. First of all the fundamental properties of organic semiconductors or rather "organic and semiconducting" are described. In the view of some organic semiconductor physicist this is more or less *chemical physics*, although the notion will be used by other scientists in a different context. The chapter continues with the specific properties of the materials under investigation. These are:

- the DB-TTF and DT-TTF, two high mobility derivatives of tetrathiafulvalene molecules, the dibenzene and dithiophene TTF. They are drop-cast deposited resulting in single crystalline structure. Furthermore the vacuum deposited variants will be investigated. The different deposition methods result in a different morphology and structure: a polycrystalline thin film with changed electrical and physical properties.

- the vacuum deposited variant of $\alpha\omega$-dihexylquaterthiophene (DH4T). While the TTFs are rather new types among the organic semiconductors in OFET applications, the thiophene derivatives have been investigated since the beginning of research in OFETs. The DH4T is one of the most interesting candidates among them with respect to structural ordering of films and high mobility. Vacuum deposited, it constitutes nearly perfect two-dimensional ultra-thin polycrystalline films of excellent ordering and thus high quality transport properties. A long experience with the material guarantees a high quality of the analysed films which in terms of mobility challenges the highest reported in literature. For these reasons, DH4T is predestined for investigating the questions concerning the experimental setup or transistor, like scaling aspects, bias stress influences, etc.. In this way the DH4T is the material "workhorse" of the thesis.

- the amorphous polymer semiconductor polytriarylamine (PTAA). The spun-cast polymer thin films cannot equal the transport properties of the vacuum deposited materials above but have different aspects: here, especially regarding manufacturability in lithographic processing.

- The following Chapter 3 applies to transport models of organic semiconductors. In order to continue with the general term choice of *chemical physics* from the previous point: this chapter is on *transport physics*: how do the electrons move or are moved in the material. It makes a comparison between the organic semiconductors and conventional inorganic semiconductors and gives a detailed description of the major transport models relevant for the above materials. The influence of the structural ordering (inter-molecular transport) and the molecules or polymers themselves (intra-molecular transport) in combination are the key influences defining the transport properties. This proves the need for the structural analysis of organic semiconductors in combination with transport measurements, a key driving force for the undertaken investigations. The observation of the transport mechanism by its temperature dependent behaviour will be described which is the basis for the experimental chapter 7 on a temperature dependent transport analysis of the TTFs.

- Chapter 4 is dedicated to the TFT device, indeed it is truly *device physics*. As a surface dominated device, the TFT is governed by its interfaces. These are the metal-insulator-semiconductor interface (the "gate" of the transistor) and the metal-semiconductor interface (the "source and drain contact"). Their theory is briefly explained which helps to continue with a theoretical treatment of the TFT devices' characteristics. This is performed under assumptions of idealisation which as a whole will not only give the reader the possibility to train his comprehension of mathematical equations but also to learn more about the origin of all the essential parameters used to characterise the materials and devices later on.

- The last chapter of this part, no. 5, deals with the hard reality of OFET devices. I would not call it *real physics* but it is to explain the use of the previous chapters findings and its limits if some of the idealising assumptions are no longer valid. These aspects of real devices are first of all the effective extraction of parameters from their characteristics and the effects and models on the characteristics that evolve apart from the idealising assumption, e.g. contact influences and scaling aspects. It is also to give tools for judging the validity of the theory on the characteristics.

With these considerations the basis for the details in the oncoming experimental results chapters is given. In these chapters (Part II) the subjects are taken on again and depending on the requirements that arise will be discussed and specified further. The large number of parameters which influence the organic semiconducting devices and the huge variety of materials have the consequence that the experimental approach for the development of models is chosen most frequently. This procedure is applied in my thesis, too.

Part II: The following five chapters on experimental investigation and interpretation of the transport properties of the before presented materials address different aspects of the

materials and the OFET devices using them as active (semiconducting) layer.

- The first chapter of the part (no. 6) is on optimised basic characteristics of the different materials. They are observed in micrometer channel OTFT devices. The optimised status regards a defined deposition method and the pretreatment of the standard bottom contact TFT templates for a maximum mobility. Furthermore the use of these standard templates (thermally oxidised Si wafers with metal contacts) and the deposition of the organic semiconductor in the terminal step allows a direct comparison of advantages and disadvantages for the investigated materials. The characteristics and resulting material and device parameters are interpreted following the previous part I. Another section of the chapter treats the aspects of ageing and environmental stability of some of the materials.

- Chapter 7 deals with the topic of the transport models (taking on subjects of Chapter 3). It presents the results of temperature dependent transport measurements for the crystalline ordered organic semiconductors DB- and DT-TTF in the temperature regime from 50 K to 400 K. The chapter further consults organic semiconductor transport theory by treating the aspects of band tails and the density of states in organic semiconductors in order to interpret the findings.

- The next chapter (no. 8) describes a very useful and most interesting method of metrology that is implemented in the vacuum deposition setup: the *in situ* electrical characterisation method. This paraphrases the investigation of a vacuum deposited organic semiconductor during its growth on a TFT template and also the analysis of the devices after growth without breaking the vacuum, in this way excluding the many perturbing extrinsic influences on the materials' properties. The method allows the direct monitoring of the influence of the active organic layer thickness, and to compare and correlate between the electrical and structural properties by using the single observations made during the analysis of structure, morphology and transport. Moreover it elucidates the influences of environmental parameters and the treatment after deposition of the OFET device by investigating them in very controlled environment. In our case the topic is the analysis during growth of DH4T and DB-TTF and the investigation of environmental and stress influences on the electrical properties of the OTFTs.

- In chapter 9 the scaling behaviour down to sub 100 nm channel lengths will be treated. The key aspects is to use the scaling behaviour in devices for analysing the materials properties. On the one side the self-organising aspects in organic materials are already defined by the single molecule, on the other hand the thin film itself reacts on downscaling of its environment. The influence of the bulk material may increase when electrical fields change under the variation of the electrode distance, the interfaces will grow in influence, if one reduces space between them, and the size of grains and defects in polycrystalline and crystalline materials give their reactions on changing the scale, just to name three of the aspects. In order to achieve a downscaling of the channel length and the gate insulator thickness, the characteristics of electron beam lithographically processed metal electrodes on SiO_2 templates with different oxide thickness down to 10 nm are analysed. There are different behaviours among the investigated materials which can be explained by the structure and

inherent transport properties of the organic semiconductor. A measure is the ability of the material to subdue short channel effects for reduced channel length. In this context the models for short channel behaviour developed in chapter 5 are applied for experimental evaluation.

- The part's final chapter no. 10 is chosen at this place because it represents the results on a more technology based subject. Therefore it is quite a good bridge to the appendices and is intended to encourage the interested reader not to stop after the following résumé, but to peruse also the last part, dealing with processing and technology based topics. The chapter finishes the experimental part with the description of the manufacturability of the PTAA in conventional lithography processes. The electrical results of the devices manufactured with the developed processes are discussed concerning performance and stability of the material. Therefore this subject should be read in combination with the section in the appendix on the technical process for lithography on organic semiconductors. The PTAA is structured on transistor templates using UV-lithography and lift-off technology or masked O_2-plasma etching. For an application it is crucial that the semiconducting layer can be structured in some way, a standard lithographic method would therefore be most attractive. The main focus lies on the comparison with the standard method of depositing the PTAA film in the final process step on the pretreated template. Additionally the influences of the applied chemistry and processing on the material's properties can be judged.

Concerning the new investigations and interpretations on the materials the conclusion can now be drawn in a detailed résumé. The following appendices bear additional information and interesting new aspects in direct connection to the until then presented models and results.

Part III: As stated above the appendices are dedicated to technological aspects, processing procedures and equipment. The chapters will focus on the context with the results of the experimental part. Exceptions are the alternative methods for fabricating submicrometer channel TFTs which bear some new experimental results not treated before. The following list gives the overview:

- Part A describes the organic molecular beam deposition method and setup. This is essential for the chapter on *in situ* investigation methods and for understanding the origin of the different polycrystalline variants of vacuum deposited organic semiconductors.

- Part B comments on the applied soft lithographic method and processes. The standard UV-lithography and the more sophisticated electron beam lithography methods are described. They are applied to manufacture micrometer and nanometer channel TFTs. A second section is on alternative methods for generating sub micrometer channels: an angular shadow evaporation of metal contacts and microcontact printing (publication [6]). The last section of Part B is the technological background to the experimental chapter on lithography on PTAA.

- Part C is about the applied pretreatment methods for the SiO_2 surface prior to the deposition of the organic semiconductor.
- Part D presents an atomic force microscope analysis of the growth mechanism in vacuum deposited DB-TTF. This study is an example for the optimisation of the growth conditions using structural analysis method in combination with electrical transport results on the evaporated thin films.

Chapter 2

Organic semiconductor materials

This chapter is dedicated to the essentials of organic semiconductor materials. It will give an overview of the fundamental transport properties of these materials with focus on the most interesting physical values for OFET applications. Besides this, the chapter will especially treat the materials investigated in this work.

Organic semiconductors are carbon-based chemical compounds that exhibit semiconducting properties. There are several definitions of a semiconductor depending on the textbook. The most common are, on the one hand, the definition based on the material-specific conductivity [7], where one important feature of a semiconductor is that it can cover a wide range of conductivity, from 10^{-8} to 10^{3} S/cm (resistivity from 10^{-3} and 10^{8} Ω·cm). This depends on the doping concentration (influence of built-in impurities) in the semiconductor. On the other hand, a semiconductor is defined using the energy between valence and conduction band from band theory. Here, the semiconductor can be characterised as an "insulator-like" material with a sufficiently small band gap (between 0.1 eV and 4 eV, at room temperature). While in this chapter the focus will be on the origin of electrical transport in molecules and between them (intra- and intermolecular transport), the following chapter is dedicated to the transport physics including a discussion of the band model. Thus at this place the electronic properties will be mentioned but not further discussed.

2.1 Fundamental transport properties

Molecular orbitals, which are the origin of electrical transport in molecules, are formed by the overlap of the atomic orbitals theoretically using transfer and overlapping integral. The coupling within a molecule is mostly covalent-like, which means based on the sharing of electrons between neighbouring atoms. The important role concerning transport comes

from the type of chemical bonding. In carbon atoms σ-bonds are formed by the coupling of sp_2-hybrid orbitals (the resulting hybridisation of p_x- and p_y-orbitals in plane). Fig. 2.1 demonstrates the formation of molecular orbitals exemplified by the benzene molecule. In

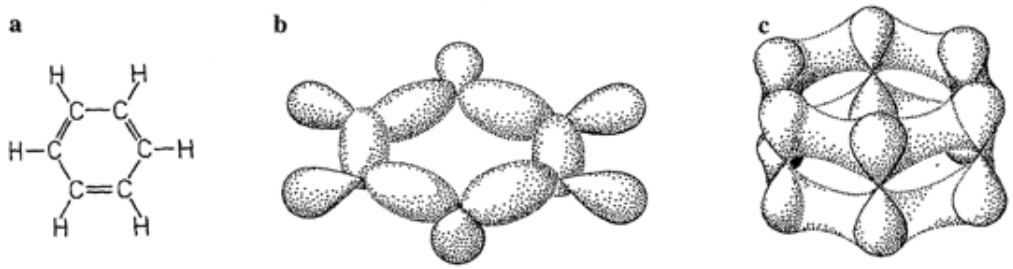


Figure 2.1: *Formation of molecular orbitals in benzene. a) Structural formula, b) σ bonds, c) π bonds (from [8]).*

part b it shows the resulting σ-bonds by the coupling of sp_2-hybrid orbitals of neighbouring C atoms and C sp_2-hybrid orbitals with a hydrogen $1s$-orbitals. σ-bonds are strongly localised and the electrons therein have high excitation energies. Therefore, they do not contribute to the transport within and between molecules. Here, the π-orbitals displayed in part c, which are formed by the overlap of the carbon $2p_z$-orbitals, play the important role. They are energetically weak in comparison to the σ-bonds. In these aromatic systems the π-orbitals form a delocalised π-electron system. This coupled system forms the molecular orbital which is responsible for the intramolecular transport. Using the Hückel theory [9] the discrete energy levels of the π-electrons can be calculated: they are the molecular orbitals of the molecule. The occupation of the orbitals is governed by the Pauli-principle. The highest occupied molecular orbital in the ground state is called HOMO, the lowest unoccupied molecular orbital LUMO. The energy difference of HOMO and LUMO defines the electronic properties of the molecule. The molecules and polymers used in this work are all formed by different aromatic systems and can be described by the molecular orbital theory. The decisive step for their properties in films or more generally in devices is defined by the intermolecular transport properties and thus strongly depending on the formation of the organic solid. In contrast to the rather uniform molecular theory the formation of organic solids is a complex system which results in a wide variety of conductivity models.

Organic solids are mainly formed by *Van der Waals* bonding. The cohesion is based on weak electron dipole forces between the neutral molecules. The weak bonding distinguishes the organic semiconductors from the covalently bonded inorganic semiconductors. The formation of a crystal by weak van der Waals forces has the advantage of a moderate energy needed in the crystallisation process [10]. This simplifies the formation of single crystals of these materials compared to the covalently bonded materials (e.g. the inorganic semiconductors). From the energetic point of view the interaction forces in van der Waals bound crystals are less than 42 kJ/mol, whereas the energies in Si are as high as 318 kJ/mol [11]. The Boltzmann factor exp(-hν/k$_B$T) for the thermal occupation of phonon states in the crystals amounts to 0.57 and 0.11 for a typical organic molecular crystal and Si, respectively, both at room temperature. The factor plays a decisive role in many solid-state

properties and reflects the intermolecular forces in both crystals [8]. This physical background of the solid, however, also affects the electronic properties theoretically predicting a mobility limit for organic semiconductors in the order of 10 cm^2/Vs [12]. The value in Si or Ge is a factor 100 times higher. Further aspects like the localisation/delocalisation of charge carriers and the relevant transport models are discussed in the next chapter.

In the following two sections the two main families of organic semiconductors, the small molecules or oligomers and the polymers will be discussed including the consequences of different morphologies which depend on their chemical properties, growth, and processing. The largest part of the results is dedicated to the $\alpha\alpha'$–dihexylquaterthiophene as representative for small molecule material in OFETs. It is a thiophene based molecule which is vacuum deposited in thin ($\sim$ 10 nm) polycrystalline films in this work. Representing another family of oligomer materials two derivatives of tetrathiafulvalenes are investigated. Here, two different types of morphologies are achieved by different deposition methods and will be compared. If they are solution processed, the deposition will result in single crystal morphology of the material and if vacuum deposited, in thin polycrystalline films. In addition these materials are compared with polytriarylamine, a polymer semiconductor, which is spin-cast from solution forming an amorphous layer.

2.2 Small molecules and oligomers

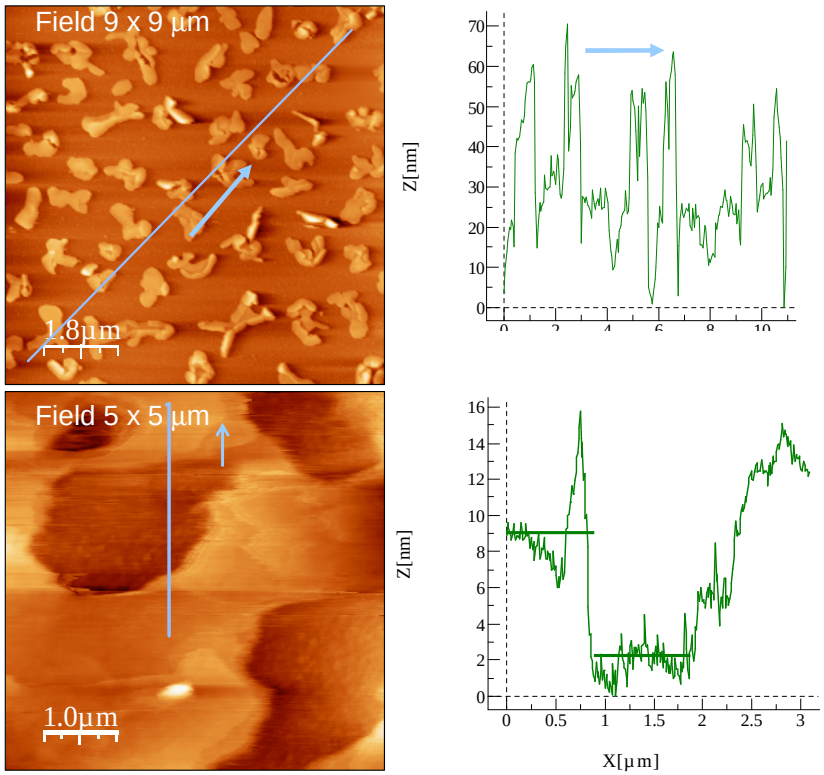


Figure 2.2: *AFM images with coverage profile along the denoted line of vacuum evaporated thin films of DB-TTF (top) and DH4T (bottom) both on OTS-treated SiO_2 substrate. DB-TTF exhibits a three-dimensional growth of islands, whereas the DH4T nearly grows layer by layer. The average layer thickness (material deposited in an ideal two-dimensional growth mode, cf. appendices A and D) is approx. 10 nm in both cases.*

Small molecules of organic semiconductors are distinguished by their chemical structure, for polymers only the monomer is defined by the chemical structure, the size of chains will vary. Therefore, the small molecules are good candidates for self-organisation and formation of ordered morphologies. Polymers form poly-crystalline or amorphous layers. The connection between long-range intermolecular order and transport properties is the reason why the highest mobility values in organic semiconductors are measured on purified small molecule material like pentacene or rubrene [13, 14]. A disadvantage results from the high expenses for scaling up in a production process and purification. Additionally, highly ordered morphology comes with an elaborate technical setup. However the small molecules used in applications, as e.g. the organic field-effect transistor, are the ideal test bed for physical research. This is also the case with respect to the oligomer approach where purified oligomer materials, tailored for a certain application, are used for characterisation of intrinsic material properties in order to investigate their nonuniform polymer variant via extrapolation of the electrochemical and physical properties [15]. Another argument for the use of small molecules in organic electronic applications is their relatively good accessibility by theoretical methods. This simplifies the design of molecules for special applications. In fig. 2.3 different field-effect transistors with active layers of organic

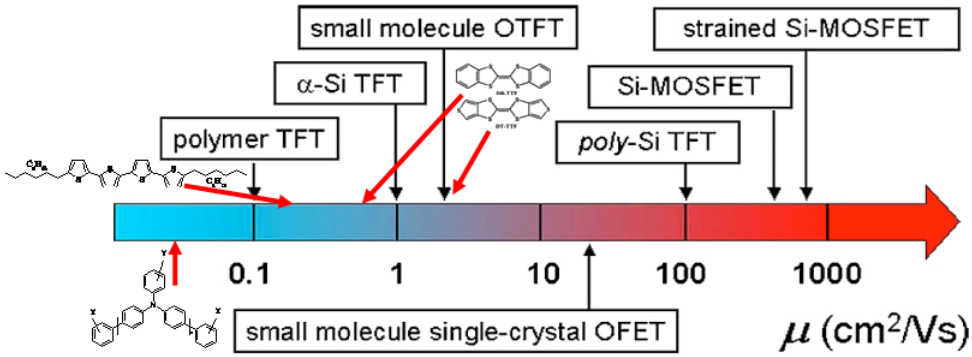


Figure 2.3: *Maximum mobility values of field-effect transistors with respect to their active layer material (different organic and inorganic types of semiconductors) on a logarithmic scale (from [16]). Furthermore, the corresponding value for the organic semiconductors (denoted by their structural formulae) underlying this work are presented.*

and inorganic compounds are classified by their maximum order of magnitude in mobility. Moreover, the maximum investigated mobility values of the organic semiconductors in this thesis, denoted by the structural formulae of the materials, is monitored. The small molecules investigated in the experimental part are two derivatives of tetrathiafulvalenes, the dibenzene and dithiophene-tetrathiafulvalene (DB-TTF and DT-TTF, respectively) and the $\alpha\alpha$'-dihexylquaterthiophene (DH4T). They rank in the range between 0.1 cm^2/Vs and 10 cm^2/Vs. The obtained maximum mobility depends on the deposition method, which defines the long-range order of the molecules. These values are in the order of the maximum reported for the materials or better, to the best of our knowledge.

2.2.1 Tetrathiafulvalenes

Recently, tetrathiafulvalenes derivatives (TTFs) have been introduced as candidates for application and analysis of organic electronic devices [17, 18, 19, 20, 21]. From the above introduction in MO theory it follows that the $\pi\pi$-stacking between next neighbour molecules defines the intermolecular transport. The illustration of the planar benzene molecule in fig. 2.1 has shown that in this case the favoured direction for transport is orthogonal to the molecule plane. The tetrathiafulvalene is planar also. Additionally to a crystallisation, strongly governed by the $\pi\pi$-stacking, the built-in sulphur atoms are beneficial for transport, because of the resulting attractive S-S interaction [22]. The latter results in an even larger overlap of neighbouring π-bonds in the organic crystals of the material.

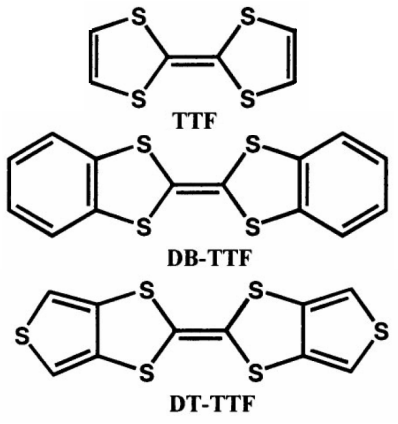


Figure 2.4: *From top to bottom: structural formulae of tetrathiafulvalene, dibenzene- and dithiophene-tetrathiafulvalene.*

TTFs have been used in charge transfer salts from the beginning of organic conductors research in the early 1970s [23]. The tetrathiafulvalene-tetracyanoquinodimethane (TTF:TCNQ) can be considered a prototype compound in this interesting class of two-component materials with anionic and cationic species. The TTF acts as the electron donor and exchanges π-electrons with the acceptor TCNQ. TTF compounds are known for their transport properties ranging from insulating through semiconducting to metallic and superconducting [24]. Our focus is on the compounds of fig. 2.4, the dibenzene- and dithiophene-tetrathiafulvalene (DB- and DT-TTF, respectively). The attachment of two benzene or thiophene, respectively, aromatic rings at the TTF structure sides results in a symmetric, completely conjugated and planar molecule. The advantages are, on the one hand, a reduction of the donor abilities of TTF which increases the stability concerning oxidation [19]. On the other hand, the $\pi\pi$-stacking is further increased resulting in a higher charge carrier mobility [19, 20, 25]. In the case of DT-TTF a mobility value of 3.6 cm^2/Vs is achieved, presented in the experimental part (see also [26]). The DB-TTF exhibits a slightly reduced mobility of up to 1 cm^2/Vs. This hierarchy within the two derivatives is in agreement with reported increased $\pi\pi$-stacking due to the S-S interaction of neighbouring sulphur atoms in the thiophene side rings [25].

The synthesis of both materials as performed by collaborating partners is described in literature [27, 28]. The encouraging mobility results increase in appreciation because they are achieved using a drop-cast from solution method [21, 25] (cf. chapter 6). The morphology is single crystalline. Organic single crystal results of high mobility are generally achieved using growth from vapour phase or melt in long and complex experiments [14, 29]. An optical micrograph of DB- and DT-TTF single crystals are presented in fig.

6.1. The crystallographic characterisation [21] of the single crystalline DB-TTF confirms

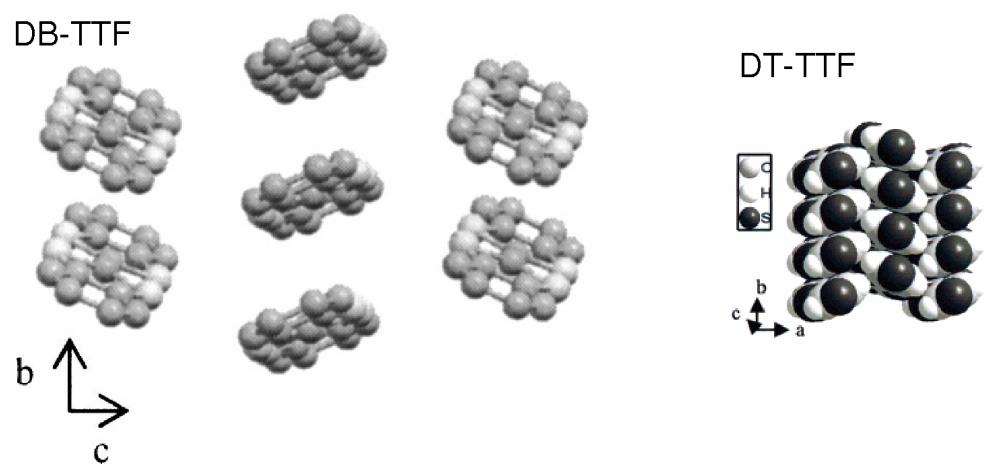


Figure 2.5: *Crystalline structure of dibenzene- and dithiophene-tetrathiafulvalene (from [20, 25, 21]).*

a herringbone structure as shown in fig. 2.5 (left). The planar distance in b-direction is 3.948 Å. The HOMO and LUMO level for the isolated molecule were calculated by DF using Gaussian03 with basis B3LYP/6-31G(d,p). They result in 4.88 eV and 1.02 eV for HOMO and LUMO energy, respectively. For DT-TTF a comparable herringbone structure is reported (fig. 2.5 (right)). The sulphur atoms of the substituents additionally induce a higher interaction between molecular layers in b-direction. The planar distance is 3.65 Å, the herringbone angle is 54°. Our calculations (same method as above) result in a HOMO and LUMO level of 5.12 eV and 1.06 eV, respectively. The DF calculations for the HOMO-levels exactly match the published values [21] of DB-TTF and vary by less than 0.2 eV for DT-TTF (4.94 eV).

In this work the properties of vacuum evaporated films are analysed and compared with the single crystalline ones, which is a novel aspect of the investigation of DB-TTF and DT-TTF. Moreover, in the case of DB-TTF an extensive AFM analysis of its growth mode on SiO_2-substrate and noble metal electrodes was performed in the sample temperature range between room temperature and desorption temperature ($\sim$ 105°C at 10^{-9} mbar) under variation of the molecular flux. The resulting morphology is different from the several 100 μm large single crystals, grown by drop-casting from solution. The AFM results are presented in appendix D. Experiments on DT-TTF suggest a comparable growth behaviour. The top image of fig. 2.2 shows the AFM-image of a grown layer of DB-TTF on octadecyltrichlorosilane(OTS)-treated SiO_2 in comparison to a thin evaporated film of DH4T. Nominally, the same average thickness (material deposited in an ideal two-dimensional growth mode) of the two materials is deposited. Contrary to DH4T the growth mode is obviously three-dimensional in large islands with a large height distribution, whereas DH4T grows in terraces in a nearly ideal *Franck–van der Merwe* layer by layer growth mode (see the following section). The behaviour of evaporated DT-TTF is

comparable to DB-TTF. Thus, the resulting electrical properties of evaporated TTFs will be largely influenced by polycrystalline effects. X-ray and Raman analysis on the evaporated films also suggest a crystalline structure different from the drop cast grown crystals [21, 30].

2.2.2 Dihexylquaterthiophene

Thiophenes (fig. 2.6) are besides the acenes the most extensively investigated chemical compounds in the field of organic semiconductors [11, 31].

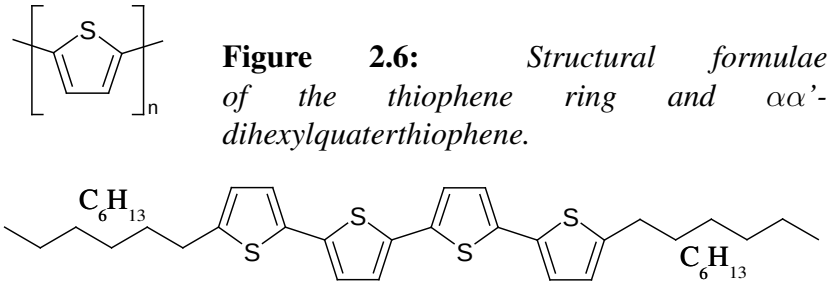


Figure 2.6: *Structural formulae of the thiophene ring and $\alpha\alpha$'-dihexylquaterthiophene.*

This is due to the combination of aromatic rings, the increased stacking of nearest neighbouring molecules which in the thiophenes is also due to the sulphur, and the rigid rod-like assembly of in principle all pure oligomers. A complete overview of thiophene oligomer and polymers also with respect to applications in electronic and opto-electronic devices is given in [32].

DH4T plays a prominent role among the thiophenes and has proved high electric transport performance in organic field-effect transistors [33, 34]. It combines the semiconducting quaterthiophene (4T) core with symmetric hexyl endings that fulfil two tasks [35]. On the one hand, they enable the solubility of the molecules in various solvents [34] and, on the other hand, they induce a much higher long-range ordering of the molecules [36]. In comparison with quaterthiophene the reported highest mobilities in evaporated DH4T thin films are improved by a factor of 100. The values are 0.23 cm^2/Vs and in the order of 10^{-3} cm^2 for DH4T and 4T, respectively [33, 37]. DH4T has a liquid crystalline structure. Differential Scanning calorimetry (DSC) has proved a phase transition to a smectic - two dimensional - phase above 84°C [34] and elsewhere at 81°C [38]. The latter reports a hysteresis of range 20 K of the phase transition so that the back transition from 2D (higher T) to 3D occurs at 61°C. This is confirmed in electrical transport data [38, 39]. The vendor DSC scan of the investigated stack of DH4T confirms a phase transition at about 84°C and a melting point above 180°C.
The growth of thin DH4T films above the transition temperature induces a long-range ordering of crystalline regions in the order of 10 μm to 100 μm [36] remaining after cooling the layers back to room temperature. The growth mode on OTS-treated (cf. appendix B) SiO_2 wafers is two-dimensional. The AFM image in fig. 2.2 (bottom) shows the terrace-like morphology of a 10 nm thick film of DH4T in a 10 nm thick film on OTS-treated SiO_2. The above denoted size of grains in such a film is confirmed in the optical micrographs of fig. 6.7 by a differential interference contrast method in the case of a 90°C substrate temperature growth. The growth at a temperature below the phase transition point (70°C) results in clearly reduced grain size.

The molecules arrange in a herringbone structure along their long axis. A detailed crystal structure analysis can be found in literature [33, 34]. From the crystalline parameters the height (in z-direction) of a single layer is 28 Å at the low temperature (room temperature) phase. This thickness is used for the calibration of the micro balance in the UHV deposition chamber. By Gaussian quantumchemical calculations (Gaussian98, B3LYP/6-31G(d)) and using the molecular structure published in [40] the HOMO and LUMO level for a single molecule were calculated to 4.7 and 1.6 eV, respectively.

The occurrence of the reproducible standard mobility values in the order of 0.1 cm^2/Vs since the late 1990s results from a well established matured preparation procedure of the thin films. Therefore, DH4T has developed as the standard material for device and setup optimisation. It is used in terms of comparison with new material, influence of device specifications and investigations of extrinsic influences (cf. chapters 6 - 9).

2.3 Amorphous Polymers

A polymer is a chemical compound constituted by the repetition of a component, the monomer. These monomers are molecules (macromolecules) which string in a long chain. They form the basis of the majority of plastics. An advantage compared to single molecules is that the fabrication of polymers is better accessible for industrial production. The discovery of conducting polymers is a relatively recent phenomenon [41], which yielded the *Nobel price in chemistry* in 2000 for *Heeger, MacDiarmid and Shirakawa* [2]. It opened a huge and important new field to physics and chemistry, and to technology in general. The π-conjugated polymers are candidates for both conducting and semiconducting properties. A summary of relevant literature is documented in [42].

Among the π-conjugated semiconducting polymers there are crystalline polymers, which develop an ordered structure due to chain to chain interactions. This favours the interchain transport and therefore an increased performance regarding the electrical transport. These high mobility polymers build crystalline films. The polytriarylamine (fig. 2.7) is an amorphous polymer which has the advantage of very good solution processability and no conductance anisotropy.

2.3.1 Polytriarylamine

Polytriarylamines (PTAA) are interesting candidates for polymer electronic applications because they have proved to be very stable during processing and in devices, especially processing in air. They are highly soluble and enable very homogeneous and stable spin-cast films and applications using different printing techniques. These features make them very interesting for a printing deposition procedure of semiconductors [43, 44]. Further-

more a newly developed lithography processing of PTAA films will be demonstrated in chapter 10 which is possible due to the resulting homogeneous and robust spin-cast films. Additionally to these application aspects, the advantage of an amorphous semiconducting layer is that the material's characterisation is easier, because morphological effects can essentially be neglected [45, 46].

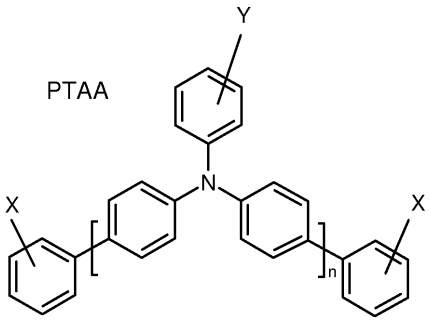


Figure 2.7: *Structural formula of polytriarylamine (PTAA).*

In this way the analysis of PTAA based devices is very useful in order to circumvent morphological effects on the device performance. Transport properties in amorphous films are generally lower due to the reduce intermolecular/chain stacking. In PTAA a mobility in the order of 10^{-3} cm^2/Vs is achieved for thin films , the bulk limit investigated by the *time of flight* method is denoted as 1.26 10^{-3} cm^2/Vs [45]. The synthesis of PTAA is patented in [47]. The PTAA-based results in this thesis employ the polymer (see fig. 2.7 for the structural formula.) in a 1 vol% toluene solution.

Chapter 3

Transport models

The following two chapters give an overview of theoretical work on the transport properties of organic thin film transistors. The large variety of organic semiconductors and the different influences from device interfaces and materials prevent from giving a uniform theory. In this chapter the major concepts of charge carrier transport which allow to describe the different types of organic semiconductors will be addressed. The focus will be on models relevant for the materials and device specification used in the present work.

First this chapter will bring the reader's attention to general transport behaviour in semiconductors and continue with models for delocalised and localised charge transport. Some of these models are known from conventional inorganic semiconductor physics and will be interpreted in their meaning for the organic semiconductors. A discussion of the different concepts of charge carrier transport relevant for the materials presented in chapter 2 will be made. Furthermore the chapter will point out the connection between the morphology of the semiconducting layer and the transport model applicable for the material.

3.1 Basic considerations on electronic transport

The large variety of organic semiconductors and their deposition methods results in a wide spread description of transport in these materials going from delocalised electrical transport models to pure localised ones.

In semiconductor physics, charge carriers are electrons (negative charge e) and defect-electrons (positive charge p) so-called holes. Driven by an external electrical field E, they move in the material with a certain drift velocity v. This velocity is an effect of the acceleration due to the field as well as the retarding of the charge carriers by scattering processes in the solid state body. The mobility describes the proportionality factor between the charge

carrier's drift velocity and the applied electrical field.

$$v = \mu \cdot E \tag{3.1}$$

This microscopic definition of μ is uniform and its value only depends on material specific properties. The mobility is essential for the application of semiconductors in devices and the description of charge transport in a specific semiconductor.
In the same way as the mobility the specific conductivity σ of a semiconductor describes the proportionality factor between the induced current density j and the applied electrical field.

$$j = \sigma \cdot E \tag{3.2}$$

In other words, it gives a value for the current that passes through the device by an applied voltage. In the case of a unipolar charge transport, which is the case in the systems investigated in this work, mobility and specific conductance are connected as

$$\sigma = en\mu \tag{3.3}$$

here e is the elementary charge and n the density of charge carriers. Although the case of ambipolar transport in semiconductors is not subject to this work, for the sake of completeness, the basic concept there has to be extended to

$$\sigma = e(n_e\mu_e + n_p\mu_p)$$

where e/p denotes the type of charge carrier (n for electrons, p for holes). In this way the contribution of it will result in an addition of the conductance of electrons and holes if both types of charge carrier contribute to transport.

In a field-effect transistor the density of charge carriers is determined by the applied gate voltage (cf. 4.3), thus with eq. (3.2) and (3.3) the mobility and the electrical field resulting from the channel voltage define the current through the device at a constant gate-source voltage. This implies the meaning of the mobility in applications, where generally one operation voltage over the transistor channel and two constant gate voltages define the on- and off-state of a logic and the mobility is the decisive parameter for any dynamical process. The combination of p- and n-type field-effect transistors is the basic concept in the so-called *complementary metal-oxide-semiconductor (CMOS) technology*. Therefore, the ambipolar transport is attracting increasing interest in the field of organic semiconductors [48].

In the present case the mobility μ of p-type organic semiconductors will be the major physical parameter discussed. Thus, the explanation of transport models below will be in a unipolar semiconductor with respect to the behaviour of mobility.

3.2 Band–like transport

The band model is most common in inorganic semiconductor physics. The basic idea is that the atomic orbitals overlap in an ordered crystalline formation of the semiconductor. Under

the condition of the *Born-Oppenheimer-Approximation* [49] which describes the solid state as a rigid, 3-dimensional system of building blocks and the *One-Electron-Approximation* where an electron behaves independently from other electrons, energetic bands over the whole solid state are formed and a delocalised transport of the charge carriers in these bands is allowed. The band model is discussed in every textbook introducing into the field of solid state physics. For such a detailed description it is refered to [50] or [51].

The electronic band model implies that free charge carriers can move with a certain effective mass along the solid state instead of being bound to an ion. They are in the conduction band (electrons) and/or in the valence band (holes) (cf. fig. 3.1). For a conducting material valence and conduction bands overlap (fig. 3.1a) or as in the case of Sodium have half filled valence bands (fig. 3.1b). In both cases free charge carriers exist. A semiconductor has a band gap (< 4 eV) which means that free charge carriers can only exist by energetic excitation or doping (intrinsic or extrinsic semiconductor, fig. 3.1c and d). Doping is the introduction of charge carriers by impurities in the semiconductor. These impurities form a doping level near the conduction (n-type) or valence (p-type) band. Already at a very low thermal energy (≈ 10 meV) this allows the formation of free charge carriers in the bands. Insulators are defined in this model by a larger energy gap (> 4 eV).

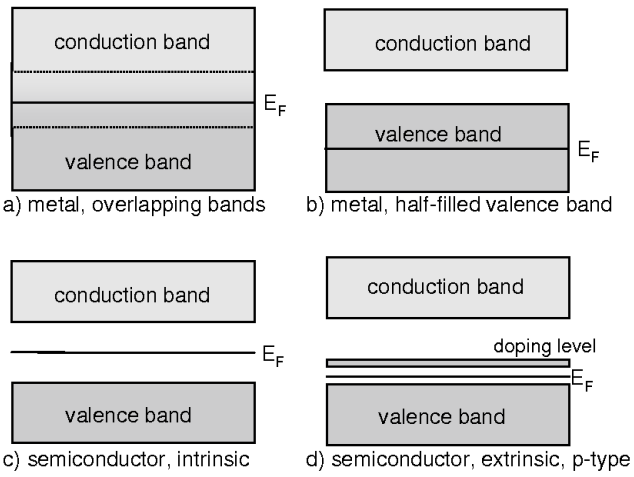


Figure 3.1: *Schematic of band structures of metals a), b) and semiconductors c) intrinsic, d) extrinsic and p-type.*

The *Fermi level* E_F is a term from *Fermi-Dirac-statistics* that describes the maximum energy of an electron of the material at 0 K. The excitation of charge carriers at temperatures above 0 K is described by the *Fermi-Dirac-distribution* of the *Fermi function* f(E):

$$f(E) = \frac{1}{exp((E - E_F)/k_B T) + 1} \tag{3.4}$$

with k_B the Boltzmann constant. In other contexts E_F is referred to as the electron chemical potential, which has the more general definition from *Gibb's fundamental equation* in thermodynamics [52].

In a metal E_F is directly related to the density of charge carriers n

$$E_F = \left(\frac{(hc)^2}{8mc^2}\right)\left(\frac{3}{\pi}\right)^{2/3} n^{2/3} \tag{3.5}$$

with h the Planck constant, c the velocity of light, and m the electron mass. In a semiconductor, doping shifts E_F towards the conduction (n-type) or valence (p-type) band, where E_F, following its definition, is inbetween the band and the doping level.

Following the band model, the charge transport is limited by microscopic perturbations of the charge carriers during their way through the material (crystalline or not), which are lattice vibrations and crystalline imperfections and/or impurities. The temperature dependence of the mobility μ in these systems depends on the scattering mechanism relevant for the given temperature regime.

In the following, the focus will be on transport in semiconductors of different morphology. In a crystalline semiconductor lattice vibrations (phonons) are one major limitation of transport. The perturbations by acoustic phonons increase with increasing temperature and increasing effective mass m^* and the mobility is decreased. Following [53] it is

$$\mu_l \sim (m^*)^{-5/2} \times T^{-3/2}.$$

In addition, the built in impurities (by controlled or unintentional doping) take effect on transport over the whole temperature range. The higher the temperature the lower is their effect on the charge carriers. For ionic impurities the behaviour is [54]

$$\mu_i \sim (m^*)^{-1/2} \times N_I^{-1} \times T^{3/2}.$$

Thus, a reduced mobility results for higher effective mass and increased density of impurities. However, contrary to the lattice phonon effects, the mobility increases with the increasing temperature. The mobility including both mechanisms above results by the Matthiesen rule [55]

$$\mu = \left(\frac{1}{\mu_l} + \frac{1}{\mu_i} \right)^{-1}. \tag{3.6}$$

The idealised temperature dependence of the mobility deduced from band theory is presented in fig. 3.4. In the low temperature regime, where there are reduced phononic effects, the mobility increases with increasing temperature. At a certain temperature, where the phononic effect predominates, this behaviour is inverted and the mobility will decrease with increasing temperature. The high temperature behaviour should follow

$$\mu \sim T^{-n} \tag{3.7}$$

where the exponent n ideally should approximate $3/2$. The effective mass of the charge carriers and the purity of the material thereby define the temperature above for this purely phononic character of the mobility temperature dependence. Experimental results for inorganic materials (Si, Ge or GaAs), however, vary between 1 and 5/2 because of other scattering mechanisms [55].

A band model transport in organic semiconductors is questionable [29, 56]. The main arguments are that in band theory the width of the bands depends on the binding energy in the crystal. A weaker binding energy means narrower bands and higher effective masses of electrons and holes. Calculations of bands in acene molecular crystals result in a mean-free path of the carriers shorter than the intermolecular distance [56]. This is crucial for crystalline organic semiconductors where the small van-der-Waals type binding energies (tenth of meV) result in narrow bands and reduced mobility μ compared to Si or Ge crystals [12].

However, recently a band transport (following eq. (3.7)) is reported in the field of ultra pure organic single crystal materials. An increasing mobility with decreasing temperature was found at least in a limited temperature range [57, 58] (rubrene), [13] (pentacene), and [59] (naphtalene and perylene). This is explained by effects of phonon interaction in the ultrapure organic crystal. Here, the pentacene, naphtalene and perylene results are determined in the bulk material by measuring the mobility with either time-of-flight (TOF) or *space-charge-limited-current* (SCLC) methods. The rubrene results are taken from OFET devices with special care on a pristine organic crystal surface (by use of a vacuum gap between crystal surface and gate contact [60]). Following their argumentation, the observation of band transport with interface dominated devices like the OFET is difficult, because a trap dominated transport (cf. 3.2.1) is almost certain. In [57] a value of the density of shallow traps n_{tr}^{sh} of 10^{10} cm^{-2} is calculated for rubrene and noted a borderline for the untrapped band transport. In the above experiments the band–like temperature behaviour of the mobility is characterised by an exponent n from equation (3.7) of 2.4 for pentacene [13], 2 for rubrene [58], and 2–2.9 for naphtalene and perylene [59]. The origin of these values above the predicted 3/2 is still under discussion [16].

3.2.1 Trapping and release

As mentioned above, the examples for band–like behaviour of the mobility vs. temperature plot are based on extremely pure materials and device interfaces. Especially the latter point is not fulfilled for the common OFET devices. Interfacial states contribute in large amount to the density of localised electronic states, so called trap states (cf. 3.4). Depending on their energy they take influence on the transport. Thus, in the more general case (especially in those organic single crystals of tetrathiafulvalenes, which will be treated more closely in chapter 7) a thermally activated transport is investigated. This can be explained by a trapping and release mechanism (MTR).

The MTR is a model for delocalised transport of charge carriers in bands that interact with localised states in the gap by trapping and thermal release. The concept of trapping and release was introduced in the beginning of semiconductor physics when the structure sensitive property of the lifetime of charge carriers, injected into the semiconductor was found [61][62][63]. In their work from 1953 Shockley and Read [64] follow the idea of traps states of energy in the semiconductor's gap that capture and release charge carriers with defined time constants τ_c and τ_r of the processes, respectively.

$$\frac{\tau_c}{\tau_r} = \frac{n_c}{n_t} exp(-E_t/k_B T) \tag{3.8}$$

where n_c is the density of charge carriers in the band of interest, n_t is the density of traps, E_t the energy difference between the trap and the carrier band edge, and k_B is the Boltzmann constant. Thus, the time constants depend on the trap energy and density. For the capture process a material specific cross section σ_c can be computed with the thermal velocity v of the charge carriers [65]

$$\sigma_c = 1/n_t \tau_c v.$$

A calculation for the reduced effective mobility following the concept of multiple (shallow) trapping and release results in [66]:

$$\mu_{eff} = \mu_0 \cdot \frac{\tau_c}{\tau_r + \tau_c}, \tag{3.9}$$

here μ_0 is the intrinsic microscopic mobility. At low temperature where $\tau_c \ll \tau_r$, μ_{eff} would vary as $exp(-1/T)$. When τ_c approaches or passes τ_r with increasing temperature μ_{eff} approaches μ_0 and for a given energy E_t the trap concentration n_t is the relevant parameter. A combining of the two equations (3.8) and (3.9) above results in

$$\mu_{eff} = \mu_0 \cdot \left(1 + \frac{n_t}{n_c} exp(E_t/k_B T)\right)^{-1}. \tag{3.10}$$

Assuming a temperature independent μ_0, the mobility increases exponentially with a saturation at the value of μ_0 at high temperatures. A phonon influence effects in a reduction of μ_0 for higher temperature. This temperature dependence can be expressed by [67]

$$\mu_0(T) \propto (300K/T)^{1.5}.$$

The latter leads to a similar behaviour as predicted in band theory with a transition from (in this case exponential) increase to decrease characterised by a temperature of maximum mobility. In this context, it implies that the lower the trap density n_t is the lower the temperature for the transition is. This is known as the *Hoesterey and Letson model* of trapping an release [65]. According to the latter consideration the trap concentration in the semiconductor can be evaluated by the temperature dependence of the mobility. In [67] it was successfully applied to the temperature dependence of the bulk mobility in tetracene single crystals. Both situations above are displayed in fig. 3.4.

Le Comber and Spears [68] describe the transport in thin-film transistors with semiconducting layers of amorphous silicon (a-Si) by the multiple trapping and release model. The organic semiconductors directly challenge this material (and polycrystalline silicon) for applications in products. As the macroscopic devices have a common principle, many of the describing models for organic semiconductors are originally from the field of these low-temperature silicon materials. It follows a trap-controlled drift mobility

$$\mu_D(T) = \mu_0 \alpha exp(-E_a/k_B T), \tag{3.11}$$

where μ_0 is the mobility of carriers without any trapping effects, E_a the trap-level energy, k_B the Boltzmann constant and α is a dimensionless factor that depends on the energetic trap distribution (e.g. for a single trap level: $\alpha = n_0/n_T$ where n_0 denotes the density of states (DOS) at the band edge and n_T the density of traps). Le Comber and Spears also argue that equation (3.11) retains for a linear or uniform energy distribution of trap states. Then, E_a is the maximum trap energy and α depends on the distribution, e.g. for a linearly decreasing density of states into the gap $\alpha = E_a/k_B T$. The behaviour for a temperature independent α and a temperature dependence as above are presented in fig. 3.4.

Horowitz et al introduced the model to the field of OFETs [69, 70]. In chapter 7 of the experimental part the transport will be mainly described by trapping and release. Especially we will address more specifically to the crucial point of determining the density of states in the gap of organic semiconductors.

3.3 Hopping transport

Pioneering work in the description of hopping transport in semiconductors was done in the late sixties/early seventies by N. F. Mott and E. A. Davis [71, 72, 73]. Therein, the transport mechanism in amorphous inorganic semiconductors is described. In these systems the electronic structure strongly depends on the degree of disorder. In [74] the band model concept of valence and conduction band with a forbidden gap is modified by the assumption of mobility edges between band and Fermi level and localised states distributed in the gap (cf. fig. 3.2). Different processes contribute to transport (consideration for electrons): (i) extended state conduction above the mobility edge, (ii) hopping conduction in localised states below the mobility edge, where both mobility and carrier concentration are activated, and (iii) hopping conduction in localised states at the Fermi level where the statistics are degenerate.

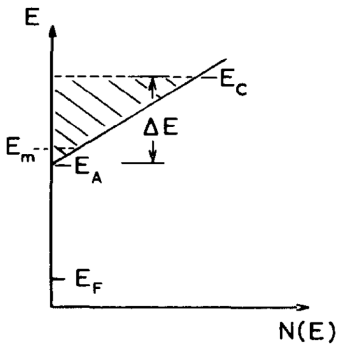


Figure 3.2: *Schematic of the energetic situation in an amorphous inorganic semiconductor, energy versus density of states. There are localised states (shaded region) under E_c. The conduction occurs in a small energy range near the mobility edge E_m (from [74]).*

Charge carriers are trapped in the localised states near E_m where transport occurs by *variable range hopping* (VRH). At the Fermi level there is a finite density of states $N(E_F)$. The difference to the situation underlying the MTR-model is that in the VRH-model a release of trapped charge carriers to the conduction (electrons) or valence band (holes) is most unlikely. Transport only occurs through a pure hopping of variable range between the localised states inbetween E_m and the Fermi level. In the simplest case of a constant density of states (fig. 3.2: the energy range of states involved around E_m is small) the hopping probability ν of a charge carrier from one localised state around a mobility edge E_m (far away from the Fermi energy E_F) to another can be written as

$$\nu = \nu_{ph} exp(-2\alpha r) exp(-\omega / k_B T)$$

where r and ω are the variable (with T) average hopping length and average hopping energy, respectively. α is a tunnelling factor and ν_{ph} a parameter related to the phonon frequency. Under the assumption of a mobility proportional to ν it will vary with T as [74]

$$ln\mu = A - BT^{-(n+1)/4}. \tag{3.12}$$

n describes the dimension of the slope of the density of states and A and B are variables including a combination of parameters. The 4 results from three-dimensional hopping and can be replaced by $d + 1$ where d denotes the dimension. In Mott's model [71] a constant

density of states is assumed and in the case of a two-dimensional transport as in transistor devices it follows [75]

$$\mu_{hop} = \mu_0 \cdot exp\left(\frac{T_0}{T}\right)^{-1/3}. \tag{3.13}$$

Further on in Mott's model [73] the general form of the temperature-dependent conductivity σ is described as

$$\sigma = \sigma_0 exp[-(\frac{T_0}{T})^{\frac{1}{d+1}}] \tag{3.14}$$

where d is the dimensionality, thus, for three-dimensional systems,

$$\sigma = \sigma_0^{3d} exp[-(\frac{T_0^{3d}}{T})^{\frac{1}{4}}] \tag{3.15}$$

with

$$T_0^{3d} = c/(k_B N(E_F) l^3),$$

where c is the proportionality constant, k_B the Boltzmann constant, l is the localisation length, and σ_0 is a temperature independent or weakly-temperature dependent prefactor. We will not address ourselves closer to the formula, but will take the above as the basis to understand the motivation of Vissenberg and Matters for their model of *variable range hopping* in organic semiconductors [76].

3.3.1 Variable range hopping

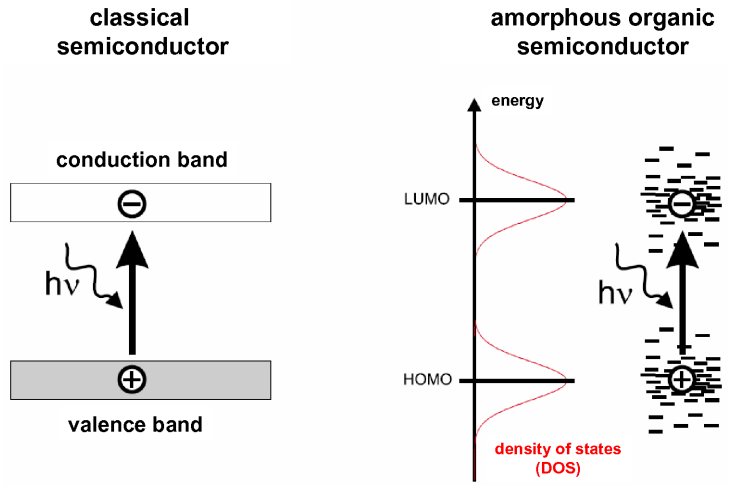


Figure 3.3: *The classical band model representation of a semiconductor and a distribution of localised states with the corresponding density of states around the HOMO and LUMO as assumed for amorphous organic semiconductors. In this case it is a Gaussian distribution.*

Amorphous layers of organic semiconductors mainly result from solution processing of organics. In this work the polytriarylamine (PTAA, cf. chapter 2) is a representative of this group. The deposited layers are generally very controllable in terms of smoothness, homogeneity, and transparency. This makes them very interesting for applications. The charge carriers in such films are strongly localised, the situation in a quasi-band model and the corresponding density of states is described on the right side of fig. 3.3. A certain

spatially and energetically distributed number of localised states around the HOMO and LUMO level leads to a decreasing density of states (in this case it is a Gaussian distribution) into the gap. Vissenberg and Matters interpret the motion in OFET active layers of amorphous organic semiconductors in the sense of Mott and Davies as a variable range hopping between these localised states (for p-type semiconductor this means around the HOMO-level). The motion is governed by a thermally activated tunnelling between the localised states, rather than by activation of trapped carriers to a transport level like in the MTR-model. In this context 'variable range' is meant in the sense of depending on spatial distance and energy of the involved states with carrier hops over short distances at a high activation energy and longer distance hops at a lower activation energy. As mentioned before, a description of the transport strongly depends on the choice of the distribution of the DOS. Mathematically, this is due to the necessary integration over the energetic distribution. In literature the assumptions vary from exponential [77] (amorphous silicon), [76] to Gaussian distributions [78, 79]. From optical analysis exponential band tails (cf. chapter 7) are known to be present in amorphous semiconductors [77, 80]. This fact supports Vissenberg and Matters' choice of a distribution of localised states of the form

$$g(E_a) = \frac{N_t}{k_B T_0} exp\left(\frac{E_a}{k_B T_0}\right) \quad (-\infty < E_a \leq 0) \tag{3.16}$$

where N_t is the number of traps per unit volume, k_B the Boltzmann constant and T_0 is a parameter that indicates the width of the distribution. A second advantage is that the exponential distribution allows an analytic description, whereas the assumption of a Gaussian distribution needs elaborated numerical methods [81]. With the denoted DOS (3.16) and using the percolation theory [82] Vissenberg and Matters conclude a temperature dependence of the conductivity as [76]

$$\sigma \propto exp(E_a/k_B T) \tag{3.17}$$

with an E_a that is weakly (logarithmically) temperature dependent. This is in contrast with the Mott formula [73] where

$$\sigma \approx exp\left[-\left(\frac{T_1}{T}\right)^{1/4}\right] \tag{3.18}$$

due to the assumption of a constant DOS. The field-effect mobility in the VRH-model approximately follows an Arrhenius behaviour

$$\mu \propto (E_a/k_B T) \tag{3.19}$$

with E_a depending on the applied gate voltage, which is explained by the filling of deeper traps (cf. next section) by the accumulated charges. The expression was used to describe the transport in OFETs with solution processed polythienylene vinylene (PTV) and pentacene (both precursor deposited) [83] very well.

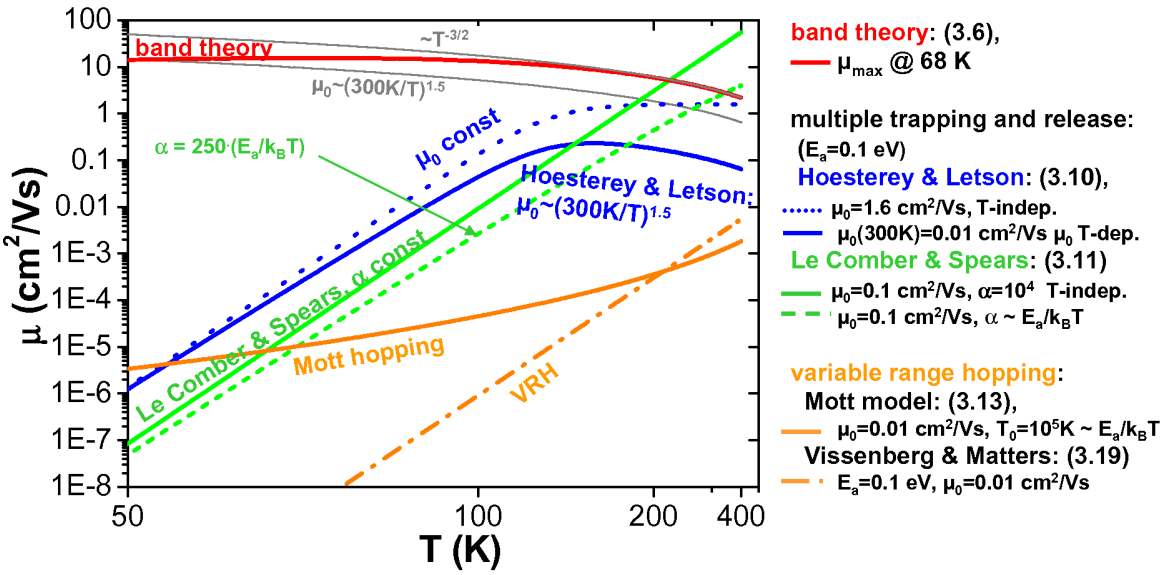


Figure 3.4: *Arrhenius plot of the temperature dependence of the mobility following band theory, the multiple trapping and release, and the variable range hopping mechanism as presented in the sections before. The different models (cf. equation numbers) and assumed parameter values for the presentation are displayed in the table aside.*

3.4 Concept of traps in organic semiconductors

The notion 'trap' has been used in the preceding sections in several instances. This section shall give the general idea of traps in a semiconductor. In this context 'trap' is the generic term for electronic states that influence charge carriers in the semiconductor. They might also be denoted imperfections. This can be due to artificial or accidental doping, the latter would be rather called 'by impurities', and both together form the origin of 'chemical traps', or due to the morphology in the semiconductor, e.g. grain boundaries in polycrystalline films or dislocations in crystals which can be denoted 'structural traps' [84]. They capture, release, or scatter charge carriers (there can be hole or electron traps, charged or neutral) at a certain probability, with characteristic time constants, and specific activation energies. In this way the kind and density of traps defines the transport mechanism and influences the device performance of OFETs. A basic idea that helps to understand the influence of traps on OFET devices is presented in fig. 3.5. The schematic of a band diagram reflects the energetic situation in a semiconductor with traps. Precisely, it considers the situation in the p-type organic semiconductor rubrene. The p-type semiconductor is characterised by a Fermi level E_F near the HOMO-level. Those traps situated between the HOMO and Fermi level (in a range k_BT) are called shallow traps and contribute directly to transport by capturing and release mechanisms. The deep traps are situated within the gap above E_F. Their effect on an OFET performance is mirrored by the threshold voltage: injected holes are captured and remain captured [16]. This simplified model assumes the existence of bands. It will help to understand the intrinsic operation of the OFET (next

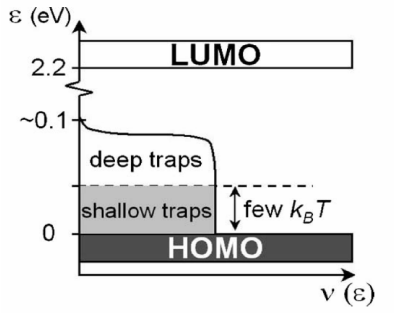


Figure 3.5: *Schematic of localised electronic trap states in the energy gap between HOMO and LUMO. The values correspond to the situation expected in single-crystalline rubrene (from [57]).*

chapter). As traps can generally be classified as electronic states in a semiconductor they constitute the localised states in the model of a localised transport as for amorphous organic semiconductors. Their origin defines the energy and their influence on the transport.

Chapter 4

The thin-film transistor

After the previous chapter on general considerations of transport theory in the field of organic semiconductors, this chapter will be more device specific. It will demonstrate a theoretical background for the treatment of thin-film transistors (TFT). The TFT can be considered as the superordinated class of the organic field-effect transistor and belongs to the family of *insulated gate field-effect transistors* (IGFET). While the first section will give an overview on the assembly and function of the TFT, the second section treats the interfaces that assemble the device. Fundamentals of the oxide-semiconductor (insulator-interface) as well as the metal-semiconductor interface (contacts) will be dealt with. Here the band model will be used in order to understand the energetic situation at the interfaces which defines the transport in the TFT. The insulator-interface of the (organic) semiconductor in combination with the gate contact forms a *metal-insulator-semiconductor(MIS)-diode* structure. The contacts can be considered as *Schottky contacts*. The two sections give the basis for the following mathematical description of the characteristics in thin-film transistor devices. After the treatment of ideal conditions for the description, the section turns to a mathematical description of the TFT in two ways: a simple and a more detailed consideration, where essentially additional charge effects in the device will be taken into account.

This will allow the description of the results of the experimental data which will be discussed in chapters 6–10. The extraction of the main device parameters from the IV-characteristics and the limits of the theory will be the subject of the next chapter.

4.1 Principles in thin-film transistor devices

The elements in the TFT device are the metal contacts, the insulating gate dielectric and the semiconductor, often called the '*active layer*'. Fig. 4.2 shows the characterising band

description of a metal and a p-type semiconductor separated by an insulator in the so-called flat-band condition. $E_{C,V,F}$ are the energies of the conduction band minimum (or LUMO for organic semiconductors), the valence band maximum (or HOMO), and the Fermi level, respectively. Φ_m and Φ_s are the workfunction values (Fermi level to vacuum level) of metal and semiconductor, respectively. χ is the electron affinity (LUMO level to vacuum level) of the semiconductor, which denotes the value for the energy required to detach an electron and thus describes the material's stability in oxidising ambient. If not mentioned otherwise an insulator is treated as ideal which implies a infinitely high (deep) energy barrier of thickness d as displayed in the fig. 4.2. The schematic of a device setup is given in fig. 4.1. A bottom gate and bottom contacts TFT setup is shown which corresponds to the assembly commonly used in the sub-micrometer channel length regime and below. The essential geometry parameters are the channel length L, the channel width W, the thickness of the active layer h and the insulator thickness d_{ox}. The principle is that the current through the semiconducting layer between source (S) and drain (D) contacts is conrolled by the applied voltage between the gate (G) and source contact. This voltage induces charge carriers in the active layer over the gate dielectric. Its capacitance per unit area is given by

$$C_i = \frac{\epsilon\epsilon_0}{d_{ox}} \tag{4.1}$$

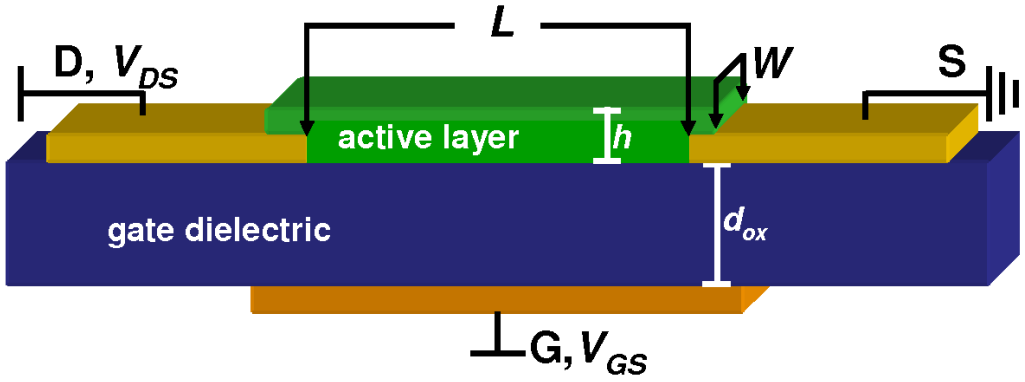


Figure 4.1: *Schematic of a thin-film transistor device with bottom gate and bottom type contacts.*

Historically, one of the first (if not the very first) working thin-film transistor device using polycrystalline layers of CdS as the active layer was presented in 1962 [85]. The principle setup was the same as shown in fig. 4.1. The active layer is deposited in the final step. This is the configuration used in the majority of devices characterised in this work. Due to the final deposition of the active layer it is the best configuration when using the TFT in order to characterise a semiconductor, which is the major interest of this work and also the background for using TFT-devices in fundamental physics investigations. Moreover, fabrication of electrode structures and the semiconductor deposition are more or less decoupled and can be optimised independently. This is an advantage for optimising a parameter in a multistep process. This fact gives a higher degree of freedom in device fabrication which will

be dealt with in the appendix on lithography and device fabrication (appendix B). The disadvantage is a reduced order in the semiconductor layer, because of the deposition on the structured surface. Here, a uniform surface would be desirable. For this purpose the surface pretreatment must be adapted for an optimal growth. An alternative top contact setup, however, has limitations regarding the resolution concerning the channel lengths, where the effort to create smallest channels is far more challenging than when using a lithographically structured surface as in the bottom-contact case.

In any case, the theoretical treatment of the IGFET is applicable for various TFT setups (e.g. top gated, top contact structures). In our description we will focus on the p-type accumulation TFT, which is the exclusively investigated OFET device of this thesis and the majority treated in literature. This differs from the treatment of the most popular device among the IGFET, the *metal-oxide semiconductor field-effect transistor* (MOSFET). In a MOSFET the contacts and the channel are made of the same semiconductor with doping of different type (p, n). A conductive channel is achieved by the inversion of the majority charge carriers in the channel which at the same time removes the blocking pn-junction at the contacts (c.f. [55]). Besides the different aspect of Schottky contacts instead of pn-junctions, an inversion in TFT active layers especially in OFETs is not achievable with sufficient efficiency [86] due to the low density and mobility of free charge carriers. Thus, the working principle is the control of the injected majority charge carriers by a voltage at the insulated gate contact. In this way, as for a MOSFET, the control of the transistor happens capacitively and - ideally - without dissipation loss.

4.2 Interfaces

Following the previous section it should be clear that besides the semiconductor's properties, the TFT is essentially dominated by its interfaces. An ideally working device consists of perfect interfaces. Apart from the properties of the semiconductor layer, the interfaces offer a huge potential for the optimisation of device performance. In order to understand possible effects at the interfaces this section will briefly give the fundamentals of the metal-insulator-semiconductor diode (MIS) and the Schottky contact.

4.2.1 Metal–insulator–semiconductor diode

The metal-insulator-semiconductor diode is the interface that controls the current flow in the TFT device. When applying a voltage between source and gate contact, either a conducting channel between source and drain (fig. 4.1) is induced by accumulation of charges or for a voltage with inverse sign a depletion of charges occurs. A so-called threshold voltage V_{TH} defines the voltage for the onset of current. It is specific to the material and the device, a quantitative definition will be given in the mathematical description of the

device. In this way it defines the working principle of a transistor e.g. in an integrated circuit. Based on the representations of metal and semiconductor in the band model, the

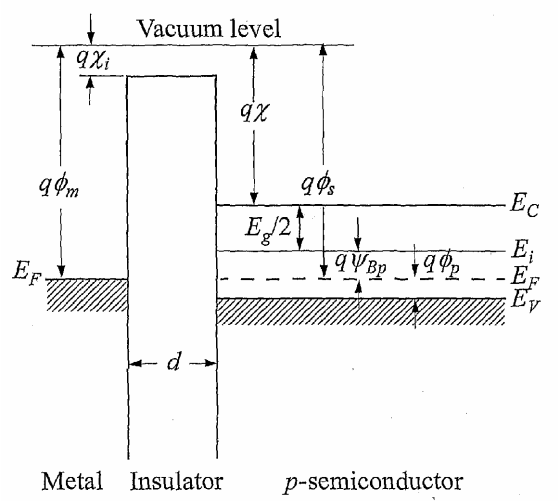


Figure 4.2: *Metal - insulator - semiconductor junction in the band model under flat band condition and with no Fermi level mismatch (from [55]).*

situation in an ideal MIS-diode is shown in fig. 4.2 for a p-type semiconductor. 'Ideal' in this case means that the flat band condition with the matching of metal and semiconductor Fermi level as well as vacuum level at zero applied gate voltage is given. This situation is described by the equation

$$\Phi_m = \chi + \frac{E_g}{q} - \Phi_p, \tag{4.2}$$

where Φ_m is the metal workfunction, E_g $=\mathrm{E}_C - \mathrm{E}_V$ the semiconductor band gap, q the absolute electron charge, and Φ_p $=\mathrm{E}_F - \mathrm{E}_V$ the potential difference between the Fermi level and the valence band edge. When applying a voltage at the gate the surface potential at the semiconductor-insulator interface changes following the definition (p-type case)

$$\Psi_p(x) \equiv -\frac{E_i(x) - E_i(\infty)}{q} \tag{4.3}$$

where $\mathrm{E}_i(x)$ and $\mathrm{E}_i(\infty)$ define the intrinsic Fermi level at distance x from the interface and in the bulk of the semiconductor, respectively, and q is the unit charge. At the surface the potential is $\Psi_p(0) \equiv \Psi_s$ Using this idealised band model, the possible situations in a MIS-diode as shown in fig. 4.3 are:

- *accumulation* - a negative applied gate voltage produces a Fermi level mismatch between metal and semiconductor. For an ideal MIS-diode, no current flows in the structure, so the Fermi level remains flat and the semiconductor reacts by band bending at the insulator - semiconductor interface as shown in fig. 4.3(a). This leads to the induction of the majority charge carriers (holes). The surface potential is negative, $\Psi_s < 0$.

- *depletion* - a small positive voltage applied at the gate depletes the majority hole charge carriers near the interface. This is illustrated in fig. 4.3(b). The Fermi level mismatch is equalised by a band bending of the intrinsic Fermi level E_i towards the Fermi energy. In the depletion case there is $\Psi_{Bp} > \Psi_s > 0$.
- *inversion* - a further increase of a positive gate voltage leads to the inversion of the majority charge carriers, when the Fermi level crosses the intrinsic Fermi level due to the band bending near the interface as shown in fig. 4.3(c). Inversion occurs for $\Psi_s > \Psi_{Bp}$.

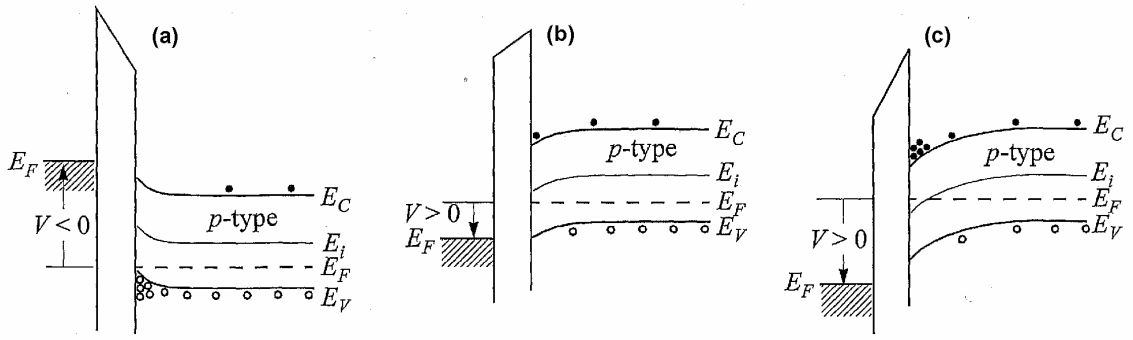


Figure 4.3: *Band diagrams of the three modi depending on bias of an ideal MIS-diode (p-type semiconductor). (a) accumulation of holes for $V_{GS} < 0V$, (b) depletion of holes for small $V_{GS} > 0V$, and (c) inversion, i.e. accumulation of electrons, for $V_{GS} \gg 0V$ (from [55]).*

In a 'real' MIS-diode the contribution of interfacial states due to impurities and imperfections has to be taken into account. There will also be traps in the bulk of insulator and semiconductor that bind induced charges. In the thermal equilibrium this results in a non-flat band condition at zero applied voltage and can be handled by the shift of the threshold voltage that is needed for the flat band condition. In the description of the IGFET which will follow after a treatment of metal-semiconductor contacts, the possible charges at the gate interface will be dealt with. This will lead to a more elaborated description of the threshold voltage for IGFET as well as for OFET devices. In that context the meaning and origin of traps accords to the description in section 3.2.1.

4.2.2 Metal–semiconductor interface, the transistor contacts

The second critical interface of a TFT device is the source and drain contact (cf. fig. 4.1). In the thin-film transistor design applied in the field of OFET it is usually a metal (polymer or inorganic) to (organic) semiconductor interface. In this way it should ideally follow the theory of a *Schottky contact*.

In the ideal case of bringing the two materials together surface states at the interface are excluded, which would influence the energetic situation. For the injection of charge carriers

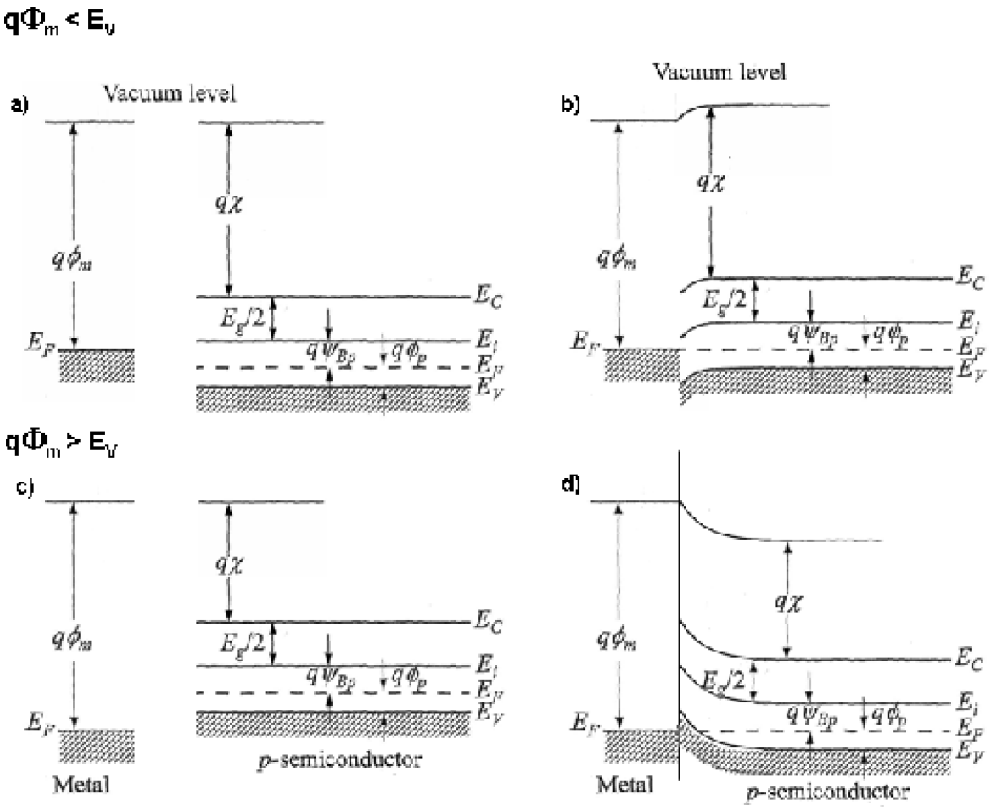


Figure 4.4: *Ideal Schottky contacts of a metal and a p-type semiconductor. Part (a) and (b) display the case when the metal Fermi level is higher than the valence band edge energy ($q\Phi_m < E_V$), where (a) is the flat band condition with equal vacuum level when the two materials have no contact and (b) is the intimate contact. The bottom diagrams (c) and (d) show the opposite case ($q\Phi_m > E_V$) in flat band condition and after intimate contact, respectively.*

into the semiconductor the relation between the metal Fermi energy and the semiconductor band energy for the injected charge carrier type ($q\Phi_m$ and $E_{C/V}$, respectively) as well as the width of a formed depleted space charge zone for the injected carrier type at the interface are crucial. In the p-type semiconductor case the contact potential is given by $\Phi_m - (\chi + E_g - \Phi_p)$ (cf. fig. 4.2). The band diagrams in 4.4 reflect the two possible situations: in parts (a) and (b) the energetic relation is $q\Phi_m < E_V$, in (c) and (d) $q\Phi_m > E_V$. In both cases the band diagrams on the left side describe the situation for a spatial separation of the two materials with aligned vacuum level. In the right side diagrams the two materials are brought together. The Fermi level E_F must be equal in both materials in thermal equilibrium. This happens by band bending in the semiconductor material, due to its substantially lower density of charge carriers compared to the metal. In the top case, where the metal Fermi level is above the semiconductor Fermi level, the result is the depletion of holes at the interface due to the downward bending of the bands. A depleted space charge region of width W depending on the density of charge carriers in the semiconductor is formed due to the immobile negatively charged acceptor dopant ions.

This means an injection barrier for hole transport into the semiconductor of height

$$q\Phi_{b0} = E_g - q(\Phi_m - \chi)$$

which is the difference between metal Fermi level and E_V. This is the situation in a *Schottky-type* of contact.
In the bottom case where $q\Phi_m > E_V$, the band bending is upwards and holes are accumulated at the interface. This is the desired behaviour without an additional injection barrier for p-type semiconductors which will result in an *ohmic* contact.

In reality surface states can not be excluded, especially in an *ex situ* step during the fabrication of interfaces. Both the metal workfunction and the functionalised organic material are modified. A review on metal–organic interfaces by Kahn et al [87] reports a breakdown of the simple vacuum level alignment rule - the so-called *Schottky–Mott limit*, used above. They experimentally prove the effect of surface dipoles and in this way induced barriers at the interfaces by a combination of optical and electrical investigations. Furthermore the impact of the interface dipole on the molecular level alignment can be used to manipulate or tune metal workfunction values by the deposition of self-assembled monolayer (SAM) [88, 89], in order to optimise the injection of charge carriers in a specific device. There has been experimental evidence for the use of thiols SAM on the metal contacts in order to improve the device performance of different organic electronic and optoelectronic devices [89, 90, 91], which is especially desirable in low-voltage injection devices.

In the Schottky-Mott limit, the width of the resulting space charge zone and the relation of the workfunctions of metal and semiconductor determine the detailed current vs. voltage behaviour. For a space charge zone of considerable width there is an injection barrier for one direction of applied voltage. This is the situation in a Schottky-diode. For neglectable width a high tunnelling rate of charge carriers through the barrier makes a quasi-ohmic contact. The width of the Schottky injection barrier is given by the potential step height and the density of the acceptor states (in the case of a p-type semiconductor) N_A [55, 92]. In a unipolar material as the organic semiconductors under investigation this is essentially equal to the density of the majority charge carriers n_h (p-type) in the semiconductor. It follows for the depletion width W

$$W \propto \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} - V_A)} \tag{4.4}$$

where V_{bi} is the built-in voltage in the Schottky contact, ϵ_s is the permittivity of the semiconductor, and V_A is the applied voltage across the junction in the forward bias. The junction capacitance per unit area C_j is then obtained from ϵ_s/W. Sufficiently high doped semiconductors result in a quasi-ohmic contact with a metal. An additional aspect is the forming of alloys at the interface or chemical bonding, which normally results also in an ohmic behaviour [93]. The evaluation of contacts under the assumption of ohmic contacts in OFETs will be discussed in section 5.2.

4.3 The thin-film transistor

The following section will continue with the mathematical description of the thin-film transistor. Idealising assumptions necessary for the description will be followed by two derivations of characteristics in the device: on the one hand a first simple ansatz and on the other hand a more detailed consideration taking into account an increased number of the involved charge effects in the device. They allow the extraction of the device parameter which characterise the active layer material as well as the device setup.

4.3.1 Ideal transistor behaviour

For the treatment of the ideal TFT several assumptions are made:

- the gate-insulator-semiconductor structure behaves like an ideal MOS-diode. Especially, there are no trapped charges in the insulator or at the insulator-semiconductor interface
- the contact-semiconductor interface is ideal in the sense of a low-resistance injection of charge carriers into the semiconductor.
- only drift currents are considered
- the drift mobility is constant in the whole semiconductor
- the gradual channel approximation (Shockley approximation) is valid. This means we have a two-dimensional conductance in the semiconductor, the transverse electrical field induced by V_{GS} is large compared to the longitudinal field by V_{DS}.

$$E_{tr} \gg E_{lo}$$

Trapped charges would introduce an additional capacitance. If further trapping and release mechanism is assumed this will introduce dynamical effects in the device performance, e.g. in integrated circuits. In this case the constant relation between applied gate voltage, MIS capacitance and resulting accumulation of charge carriers would require a more complicated treatment. As mere effect on the threshold voltage, in the sense of the voltage shift needed for establishing a flat band condition, they will be treated in the more detailed consideration. The low-resistance and ohmic injection avoids the treatment of additional contact barriers and the channel voltage dependent width of the Schottky depletion zone at the contacts. Besides the reduction of the effective channel length, this would additionally involve tunneling mechanism. The consideration of only drift currents avoids diffusion currents in the semiconductor. Finally, the last point - the Shockley approximation - is needed in order to apply the Poisson ansatz for the description.

4.3.2 Characteristics of the ideal TFT

Simple consideration:

In a device like in fig. 4.1 with no V_{GS} applied the longitudinal electrical field E_{lo} in the channel of length L is

$$E_{lo} = -\frac{V_{DS}}{L}. \tag{4.5}$$

The charge carrier drift time is then given by

$$t_L = \frac{L}{v} = \frac{L}{\mu E_{lo}} = -\frac{L^2}{\mu V_{DS}}. \tag{4.6}$$

The last row incorporates the relation between the drift velocity, the mobility and the electrical field (3.1) and equation (4.5). When the total charge in the channel is Q_{ch}, the stationary current will be

$$I_D = -\frac{Q_{ch}}{t_L}. \tag{4.7}$$

When a gate voltage is applied, the potential in the channel V_{ch} which is relevant for the induced charges Q_i depends locally on both V_{DS} and V_{GS}. A first approximation gives the mean value

$$\bar{V}_{ch} = V_{GS} - \frac{V_{DS}}{2}. \tag{4.8}$$

Then the induced charges over the insulator capacitance along the channel C_{ch} is:

$$Q_i = -C_{ch}(V_{GS} - \frac{V_{DS}}{2}).$$

The intrinsic charges Q_0 and induced charges add up to the total channel charge $Q_{ch} = Q_i + Q_0$. It follows from (4.7):

$$\begin{aligned} I_D &= -\tfrac{Q_i+Q_0}{t_L} = \tfrac{\mu V_{DS}(Q_i+Q_0)}{L^2} && (4.9)\\ &= \tfrac{\mu V_{DS}}{L^2}[Q_0 - C_{ch}(V_{GS} - \tfrac{V_{DS}}{2})] && (4.10)\\ &= \tfrac{W\mu V_{DS}C_i}{L}[(V_{GS} - \tfrac{Q_0}{C_i} - \tfrac{V_{DS}}{2})]. && (4.11) \end{aligned}$$

The last equation implies the relation: $C_{ch} = C_i \times$ *channel area* $= C_i WL$ with C_i from (4.1).
Equation (4.11) describes a parabolic dependence of I_D on V_{DS}. The apex of the parabola can be identified to

$$V_{DS}|_{\frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}=const}} = V_{DSsat} = V_{GS} - \frac{Q_0}{C_i} = V_{GS} - V_{TH} \tag{4.12}$$

where the parameter V_{TH} is introduced. It represents a threshold voltage for the transport. We will discuss the meaning of V_{TH} later in this and the following chapter. At V_{DSsat} the potential difference between the gate and the channel at drain becomes zero. This is the so-called *pinch-off*. No charge carriers are induced at that point. The voltage being further

increased the pinch-off point moves to the source electrode (cf. the TFT schematics of fig. 4.5). The current at drain saturates because no additional charges are induced. The different regimes in the standard output behaviour at constant V_{GS} beyond the threshold of an IGFET are shown in the diagrams of fig. 4.5. The top diagram shows a linear increase of the current for V_{DS} near zero this is in first order the approximation of equation (4.11) for small V_{DS}:

$$I_D \approx \frac{W\mu C_i}{L}[(V_{GS} - V_{TH}] \cdot V_{DS}. \tag{4.13}$$

In the mid diagram the parabola of (4.11) branch until the pinch-off point is shown and the bottom figure presents the complete output characteristic with a saturating current for a voltage beyond V_{DSsat}. The pinch-off represents the limit of the simple consideration that ended with (4.11). The replacement therein of V_{DS} by V_{DSsat} from (4.12) leads to the expression for the V_{GS} dependent saturation current:

$$I_{Dsat} = \frac{W\mu C_i}{2L}[(V_{GS} - V_{TH}]^2. \tag{4.14}$$

More detailed consideration:

Equations (4.11)–(4.14) describe the characteristics of thin-film transistors rather well. The theoretical background, however, is very simplified, e.g. the assumption of the potential in the channel (4.8) is not correct. The basic ansatz for charge currents is its definition using the current density:

$$I = \int_A j,$$

in the unipolar, p-type semiconductor case, this leads to

$$I_D = q\mu(x)\rho(x)\frac{dV(x)}{dx}Wh \tag{4.15}$$

where q is the unit charge, μ the mobility, ρ the charge density, W the channel width, and h the height of the channel (c.f. fig. 4.1). Equation (4.15) needs to be integrated over the channel length where the current remains locally independent. It is necessary to discuss possible contributing charges to ρ. We will partly abandon the assumptions from 4.3.1. q remains the unit charge but any indexed small letter q is a specific charge per area.
In a real device there will be trapped charges in the insulator q_i especially when using SiO_2. The latter influence counter charges $q_k = -q_i$ at the insulator-semiconductor interface. In the band model they cause a bowing of the bands at the interface. Flat band condition is achieved by eliminating these charges with a voltage applied at the gate

$$V_{F0} = \frac{q_k}{C_i} = -q_i\frac{d_{ox}}{\epsilon\epsilon_0}.$$

Another contribution to charges in the device with no gate voltage applied is the counter charge to a contact potential at the gate electrode $q_{Kp} = -V_{Kp} \cdot C_i$ the "real" flat band voltage changes to

$$V_F = V_{F0} - V_{Kp}.$$

In this case, one has to consider the influence of volume charges in the bulk material q_B. Moreover traps of density n_t are distributed locally in the semiconductor and energetically in the forbidden gap. With no regard to any trapping and release dynamical behaviour, they catch charges and have to be satisfied before a charge transport in the channel can occur. All these effects - and maybe additional ones, which will be omitted here - can be summed up by a threshold voltage. The simple consideration was purely defined by the intrinsic charges in the device, this is the ideal case of an accumulation FET. This image has to be corrected:

$$V_{TH} = V_F - \frac{1}{C_i}(\bar{q}_B + q\bar{n}_t) \tag{4.16}$$

where q_B is the space charge contribution of the bulk material. The bar means that both q_B and n_t are not varying along the channel length. The induced mobile charges q_p are then

$$q_p(x) = q\rho(x)h = -C_i(V_{ch}(x) - V_{TH}) = -C_i(V_{GS} - V_{TH} - V(x)). \tag{4.17}$$

Here the inducing voltage V_{ch} is described by $V_{ch} = V_{GS} - V(x)$ where the term V(x) results from the superposition of V_{DS} and V_{GS} in the channel. As in the simple consideration the validity of this consideration is limited to the pinch-off because of the condition $0 \geq V(x) \geq V_{DS}$:

$$V_{GS} - V_{DS} < V_{TH}. \tag{4.18}$$

Now ρ can be replaced in (4.15) and both sides be integrated, where the mobility is considered locally independent $\mu(x) = \mu_0$ as in the ideal asumptions.

$$I_D \qquad = W\mu(x)C_i(V(x) + V_{TH} - V_{GS})\tfrac{dV(x)}{dx} \tag{4.19}$$

$$I_D \int_0^L dx \quad = W\mu_0 C_i \int_0^{V_{DS}} (V(x) + V_{TH} - V_{GS})dV(x) \tag{4.20}$$

$$I_D \qquad = \tfrac{W}{L}\mu_0 C_i[\tfrac{V_{DS}^2}{2} + V_{DS}(V_{TH} - V_{GS})] \tag{4.21}$$

The last equation is substantially equal to (4.11). In the oncoming chapter we will consider the extraction of the device parameters as well as additional aspects to the theory.

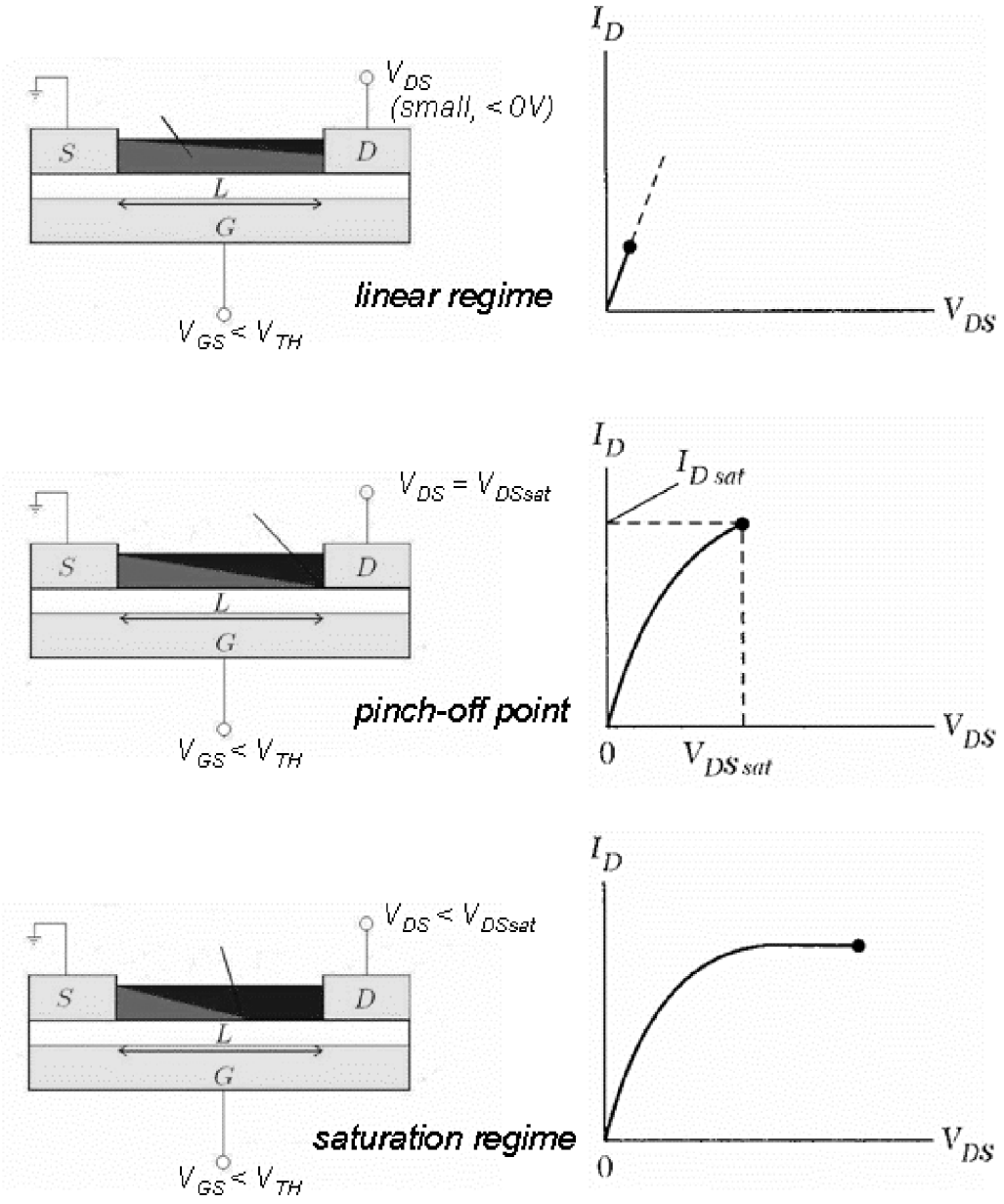


Figure 4.5: *The different regimes in an IGFET output characteristic at V_{GS} beyond the threshold voltage and the corresponding bias situation in the device: linear increase of the current I_D for small V_{DS} (top), parabolic behaviour for higher V_{DS} leading to the pinch-off at the parabola's apex at $V_{DSsat} = V_{GS} - V_{TH}$ (middle), and saturating current I_{Dsat} for V_{DS} beyond the pinch-off point (bottom).*

Chapter 5

Special aspects to theory in real devices

This chapter is intended to build a bridge between theory and experimental results by the treatment of special aspects relevant in real OFET devices. They are closely connected to the chapters 6–10. This introduction will continue with the explanation of notions in order to give a better insight into the transport behaviour of TFT devices. Then the following three sections - in this order - first treat the description of TFT device parameters, their extraction from the characteristics, and their meaning for the intrinsic transport properties of the semiconductor layers, as well as for the aspects of device physics. Secondly the influence of the contact on device performance will be addressed. This will be illustrated by experimental data on dihexylquaterthiophene OFETs. The last section will deal with the aspect of miniaturisation of TFT devices and the oncoming of short channel behaviour in OFETs, the experimental results regarding this will follow mainly in chapter 9.

Space charge in OFETs: In the previous considerations the notion of space charge appeared at interfaces and in the bulk resulting from immobile (ionic) charges depopulated by their mobile partners, the electrons or holes. The notion of space charge limited current was first attributed to the resulting localised region of excess negative charge driven out of a heated metal. It was first observed by Thomas Edison in light bulb filaments, which is sometimes also called the *Edison Effect*. In a semiconductor a space charge is constituted at the surface region by excess or deficiency of electrons. They originate from energy mismatch at the interface (to a metal or insulator), which also causes the band bending in the band model.

Grain boundary effects: Grain boundaries, during crystalline growth, result from different crystallisation centres that grow together, e.g. in organic molecular beam deposition (cf. appendix A). If the surface does not provide a special crystalline order the edges of these grains will form dislocations within the crystalline film and in this way will limit the long-range order and thus the performance in OFETs. Grain boundaries constitute a main contribution to the density of traps in an organic film.

Polarons, charge carriers in OFET devices: Polarons are so-called quasiparticles that consist of a charge carrier bound to a polarisation in the surrounding medium. The charge transport in the OFET occurs in the organic semiconductor near the interface to the dielectric (cf. fig. 4.1). In this way the injected charge carriers in OFET devices can be understood as two-dimensional polarons due to their polarising effect on the structure (crystalline or not) of the organic semiconductor near the insulator interface. The theory considers two possible kinds of polarons responsible for the transport properties in OFET. On the one hand, the *Holstein Polaron* is defined by the polarisation effect due to a short-range deformation of the molecular crystal [94]. On the other hand, the *Fröhlich polaron* has a more long-range origin by the polarisation effect due to an ionic polarisation cloud in the surrounding medium [95]. In the latter reference, the conclusion is that both types of polaron transport occurs in OFETs, where the nature of the dielectric and the crystallinity in the organic semiconductor at the dielectric interface are crucial. The constitution of *Fröhlich polarons* is favoured in devices with a sufficiently polar dielectric and a highly ordered organic semiconductor.

5.1 Device parameters

The diagrams of fig. 5.1 show exemplary characteristics of an OFET based on $\alpha\alpha'$-dihexylquaterthiophene. The field of characteristics in diagram (a) are the output characteristics $\mathrm{I}_D(\mathrm{V}_{DS})|_{V_{GS}=const}$ for different V_{GS}. with linear and saturation regime as already presented schematically in fig. 4.5. The orthogonal sections of this field of output characteristics denoted by the vertical lines at $\mathrm{V}_{DS} = -1$ V and $\mathrm{V}_{DS} = -15$ V in fig. 5.1 (a) represent the transfer characteristics $\mathrm{I}_D(\mathrm{V}_{GS})|_{V_{DS}=const}$ from the linear and the saturation regime, respectively. They are displayed in the two other diagrams. Here, diagram (b) shows the representation with linear scaling of the current axis and diagram (c) with the logarithmic scaling. In all diagrams the red lines are fits to the data points following the derived equations (4.11).

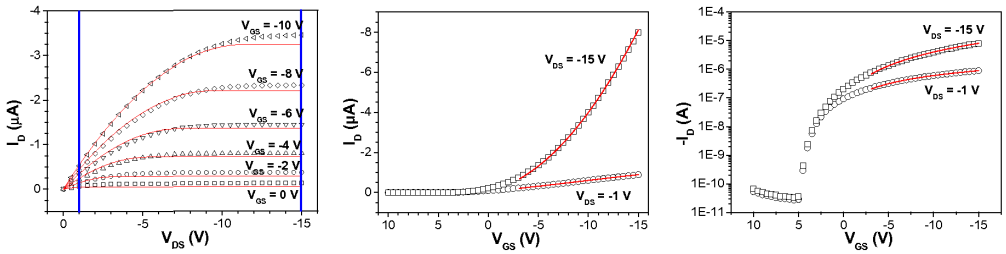


Figure 5.1: *Three diagrams representing a field of output characteristics (a), and the transfer characteristics in the linear regime ($V_{DS} = -1$ V) and in the saturation regime ($V_{DS} = -15$ V) in linear current representation (b) and logarithmic one (c). The vertical lines in diagram (a) mirror the context between transfer and output characteristic. The red lines are fits to the data following the derived theory from the previous chapter.*

5.1.1 Extraction of the mobility

Knowing the geometry parameters channel width W, channel length L and the capacitance per unit area C_i of the OFET, the mobility directly follows from the slope of the transfer curves or alternatively after the application of the theory on the field of output characteristics which involves an increased fitting effort. For the linear regime the slope follows from a fit of the form $y = P_1(x - P_2)$ with P_1 the fitting parameter that includes the geometry parameters, the applied V_{DS}, and the mobility, and the second fitting parameter $P_2 = \left(V_{TH} - \frac{V_{DS}}{2}\right)$ (cf. 5.1.2).

$$\mu_{lin} = \frac{L}{WC_iV_{DS}} \cdot \frac{\partial I_D}{\partial V_{GS}} \tag{5.1}$$

In the saturation regime the transfer curve ideally follows a parabolic fit of the form $y = P_1(x - P_2)^2$ with P_1 again resulting as the product of the geometry parameters and the mobility but independent of V_{DS}, and $P_2 = V_{TH}$.

$$\mu_{sat} = -\frac{L}{WC_i} \cdot \frac{\partial^2 I_D}{\partial V_{GS}^2} \tag{5.2}$$

5.1.2 Extraction of the threshold voltage

The threshold voltage has decisive influence on the device performance of a transistor within e.g. integrated circuits. Therefore, its origin and manipulation in device optimisation is of crucial interest. In the previous chapter it was clarified that the origin of V_{TH} in an accumulation field-effect transistor are inherent charges in the involved materials or charge effects like trapping of charge carriers. In the ideal case of an accumulation FET, flat band condition with ideal interfaces and an intrinsic semiconductor, charge carriers, i.e. electrons or holes, should be accumulated by any positive or negative gate voltage [96], respectively, such that $V_{TH} = 0V$. The anyhow observed threshold voltages in OFETs can be ascribed to the (counter-) voltage which is required to establish flat band condition and the voltage needed for the saturation of localised trap states. Equation (4.16) gives just a first expression for the involved fractions. Horowitz et al for example introduce a zero voltage V_0 connected to the equilibrium free carrier density in the case of a constant mobility [86]. Thus, this procedure follows the description which results in (4.16). The observation of a gate voltage dependent mobility however demands a more elaborated description. In this way V_{TH} results as fitting parameter. After the above fitting descriptions V_{TH} from the linear regime follows as

$$V_{THlin} = P_2 + \frac{V_{DS}}{2}, \tag{5.3}$$

and from saturation

$$V_{THsat} = P_2. \tag{5.4}$$

In section 5.3 the channel length dependence of the threshold voltage for smaller channel lengths will be given.

5.1.3 The subthreshold regime

From the fitting in fig. 5.1(b) it is obvious that there is current flow in the transistor before the defined threshold voltage for both regimes. The logarithmic scaling of the current in part (c) of the same figure demonstrates that the current increases exponentially with V_{GS}. In an inversion MOSFET it describes the state of weak inversion. The origin in the accumulation type FETs like the OFETs is still under discussion but can most likely be ascribed to influences of traps in the bulk and/or at the interfaces [97, 98]. The slope in the subthreshold regime is of interest in low voltage and low power applications, e.g. digital switches or memories, because it defines the switching speed of the devices. The characterisation is achieved by the so called *subthreshold swing*

$$S = lg10 \cdot \frac{V_{GS}}{d(lgI_D)} \qquad [V/dec]. \tag{5.5}$$

The scaling behaviour of S in devices with different active materials will be investigated in the result part. The subthreshold regime separates the *off-state* and the *on-state* of the transistor (fig. 5.1(c)). In the oncoming chapters of this thesis the ratio between on- and off-state will be defined by the maximum current value in the on-state divided by the minimum current value in the off state

$$I_{on}/I_{off} = \frac{maximum[I(V_{GS})]}{minimum[I(V_{GS})]}. \tag{5.6}$$

5.2 Contacts

The performance of OFET devices is strongly influenced by the metal-organic interface and the injection of charge carriers. Under the assumption of ohmic contacts the device resistance is the serial resistance of the organic channel R_{ch} and the total contact resistance $R_{co} = R^d_{co} + R^s_{co}$

$$R_t = R_{co} + R_{ch}$$

The contact resistance is evaluated from the linear regime considering an additional voltage drop [37]

$$I_D = \frac{W}{L}\mu C_i(V_{GS} - V_{TH})(V_{DS} - I_D R_{co}) = \frac{W/L\mu C_i(V_{GS} - V_{TH})V_{DS}}{1 + W/L\mu C_i R_{co}(V_{GS} - V_{TH})}. \tag{5.7}$$

Using the definitions of the transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}}$ and the drain conductance $g_d = \frac{\partial I_D}{\partial V_{DS}}$, the above equation for the intrinsic mobility simplifies to

$$\frac{g_d}{\sqrt{g_m}}\sqrt{\frac{W}{L}\frac{V_{DS}}{C_i}} = \sqrt{\mu}(V_{GS} - V_{TH}). \tag{5.8}$$

In the linear regime $g_d \approx \frac{I_D}{V_{DS}}$ and the contact resistance R_{co} follows as

$$R_{co} = \frac{V_{DS}}{I_D} - \frac{L}{W\mu C_i(V_{GS} - V_{TH})}. \tag{5.9}$$

The last equation accords to a straight line

$$\frac{WV_{DS}}{I_D} = const \cdot L + \rho_{co}, \tag{5.10}$$

where $\rho_{co} = R_{co} \cdot W$. In this way the specific contact resistance ρ_{co} graphically results from the intersection with the ordinate using corresponding V_{DS}/I_D-pairs of a series of devices with differing channel length.

An evaluation of ohmic contact resistance in the saturation regime can be carried out by the mere consideration of involved resistances. For a constant intrinsic mobility of the organic film effects the channel resistance scales with L, $R_{ch} = \rho_{ch}L$, where ρ_{ch} is the constant specific channel resistance and we obtain with equation (4.14)

$$I_D = \frac{V_{0,DS}}{R_{co} + R_{ch}} = \frac{V_{0,DS}}{R_{co} + \rho_{ch} \cdot L} \propto \frac{\mu}{L} \tag{5.11}$$

$$\mu(L) \propto \left[\rho_{ch} + \frac{R_{co}}{L}\right]^{-1} \tag{5.12}$$

where $V_{0,DS}$ denotes the voltage applied between source and drain contact. The influence of the contact resistance on the mobility μ(L) increases with decreasing channel length L. Therefore, the contact resistance can be derived from the decrease of $\mu(L)$ with decreasing L. Fig. 5.2 shows in diagram (a) the mobility values μ(L) obtained from three series of

contact material	Φ_m [eV]	ρ_{Co} [MΩ·mm]	S [V/decade]
Ti/Au	4.1/4.8	2	-0.59
Ti/Pt	4.1/5.3	1.4	-0.32
Pd	5.0	0.2	-0.36

Table 5.1: *Properties of DH4T-TFTs with different contact metals. The work function value Φ_m for the employed metals [99], the calculated specific contact resistance ρ_{Co}, and the subthreshold swing value S in each case for a L = 4 μm device.*

OTFTs, whose contact metals were Ti/Au (thickness 5/25 nm), Ti/Pt (5/25 nm) and Pd (25 nm). Each series covered a variety of channel lengths L in the range between 1 μm and 50 μm. Obviously, the mobility value μ decreases with decreasing L for the Ti/Au and Ti/Pt contacts, in accordance with the expected increasing role of the contact resistance. In contrast, for Pd contacts there is no distinct mobility drop with decreasing L. The resulting specific contact resistances $\rho_{co} = R_{co} \cdot W$ are listed in table 5.1. The Pd value of 0.2 MΩ·mm is by a factor of 10 lower than the value for Ti/Au and by a factor of 7 lower than Ti/Pt.

The contact resistance is expected to be influenced essentially by the work function Φ_m of the contact metal. Φ_m determines the hole injection into the highest occupied molecular

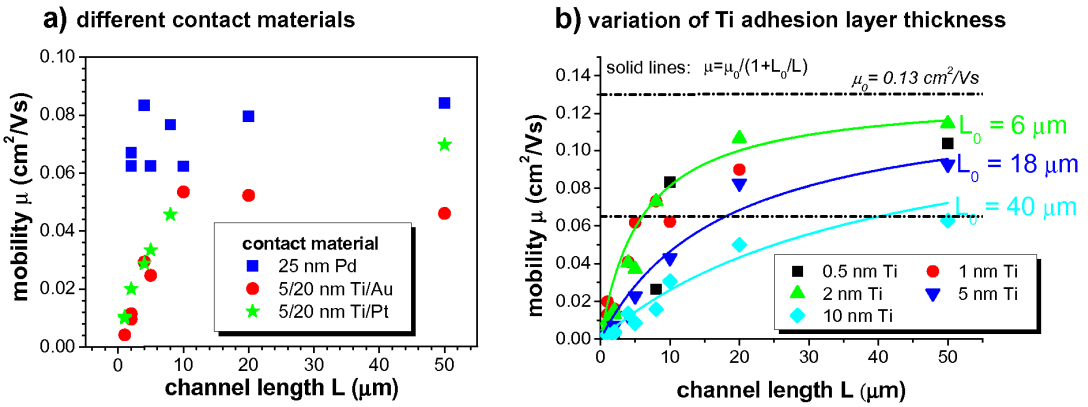


Figure 5.2:
(a) The scaling behaviour μ(L) for various devices with differing contact material, 5/20 nm thick Ti/Au, 5/20 nm thick Ti/Pt, and 25 nm thick Pd. L is ranging from 1 to 50 μm. (b) The scaling behaviour μ(L) of five different DH4T samples with TFT-structures. (L is ranging from 1 to 50 μm). The Ti thickness within the 25 nm thick Ti/Au structures is 0.5, 1, 2, 5, 10 nm, respectively.

orbital (HOMO) of the p-type DH4T. High Φ_m values are beneficial for a low contact resistance. In our case the values for the work functions of the noble metals are comparable ($\Phi_m = 4.8$ eV, 5.0 eV, and 5.3 eV, for Au, Pd, and Pt, respectively). They cannot explain the different behaviour of Pd with respect to Au and Pt. Titanium, however, has a considerably lower work function of 4.1 eV, which is unfavourable for carrier injection. This is a hint that the Ti adhesion layer may be relevant for the different behaviour of Ti/Au and Ti/Pt with respect to Pd contacts. In order to investigate the influence of the Ti adhesion layer, μ(L) was analysed for five series of OTFTs with Ti/Au contacts. Each series had a specific Ti adhesion layer thickness d_{Ti}. The d_{Ti} values were 10 nm, 5 nm, 2 nm, 1 nm, and 0.5 nm. Within each series the channel length L stepwise decreased from 50 μm to 1 μm.

The scaling behaviour of the mobility for these series is presented in fig. 5.2 (b). The trend of the experimentally derived data is the same as part (a) of the same figure and follows equation (5.12): decreasing mobility for decreasing channel length L due to the increasing influence of the contact resistance. However, this effect is strongly reduced with decreasing adhesion layer thickness.

This result confirms the detrimental influence of the Ti adhesion layer for the carrier transport at the organic-metal interface. Obviously, best transport properties using DH4T occur when the first monolayers of the organic layer have a direct connection to the Au contact layer. This underscores the assumption that the first monolayers of the organic molecules, i.e. those near the interface to the oxide layer, are the essential ones for the electrical current. (Also observed in *in-situ* experiments during deposition, cf. chapter 8, [100]). Following these results the necessary Ti adhesion layer thickness under electron beam evaporated gold or platinum should be limited to a value below 2 nm.

5.3 Short channel behaviour

This section will explain the effects of OFET devices which are due to a reduction in size. The subordinate concept for this is *short channel behaviour*, which combines effects that have their origins at the different device interfaces (insulator-semiconductor, contacts) as well as in the geometry factors of the semiconducting material, the insulator and the contacts. The crucial meaning of miniaturisation for advances in the field of semiconductor technology is omnipresent. Especially due to the low upper limit of field-effect mobility in organic semiconductors a reduction of sizes is the key parameter to further improve the performance of OFETs in integrated circuits. The maximum switching frequency in FET devices for example is proportional to μ and antiproportional to L^2 [55]

$$f = \frac{\mu}{L^2}. \tag{5.13}$$

The frequency is a key parameter for switching ability for example in RFID-tags, and other integrated circuits applications, where in the former the common standards are 128 kHz and 13.54 MHz. Already for high mobility organic semiconductors the MHz values can only be achieved by sub-micrometer channel lengths. Still equation (5.13) is based on standard behaviour of the device in the sense of following the characteristics from 4.3. This behaviour will be called *long-channel behaviour* in the rest of this work. Other advantages of a reduced size in devices are a reduced influence of grain boundaries, e.g. in the case of $\mu = \mu(\mathrm{L}) \propto 1/\mathrm{L}^n$ (n> 0). Disadvantages are that interfacial effects become more and more important like contact resistances (cf. section 5.2) and other effects at the interfaces (e.g. traps or charging and leakage currents). For reducing the size they have to be sufficiently low to avoid their domination of the characteristics. In our considerations the minimum sizes will be kept in the deep sub-micrometer region (down to 10 nm), where there is still no need to regard quantum effects as for example in the case of molecular devices. The first effect of a reduction of sizes is a changing of the capacitance and thus the electrical field if the applied bias voltage remains the same. In first order (under the assumptions of the simple consideration of 4.3.2) one would expect that the OFET characteristics will be maintained in the long-channel behaviour if the biases are reduced in the same way as the sizes. The existence of space charges at the interfaces destroy this easy image, because they are based on intrinsic material specific properties and usually cannot be scaled down in the same way as electrodes and layer thicknesses.

The short channel effect (SCE)

From MOSFET technology it is known that by a reduction of the channel length while keeping the other device parameters constant, the space charge zone at the insulator interface is reduced by the space charge zone of the contacts [55, 101]. This is illustrated in fig. 5.3. The space charge at the insulator interface is specific per area. The reduction due to the contact's space charge zones is a constant contribution, thus the necessary gate induced charges to compensate these charges is reduced which is directly followed by a lower threshold voltage V_{TH}. One has to be careful with generalising this explanation to the OFET devices. The SCZ on each side of a pn-junction will always be of the inverted type, and extend into the channel, because of the higher doping level of the contacts. Thus,

due to the 'channel using charge carrier inversion' principle in MOSFETs it will always effectively reduce the channel. The OFET's SCZ at the contacts are a consequence of the type of contact (see 4.2.2). In the Schottky-Model the charge type depends on the metal and semiconductor Fermi level. In the case of a p-type OSC an effective reduction of the channel will be granted if the metal Fermi level ($\approx$ workfunction) is energetically lower (of higher absolute value) than the Fermi level of the semiconductor. This is displayed in the bottom diagrams of fig. 4.4. The electrostatically forced bending in the semiconductor bands will accumulate holes at the interface to the contacts. In the case of the top diagrams, where a Schottky depletion zone of width W (4.4) is generated the effect will be an injection barrier which would drive the threshold voltage to more negative values. In consequence, equation (4.16) must be extended by the positive accumulation charges or the negative space charges at the contacts Q_{co} =Q_D+Q_S. In this way, the length dependence of the threshold voltage follows:

$$V_{TH} = V_F - \frac{1}{C_i}(\bar{q}_B + q\bar{n}_t - \frac{Q_{co}}{W \cdot L_{co}}), \tag{5.14}$$

where Q_{co} should ideally define the type of contact, W is the channel width, and L_{co} the reduced expansion length into the channel region of the space charge zones at source L_S and drain L_D. $L_{co} = \frac{2L_S L_D}{L_S+L_D}$. In this context the shift of the parameter V_{TH} compared to a reference long-channel value, where $L_{co} \ll$L is often used as a figure of merit for the influence of the SCE [101].

$$SCE = \Delta V_{TH} = V_{TH}(L_{long}) - V_{TH}(L_{short}), \tag{5.15}$$

here $V_{TH}(L_{long})$ and $V_{TH}(L_{short})$ are the threshold voltage value for the reference long channel and the evaluated short channel, respectively. Equation (5.15) allows a qualitative

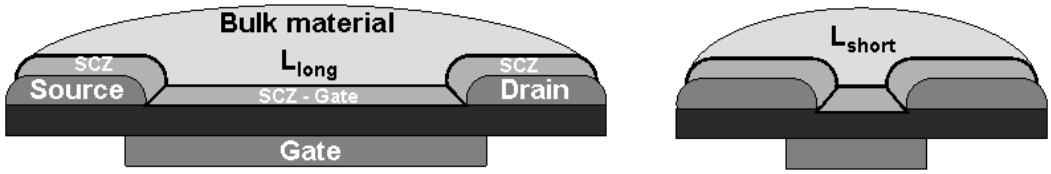


Figure 5.3: *Long channel to short channel TFT, the effective reduction of charges in the space charge zone at the insulator interface by the channel length independent space charge zone at the contacts.*

evaluation of the type of contact. A resulting n-type SCZ at the contacts of a p-type OFET would not cause a reduced threshold voltage, but rather an increased one following equation (5.14).

The drain induced barrier lowering (DIBL)

Again making the analogy to the MOSFET devices, the DIBL is the reduction of the diffusion barrier of the p-n-junctions (the contacts), induced by the applied drain voltage [55, 101] (by the lateral electrical field).

When the drain is close to the source, the drain bias can influence the barrier as demonstrated in the schematic of fig. 5.4 (pnp-MOSFET), the dashed curve describes the barrier lowering effect in a short channel and the unbiased situation, respectively. For a the long-channel device the drain bias can change the effective channel length, but the barrier at the source contact remains constant. The threshold for the inversion of the charge carriers will be reduced.

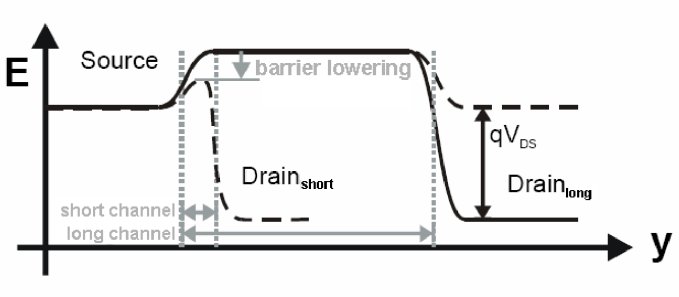


Figure 5.4: *Energetic band devolution of a pnp-semiconductor channel. The barrier height at source is reduced effectively in a short channel, when a positive drain voltage is applied. The dashed curve describes the barrier lowering effect in a short channel and the unbiased case in the long channel, respectively.*

The situation in OFETs is again a case differentiation of the contact type. In the case of an ohmic contact with holes accumulated at the metal-semiconductor interface there is basically no barrier for hole transport. The influence of the longitudinal field is the reduction of the effective width. In a Schottky-type contact one will always end up with a back-to-back Schottky contact. When applying a negative voltage at drain the inverse sign case to fig. 5.4 will occur and the drain induced barrier lowering at the source will result. An exception is the exact matching of Fermi level E_F in metal ($\approx \Phi_m$) and semiconductor, where there is no SCZ.

The DIBL results in a dependence of V_{TH} on the applied electrical field in the channel E_{long}, which is equivalent to $V_{TH} = V_{TH}(V_{DS})$. The larger $|V_{DS}|$, the more V_{TH} will be reduced (shift to more positive values for p-type). Again this effect can be used to evaluate the contact but due to the superposition of the effects a separated investigation is always difficult.

The channel length modulation (CLM)

Whereas the effects described before already occur at low bias, the CLM is an effect which may occur when the drain source voltage is beyond pinch-off $V_{DS} \geq V_{DSsat}$. The effect is illustrated in fig. 5.5. The SCZ at the drain expands into the channel, induced by the high electrical field in the saturation region. The channel length is reduced effectively. The CLM is the consequence of the invalidity of the Shockley approximation (cf. 4.3.1). The effect is characterised by a V_{DS} dependence of the drain current I_D in the saturation

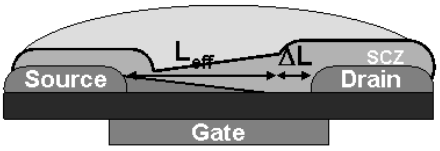


Figure 5.5: *The effective reduction of the channel length due to the expansion of the space charge zone at drain in the saturation regime.*

regime. Assuming a linear relationship [102], the behaviour can be described by

$$I_D = I_{Dsat}(1 + \lambda V_{DS}) \tag{5.16}$$

where λ is the CLM parameter of dimension V^{-1}. A graphical determination (fig. 5.6) can be achieved by backward extrapolating the linear increasing saturation current at different values of V_{GS}. The intersection with the abscissa gives an *early voltage* V_{early} which is related to λ as

$$V_{early} = -\frac{1}{\lambda}. \tag{5.17}$$

The illustrated ΔI_D in fig. 5.6 is used to give a quantitative definition of the CLM

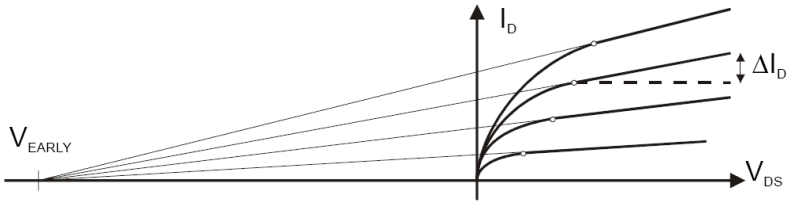


Figure 5.6: *Channel length modulation effect on a field of output characteristics TFT device.*

$$\Delta I_D(V_{DS}) = I_D(V_x - I_D(V_{DSsat})). \tag{5.18}$$

V_x is the channel voltage used to compare the short channel device with a long channel device and V_{DS} is the point of pinch-off as defined in equation (4.12). With this definition and in case of a linear relationship the value for ΔI_D should be the same for all V_{GS}.

The punch through (PT)

The punch through is a notion for a stronger than linear increase of the drain current with increasing drain-source voltage. The increased electrical field leads to overlapping SCZ at the contacts and the current can 'punch through'. In this context the PT is only limited to the channel and not to an insulator break through. Therefore, it is a non-destructive effect and reversible. The modulating effect of the gate voltage is strongly reduced.

The current voltage behaviour in the PT-regime can be described by means of the *space charge limited current* model (SCLC). It describes the injection of charge carriers in different solids [103]. The Mott-Gurney equation theoretically describes the injection from one to the other infinitely large ohmic contact through an intrinsic semiconductor of thickness L. The current density j is given by

$$j = \frac{9}{8}\epsilon\epsilon_0\mu_{SCLC}\frac{V^2}{L^3} \tag{5.19}$$

where ϵ_0, ϵ, μ_{SCLC} describe the dielectric constant, the relative permittivity of the semiconductor, and its mobility, respectively. The SCLC is also used to describe the current in MOSFETs and TFTs which show PT [102, 104, 105]. The behaviour is diode-like. In reference [106] the following relation between V_{DS} and I_D is established for SCLC in a film:

$$I_D = -0.6\epsilon\epsilon_0\mu_{SCLC}W\frac{V_{DS}^2}{L^2}, \tag{5.20}$$

where ϵ_0, ϵ, μ_{SCLC} describe the dielectric constant, the relative permittivity of the OSC, and its mobility, respectively. With this equation a comparison of mobility values in short channel and long channel devices is possible.

The final figure of this chapter presents the influence of the different effects characterising a short-channel behaviour on the IV-characteristic of a TFT. The top diagrams (a) and (b) show the idealised transfer and output characteristics, respectively, of a long-channel TFT and (c) and (d) the corresponding diagrams for a short-channel device. In the long-channel device the subthreshold regimes are equal under variation of V_{DS} and V_{TH} is constant. The DIBL and the SCE introduce an increasing current dependence with increasing V_{DS} and a shift of V_{TH} towards 'open channel device' for increased V_{DS}. Another effect in the short channel is an increased channel leakage, which results in an increase of the minimum off-current which decreases, following 5.1.3, the on/off-ratio in the device. The output characteristics of the short-channel device diagram (d) mirror the CLM resulting in PT at increased $V_{DS} = V_{PT}$. The break down voltage V_{BD} defines the limit of the irreversible drain to substrate break down of the dielectric due to charge carriers of high energy by avalanche ionisation.

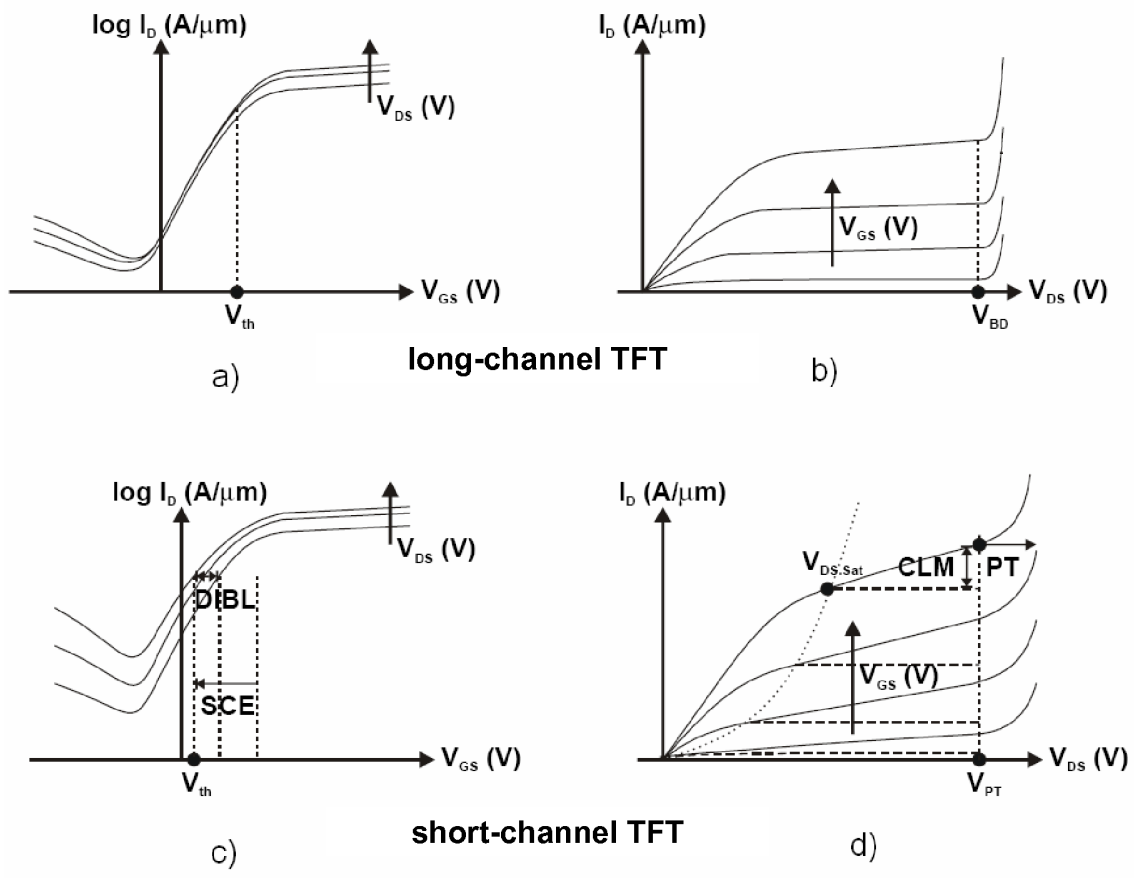


Figure 5.7: *Schematic of model TFT characteristics of a long- and short-channel device. Overview of the effects of oncoming short channel behaviour.*

Chapter 6

Electrical characteristics at room temperature

The focus in this work lies on the experimental analysis and interpretation of transport properties in organic semiconductors depending on the morphology. Therefore, different types of organic semiconductors are investigated. The notion "type" is defined by the morphology, which in turn (e.g. for the tetrathiafulvalenes) is controlled by the deposition method. The transport properties are derived from the performance of the OFETs in which the organic semiconductor acts as the active layer. For each investigated material it is necessary that the high quality of device properties is guaranteed. This allows to attribute the results directly to the material by excluding the limiting effects of the device itself.

This chapter presents the optimised output of devices with the different investigated active materials. The characteristics are modeled by the theory developed in chapters 3 and 4. The main parameters are all extracted at room temperature. Long channel devices are employed with micrometer range channel lengths up to a limit of L = 100 μm. The OFET results for sub-micrometer channel length will be presented in chapter 9.

The "testing platforms" are commercially acquired Si-wafer with a thermally grown SiO_2 layer of a defined thickness d_{ox}. They are lithographically structured with metal (evaporated or sputtered) source and drain electrodes and a common backside gate contact (the highly n-type doped Si-wafer). Furthermore the template fabrication is standardised in order to guarantee the same starting configuration for the various materials. The standard lithography process is described in appendix B. The principle device setup has already been presented in chapter 4 (cf. the picture in fig. 4.1). Before the deposition of the organic semiconductor the SiO_2 surface is usually pretreated with a silane compound in order to clean the surface and to homogenise it with a self assembled non polar monolayer. This optimisation procedure by pretreatment steps is described in appendix C. In this chapter, the resulting best pretreatment process (in terms of transport properties) will just be denoted for the different materials. In the finalising step the organic material is deposited using the

specific method (cf. appendix A). For the polymer material polytriarylamine this includes a special annealing step, which will be addressed to in the relevant subsection.

If not mentioned differently the characterisation is done in ambient air and in the dark shortly after the finalising steps. Additionally to the output in the optimised devices the chapter will present the characteristic scaling behaviour of the key device parameters. This is a pre-stage for appreciating the additional scaling effects which occur for channel lengths down to the sub-micrometer regime (chapter 9). Hereby, the limiting influences of the contacts can be estimated as presented in section 5.2, as well as an oncoming short channel behaviour specifies the requirements concerning the device architecture (e.g. the reduction of the oxide thickness). Moreover ageing and/or environmental effects on some of the investigated materials will also be addressed. This is the subject of the last section of this chapter. Here, the focus lies on the comparison of solution processed single crystals and their vacuum deposited variants. A more detailed investigation of stressing effects for vacuum–deposited materials will be presented in chapter 8 dedicated to *in situ* electrical characterisation in the organic molecular deposition chamber (OMBD, cf. appendix A).

The order of presentation of the various materials follows the crystalline order of the organic semiconductors: from (i) single crystal organic materials, the solution processed tetrathiafulvalenes (by drop-cast deposition), over (ii) vacuum deposited polycrystalline films, the OMBD processed dibenzene- and dithiophene-tetrathiafulvalene and $\alpha\alpha'$-dihexylquaterthiophene to (iii) the amorphous solution processed polymer (spin cast deposition) polytriarylamine.

6.1 Single Crystalline: drop-cast tetrathiafulvalenes

The applied drop-cast from solution method of tetrathiafulvalene material combines the convenience of solution processing of the active layer material with the high-quality electronic transport properties of organic single crystals (OSC). Both dithiophene- and dibenzene-tetrathiafulvalene (DT- and DB-TTF) are dissolved in a polar solvent. For reasons of uniformity the presented results will address only to solutions in toluene. They consist of about 1 mg of material in 10 ml toluene. The deposition is done using a small amount (≈ 0.03 ml for a wafer of area of 1×1 cm^2) of the solution and drop-casting it onto the silane pretreated wafer which is structured with electrodes. The droplet of solution covers the wafer and the evaporation process is extended to about 3 h by covering the sample in a Petri dish. The whole process is carried out in the cleanroom in order to prevent impurities from entering into the solution during the crystallisation phase. The resulting morphology is presented in fig. 6.1. The two top micrographs show the overview (left) and a single crystal on a titanium/gold electrode structure (right) for the DT-TTF, the bottom two micrographs the overview and a detailed image of DB-TTF crystals on an unstructured substrate surface (without electrodes).

The overview micrographs show that several 100 μm size crystals are formed randomly distributed on the surface. The generally higher coverage of crystals, formed near the edges of the wafer, is due to the evaporation process of the polar solution on the non-polar (silane treated) surface. During the elongated evaporation process a higher concentrated solution settles at the edges. The analysis of the crystal dimensions by DEKTAK-profiling gives a ratio of about 1/10 for the height to the width of the crystal in both derivatives, the length varies strongly. The width was usually 5 to 10 μm, however its variation was also large.

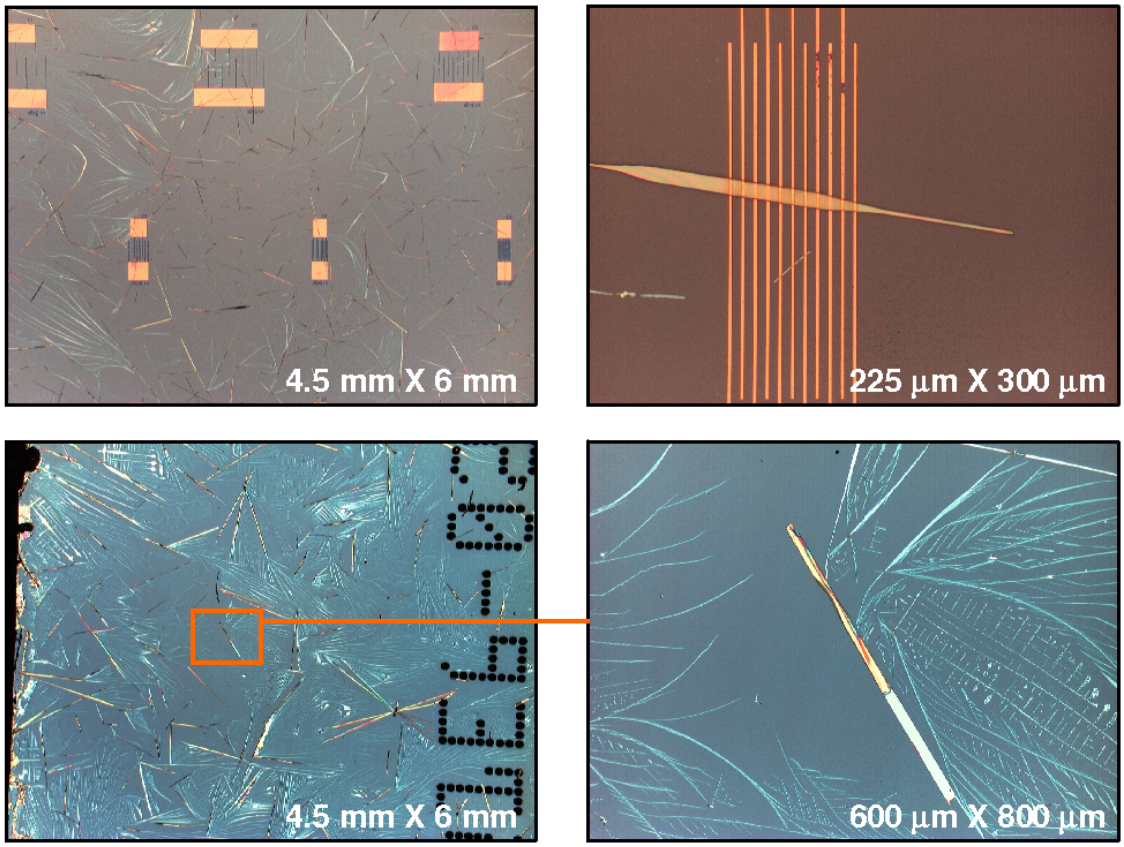


Figure 6.1: *Micrographs of tetrathiafulvalene single crystals on oxidised silicon wafers (DT-TTF, top) and (DB-TTF, bottom). Additionally, the top substrate has titanium/gold electrode structures.*

When assembling on an electrode structure, the crystals form the active layer in the OFET device. In order to analyse the material specific mobility a normalisation of the channel width according to the crystals' diameter is necessary. The effective width of the channel was determined by optical micrographs of each investigated transistor. In this way it is assured that the resulting mobility value calculated from the device characteristics is directly related to the crystalline material which forms the channel. Those electrode structures, which show by optical microscope inspection no organic crystallite coverage, have a non-conducting behaviour (all currents in the off–current regime $< 10^{-10}$A)). Thus, a thin semiconducting layer can be excluded and the investigated transport behaviour is ex-

clusively attributed to the organic single crystals. This attribution is further underscored by the removal (mechanically with the testing probes) of all crystals from a formerly normally working transistor structure. Again the result is the same: a leakage current in the I $< 10^{-10}$A range and no modulating effects of an applied gate-source voltage, which means their is no field-effect. This is valid for both materials DB-TTF and DT-TTF. For reasons of completeness it is mentioned that no current flow could be induced, by replacing a beforehand removed crystal between the electrodes. It can be concluded, that the intimate contact of the organic crystal to electrode is assured during the evaporation/crystallisation process and once disconnected, it can not simply be reversed. The pretreatment of the SiO_2 with OTS and HMDS (cf. appendix C) ameliorates the transport results in the single crystals with no substantial difference between the two treatments. The following results apply for a pretreatment of the SiO_2 with HMDS.

Dithiophene-tetrathiafulvalene (DT-TTF)
The excellent qualification of DT-TTF as organic single crystalline, semiconducting material has already been pointed out in chapter 2. This fact is attributed to the increased $\pi\pi$-stacking of the fully conjugated molecules in combination with the interaction of neighbouring sulphur atoms (cf. section 2.2). In the present thesis even higher mobility values than the elsewhere reported 1.4 cm^2/Vs [25] are demonstrated.

The microscopic picture of single crystals of DT-TTF on source and drain electrode transistor structures on the right hand side in the top of fig. 6.1 shows a crystal with a length of over 200 μm and a width of approx. 10 μm width lying on the thin gold lines (19 nm gold on 1 nm titanium, Au line width 2 μm). These lines belong to the interdigitated electrode structures with large contacting pads, as presented in the overview micrograph on the top left of the same figure. The corresponding characteristics of the L = 30 μm transistor are presented in the three-dimensional plot of fig. 6.2. The voltages range from 0 V to -15 V between source and drain (V_{DS}) and from 1 V to -11 V between gate and source (V_{GS}) with the device's transfer characteristics at V_{DS} = -1 V and -15 V and output characteristics at V_{GS}-values between 0 V and -10 V with a V_{GS}-step width of -2 V. Moreover they are measured for increasing and decreasing current (back and forth, respectively) in order to monitor a possible hysteresis effect in the characteristics. The thinner blue and red lines in the plot are fits to the measured data according to the theory developed in section 4.3, which is described by equation (4.11). The geometric parameters

	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DT-TTF	30	10	33	3.65 (3.65)	1.16 (1.20)	5.1 (1.2)·10^7	-0.45 (-0.51)

Table 6.1: *Geometry and device parameters for an optimised OFET with solution processed single crystal DT-TTF. The device parameters in brackets are from the linear regime, the others from saturation.*

and the derived main device parameters are tabulated in table 6.1. The diagrams of fig. 6.3 further show the best fit to the pinch-off curve $V_{DSsat} = V_{GS} - V_{TH}$ (cf. section 4.3.2) (output characteristic's diagram (left)) and the transfer characteristics (right diagram) in

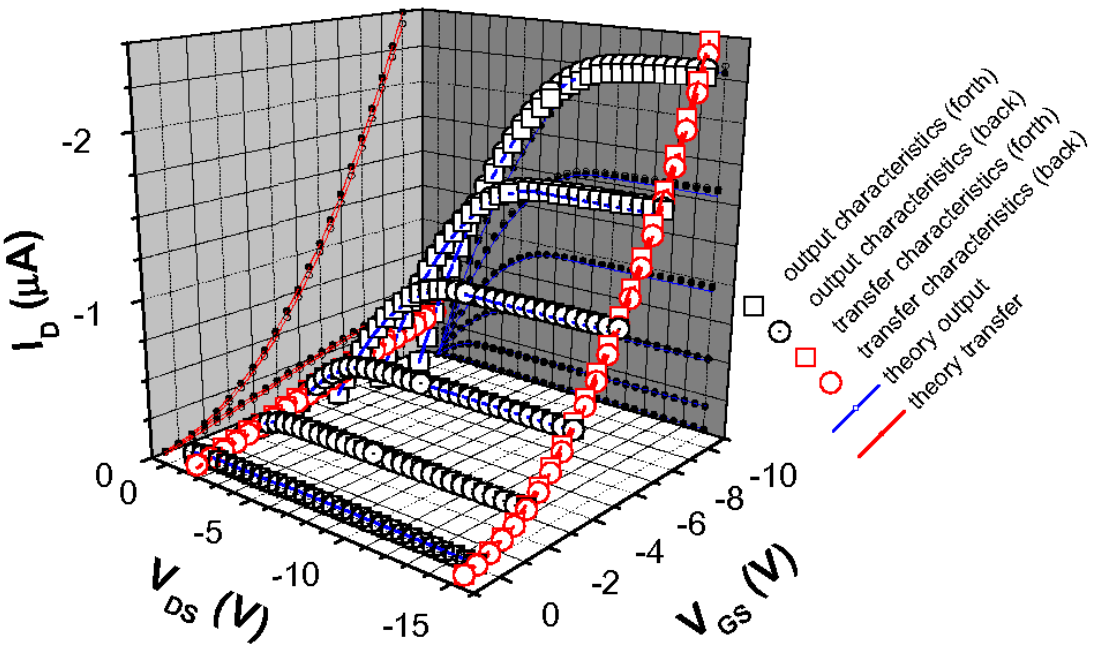


Figure 6.2: *Three-dimensional representation of the measured characteristics and best fits to the data of a single crystal DT-TTF OFET with L = 30 µm at T=295 K. The fitting follows the theory of chapter 4. The two-dimensional representation is presented by the projections to the I_D-V_{DS} and I_D-V_{GS} plane for the output and transfer curves, respectively. For the standard two-dimensional representation refer to fig. 6.3.*

logarithmic current scale in the common two-dimensional representations. It separates the linear from the saturation regime and the logarithmic representation of the transfer curves in the two regimes, linear (V_{DS} = -1 V) and saturation (V_{DS} = -15 V). The DT-TTF characteristics behave quasi-ideally following the TFT theory. The field-effect mobility derived from the transfer characteristics in the linear (V_{DS} = -1 V) and saturation (V_{DS} = -15 V) regime are in both cases 3.65 cm^2/Vs, which are the highest values reported for the DT-TTF and also - to the best of our knowledge - for a solution processed organic semiconductor. The fact that the values are identical shows that limitations by charge carrier injection or displacement currents can be neglected. They would both result in a reduced mobility in the linear regime. Again this proves the uniformity concerning the theoretic behaviour of the characteristics over the analysed voltage range. The contact resistance is estimated under the assumption of ohmic contacts (cf. section 5.2, [37]) to be approx. 30 kΩ·mm, which is rather low for OFETs.

The monitoring of the two directions shows a very small hysteresis effect of the device. The measurements are taken separately one from the other. This may explain the slightly different current values at $V_{DS} = -15$ V in the output characteristics with $V_{GS} = -10$ V for forth and back direction by a small shift (some tens of mV) in threshold voltage between

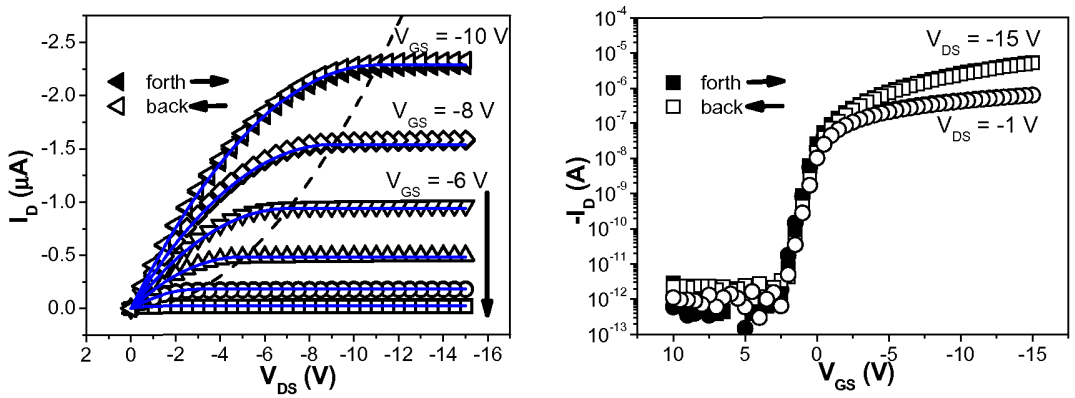


Figure 6.3: *Electrical output characteristics with best fit to the data and the pinch-off curve $V_{DSsat} = V_{GS} - V_{TH}$ (left) and transfer characteristics in logarithmic current representation (right) of a single crystal DT-TTF OFET with L = 30 μm at T=295 K.*

the measurements. The current in the saturation transfer characteristic (fig. 6.3, right) is in logarithmic scale, which conceals the small difference. However, in the subthreshold region (between V_{GS} =2.5 V and -2.5 V) and in the off-region ($V_{GS} > 2.5$ V) of the diagram a difference between forth and back direction is visible . These small effects suggest neglectable charging effect in oxide and/or semiconductor caused by impurities [107].

The results in fig. 6.4 reflect the behaviour of the analysed DT-TTF samples over the channel length range from 1 μm to 100 μm. Interestingly, the scaling behaviour of DT-TTF single crystal OFETs shows no monotonous tendency. The mobility shows higher values in the channel length regime between 10 μm and 30 μm. The effect cannot be attributed to the contact, but is rather an optimum channel length for the crystallisation on the patterned SiO_2 templates. There are only small variations between values investigated in the two different regimes and the two different current directions for all devices. For the 30 μm device, there is even nearly an ideal coincidence of all values. This is an observed tendency of the DT-TTF that the device characteristics follow ideal textbook behaviour over a wide range of operation voltages. The limits of this behaviour can be encountered in sub-micrometer channel results [26]. The small fluctuations in the investigated threshold voltage V_{TH} of the devices are below 2 V (fig. 6.4, right) and the anew lack of a clear tendency over the channel length range permits the argumentation that V_{TH} in the DT-TTF FET is rather based on pure intrinsic effects than by space charge zones at the contacts, which would manifest itself by a monotonous L-dependence of V_{TH}.
The argumentation of V_{TH} as a pure fitting parameter has been discussed in subsection 5.1.2. The apportionment by contributing charge influences as presented by equation (4.16) may still be too simplified.

Dibenzene-tetrathiafulvalene (DB-TTF)
As far as quality in device performance is concerned, the DB-TTF in general shows a less favourable behaviour of electric transport characteristics compared to the DT-TTF. The

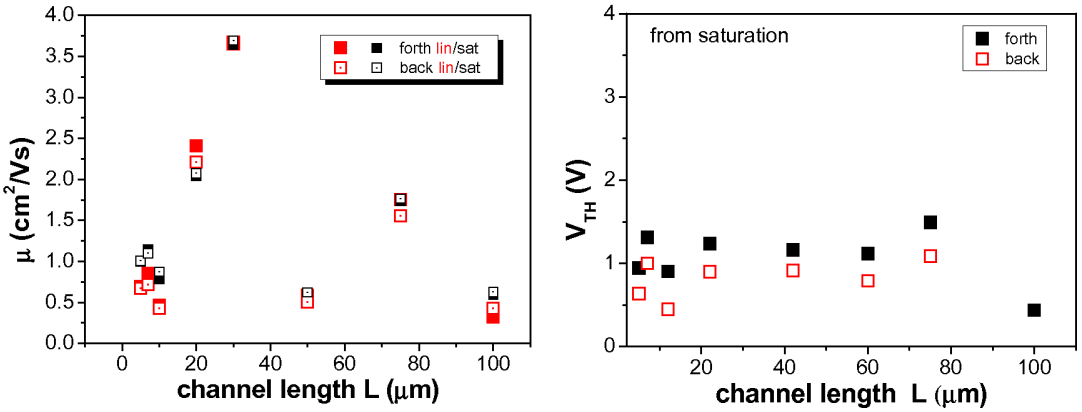


Figure 6.4: *Scaling behaviour of the mobility and the threshold voltage in single crystal DT-TTF OFETs investigated in transfer characteristics in forth and backward current sweep. Several devices on the same template with channel length between 1 and 100 μm were analysed.*

observed maximum mobility values range an order of magnitude lower than for DT-TTF. Following the argumentation in chapter 2, this can be attributed to a reduced $\pi\pi$-stacking of molecules compared to DT-TTF, due to the missing thiophene substitutes [25]. A larger variation of values also induces the interpretation of a higher statistical variation of the crystal quality. The devices are fabricated in the same way as described above for DT-TTF. The micrographs in the bottom part of fig. 6.1 show the results after the crystallisation process. The characteristics of a DB-TTF OFET with a channel length of 2 μm are represented in a three-dimensional plot in fig. 6.5. Contrary to the quasi-ideal behaviour of DT-TTF (fig. 6.2) it confirms several differences. The plots of transfer (current in logarithmic scale) and output characteristics in fig. 6.6 reveal this more clearly. The off-current depends on V_{DS}. This results in a higher on/off-ratio for the linear regime compared to the saturation regime. Moreover, the subthreshold slope is affected by the drain-source voltage V_{DS}. It has a rather elevated value of 1.8 V/decade in saturation and a better but still large value of 1.1 V/decade in the linear regime. All parameters result from the analysis of the transfer characteristics. The comparison of the measured field of output characteristics with the one calculated following the theory (blue lines) has the following results: the measured current in the linear regime is lower and in the saturation regime higher than the calculated current, and moreover increasing instead of being constant. The former can be due to the influence of the contact, the latter is an oncoming short channel effect in the L = 2μm channel device or an intrinsic ohmic charge carrier conductance superposing the field-induced charges. The larger channel devices show the same behaviour, so that it can be assumed that the effect is rather intrinsic and not a starting short channel behaviour. The device parameters are summarised in table 6.2.

The mobility derived from saturation is 0.41 cm^2/Vs. The linear region value is substantially lower with 0.24 cm^2/Vs. Under the assumption of an injection barrier the value can be corrected. This is illustrated by the dotted red line in the output characteristics diagram of fig. 6.6 (left). In the ideal case the barrier value substracts linearly from V_{DS} and

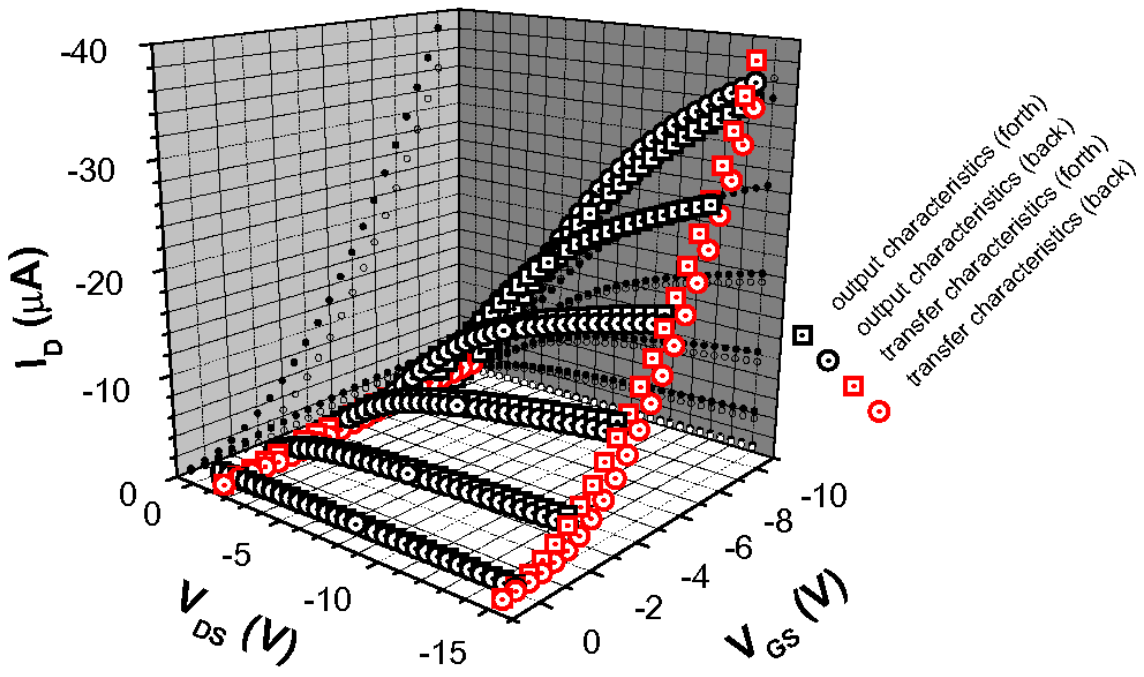


Figure 6.5: *Characteristics (transfer and output) of a DB-TTF FET in a three-dimensional representation. The channel length L is 2 µm.*

	L (µm)	W (µm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DB-TTF	2	100	33	0.41 (0.24)	1.09 (1.08)	0.8 (4.1)·10^5	-1.82 (-1.1)

Table 6.2: *Geometry and device parameters for an optimised OFET with solution processed single crystal DB-TTF. The device parameters in brackets are from the linear regime, the others from saturation.*

thus only "shifts" the output characteristics along the x-axis. In this way with a corrected effective V_{DS} (subtraction of -0.4 V), equation (4.13) from section 4.3 results in the better matching value of 0.39 cm^2/Vs. This method introduces an estimation of injection barriers with respect to the textbook behaviour under the assumption that their effects in the high V_{DS} regime (saturation) can be neglected. The determined V_{TH}-values are essentially equal (1.1 V) and thus behave comparably to DT-TTF: the switching behaviour is not influenced either by the injection barrier or the relatively small device. A typical scaling behaviour in DB-TTF was not accessible due to the large variation in performance of devices. For the temperature dependent characterisation the investigation was performed in devices of comparable quality.

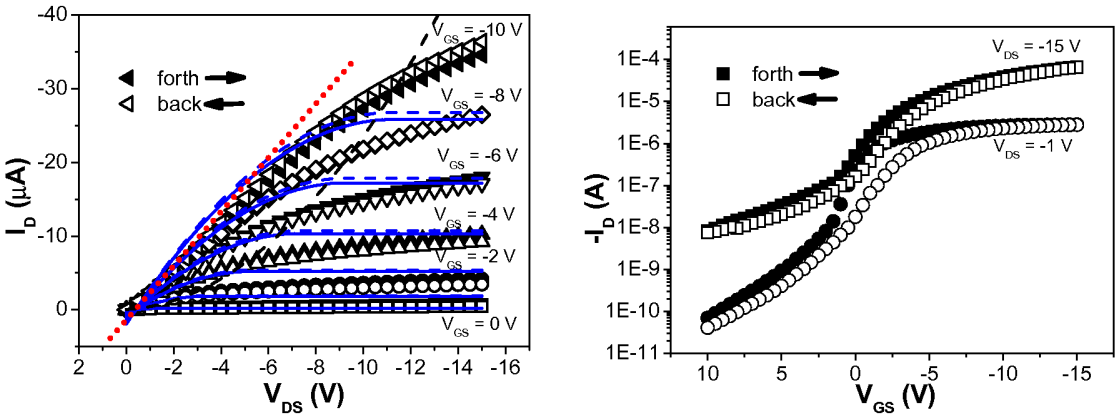


Figure 6.6: *Output characteristics and transfer characteristics of a single crystal DB-TTF OFET (cf. fig. 6.5). Here the transfer characteristics are presented in logarithmic current scale. The fitted lines in the output diagram take into account an injection barrier (red, dotted) and the pinch-off curve (black, dashed).*

6.2 Poly-crystalline: vacuum evaporated organic semiconductors

The vacuum evaporation of organic molecules is carried out in the organic molecular beam deposition chamber (OMBD) (cf. appendix A) in UHV of base pressure $1{\cdot}10^{-8}$ mbar and below. On the one hand the standard two-dimensional growth material, the $\alpha\alpha$'-dihexylquaterthiophene (DH4T) is used for comparison and further investigation of effects. On the other hand poly-crystalline films of the same TTF derivatives as in the previous section are analysed. The resulting characteristics and effects elucidate the influence of the crystalline structure and material morphology on the performance. As far as the thin films are concerned this is especially the grain boundary effect.

6.2.1 Dihexylquaterthiophene

DH4T is deposited on octadecyltrichlorosilane (OTS) treated SiO_2 surfaces (cf. appendix C, [108]). The sample temperature for a maximum mobility was optimised in former studies [40][109] to 90 °C, which is due to the phase diagram of the liquid crystal material (cf. section 2.2.2 of chapter 2). Fig. 6.7 shows the optical micrograph using a Nomarski optical setup for DH4T layers on silane-treated SiO_2 grown at 70 °C and at 90 °C, respectively. Both samples have a nominal height of 12 nm, measured during growth by a calibrated micro balance. The Nomarski optical principle is the differential interference contrast (DIC). It illustrates minimal height differences. Thus, the large domains in the 90 °C sample can not directly be connected to domains of similar crystalline ordering, they represent terrasses of similar height. Together with the electrical transport proof [40][109]

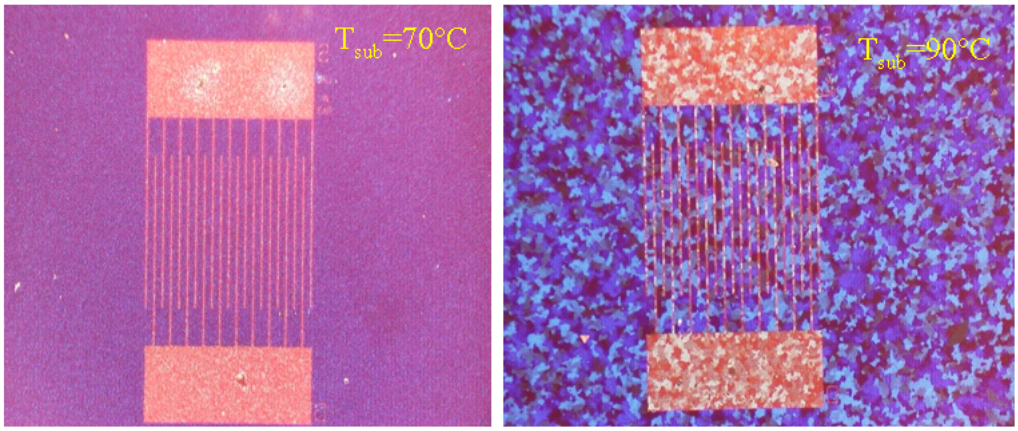


Figure 6.7: *Optical micrographs of DH4T layers of the same layer thickness (12 nm) grown at 70 °C (a) and at 90 °C (b). The domains of different colour are effects of the differential interference contrast by a Nomarski optical setup and represent terrasses of different height.*

this indicates an increased long range ordering compared to the 70 °C sample. A further confirmation is the atomic force micrograph in the bottom of fig. 2.2, which shows the μm-size terrace of height in the molecular scale.

The electrical characterisation of the material reflects the resulting two-dimensional thin film. The grain size is directly connected to the transport performance [109]. The characteristics of fig. 6.8 are taken from a device of L = 100 μm on OTS-treated 100 nm SiO_2. In section 5.2 a typical scaling behaviour of the mobility has already been presented. The mobility values decrease for smaller channel length (fig. 5.2) due to the influence of the contact resistance. The intrinsic value is thus obtained for the large micrometer size channels.

	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DH4T	100	1400	33	0.13 (0.13)	1.75 (0.92)	2.4 (0.3) $\cdot 10^5$	0.50 (0.46)

Table 6.3: *Geometry and device parameters for an optimised OFET with a thin layer of vacuum evaporated DH4T as active material. The device parameters in brackets are from the linear regime, the others from saturation.*

The mobility value of 0.13 cm^2/Vs is measured in the linear as well as in the saturation regime. All key parameters are displayed in table 6.3. The subthreshold slopes in saturation and linear regime are also comparable. They amount to 0.5 and 0.46 V/decade, respectively. There is a difference in threshold voltage measured in the linear and saturation regime (0.92 V and 1.75 V, respectively). The higher electrical field regime results in a more positive V_{TH}. The *in situ* results (in UHV) for DH4T generally show negative V_{TH},

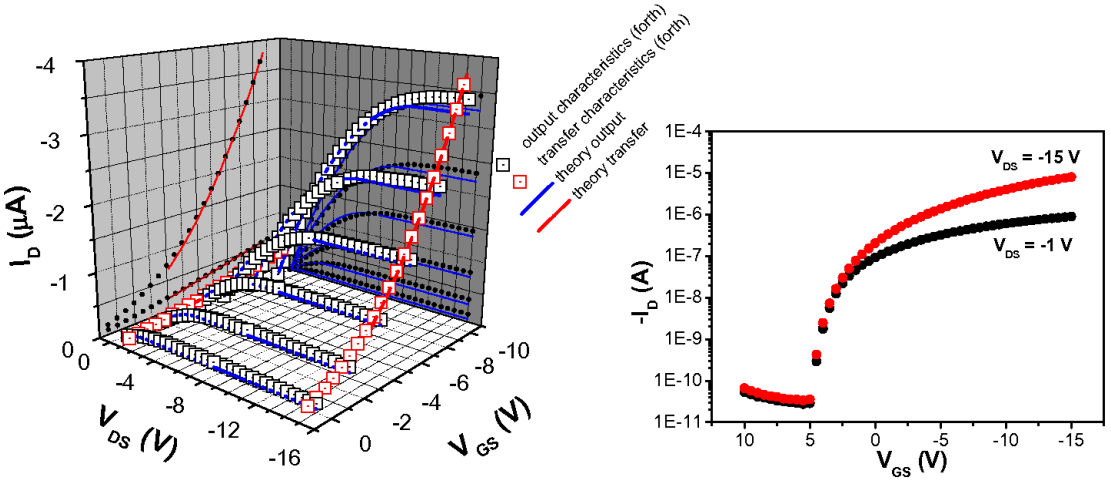


Figure 6.8: *Left: three-dimensional representation of the measured characteristics and best fits to the data of a DH4T OFET with L = 100 µm at T=295 K. The two-dimensional representation is presented by the projections to the I_D-V_{DS} and I_D-V_{GS} plane for the output and transfer curves, respectively.*
Right: the transfer characteristics in linear and saturation regime in logarithmic current scale.

therefore, the positive threshold can be attributed to an atmospheric effect on the DH4T films (most probably a p-type doping effect of oxygen on oligothiophenes [110]). The textbook behaviour is further confirmed by the lack of leakage or displacement currents. In the presented device the organic material is evaporated through a shadow mask on the transistor structures. This more elaborate deposition guarantees the absence of larger displacement currents due to the charging of the surface capacitance or any superficial leakage current (e.g. over the edges to the gate). These effects are usually impeded by mechanical isolation (after deposition in ex-situ investigations) of structures or by sealing of the edges (in *in situ* studies). They would mainly affect the low V_{DS} regime where the highest potential difference between the surface and the gate occurs. In the following chapters influences of this kind can be neglected, although a shadow evaporation is not always performed.

Besides the scaling behaviour of the mobility shown in fig. 5.2 of section 5.2, the general micrometer channel regime scaling of DH4T OFETs (all parameters from saturation) is presented in fig. 6.9. The decreasing mobility can be attributed to the contact resistance as stated before (section 5.2). The on/off ratio also reflects this influence which can be seen by the values after normalization with respect to geometry factors (divided by W/L and multiplied by 10000 for reasons of comparison). The value increases from below 10^6 to above $4{\cdot}10^6$ for a channel length below 5 μm up to 20 μm. In the third diagram (c) the scaling behaviour of the threshold voltage (left ordinate) and the subthreshold slope (right ordinate) are plotted together. The scaling is comparable: with increasing channel length, the threshold voltage V_{TH} develops to more positive values (open channel) and S becomes smaller (enhanced switching). This suggests an increased influence of the contact with respect to the grain boundaries or other trapping effects in the film and no oncoming short

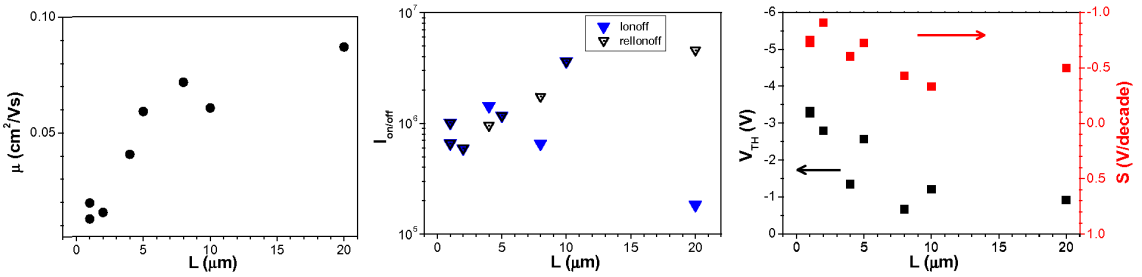


Figure 6.9: *(a) Scaling of the mobility, (b) of the on/off-ratio (as measured (blue, full triangles) and divided by $W/10^4 \cdot L$ (open triangles)), (c) and scaling of the threshold voltage and subthreshold swing from OFETs of DH4T in the micrometer channel range determined in the saturation regime.*

channel effects, in which case the opposite trend would be expected (cf. 5.3).

6.2.2 Tetrathiafulvalenes

In addition to the characterisation of the single crystal TTF material (by drop-cast, 6.1) the two materials DT- and DB-TTF were also investigated in their UHV evaporated variant. This allows interesting aspects of comparison.

The standard characterisation discussed here reflects the different morphology of the evaporated layer compared to the single crystals. This part of the chapter is based on quite an extensive investigation of the growth mechanism of DB-TTF on SiO_2 substrates. It is presented in appendix D accompanied by a morphological study (AFM and Nomarski microscopy). The optimisation of the electrical transport properties in correlation between transport and morphology was achieved with respect to the structural analysis made in this study (for details see also [111]). For the DT-TTF a cross-check with the behaviour of the evaporated DB-TTF was performed. A similar behaviour was found and consequently the same growth conditions are chosen.

Contrary to the dihexylquaterthiophene, the TTF-materials show a Vollmer–Weber growth mechanism in their vacuum deposited variant. This is verified on polar (cleaned in H_2O_2/H_2SO_4 (1/4), rinsed in water) and non-polar OTS-treated (cf. appendix C) SiO_2. The non-polar surface results in a more homogeneous growth of the material, whereas the polar surface tends to a more pronounced formation of islands/clusters. This is presented for the DB-TTF in the overview micrographs of fig. 6.10. The behaviour is confirmed by the AFM data (cf. appendix C). The electrical characterisation reveals a stabilising effect of the OTS-treatment for both materials, which manifests itself by textbook-like characteristics and a mobility enhancement of a factor 10 - 100.

The characteristics of the two materials on OTS-treated SiO_2 are shown in fig. 6.11.

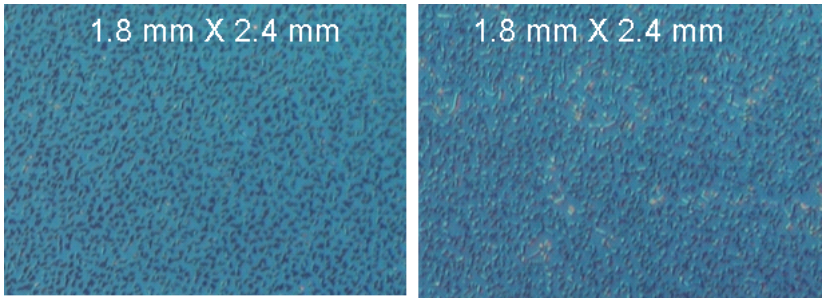


Figure 6.10: *Nomarski optical micrographs of DB-TTF vacuum evaporated on OTS-treated (left) and piranha-cleaned SiO_2 (right).*

The growth parameters follow the optimisation process described in appendix D. The substrate temperature during growth is room temperature and the flux is low $\sim$ 1 nm/min. This is a compromise between the formation of new nucleation centres which favour the poly-crystallising of the film and the piling up of the material which favours the three dimensional growth mechanism. The presented characteristics are from transistors with L = 20 μm in both cases. They nicely follow textbook behaviour. The mobility and other main device parameters are shown in table 6.4. μ is reduced by more than one order of magnitude compared to the single crystal results of 6.1. The saturation values are 0.039 cm^2/Vs and 0.066 cm^2/Vs for the DB- and the DT-TTF, respectively. The linear values behave comparably to the single crystalline result. Whereas in DT-TTF the value matches with 0.068 cm^2/Vs, the corresponding value for DB-TTF is reduced (0.023 cm^2/Vs). When applying the same correction as above, by the assumption of an injection barrier of -0.4 V, the result is 0.038 cm^2/Vs which is nearly the exact saturation value. Indeed, the output characteristic allows a correction in this way. DT-TTF has a negative threshold voltage and the series of values from linear and saturation regime differs from the situation investigated before. With -1.23 V the value from the linear regime is more positive compared to the saturation value. The shift is visible in the transfer characteristics and can be confirmed for all devices on the sample with L $\geq 7\mu$m (see fig. 6.12). In the DB-TTF FET the threshold is extremely positive 4.75 V in saturation and 4.5 V in the linear regime. When addressing

	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DB-TTF	20	$2{\cdot}10^5$	66	0.039 (0.023)	4.75 (4.50)	1.4 (0.1) $\cdot 10^7$	0.30 (0.33)
DT-TTF	20	2000	33	0.066 (0.068)	-1.57 (-1.23)	2.0 (0.1) $\cdot 10^7$	0.22 (0.13)

Table 6.4: *Device parameters from optimised OFETs with evaporated layers of DB- and DT-TTF. The device parameters in brackets are from the linear regime, the others from saturation.*

the scaling behaviour of the device parameters more closely the two materials show a similar developing of their parameters with channel length. The results are compared to each other in fig. 6.12. The top diagrams present the scaling behaviour of the mobility in both regimes (linear and saturation). For DB-TTF the values for a channel length of L = 5 μm and above are nearly constant in the order of the L = 20 μm device of fig. 6.11 and table 6.4. For channel lengths below 5 μm they increase. A difference between linear and saturation mobility as mentioned above is present in all devices. It additionally increases for the smaller channels. For DT-TTF a larger range of L is investigated (up to L = 100 μm).

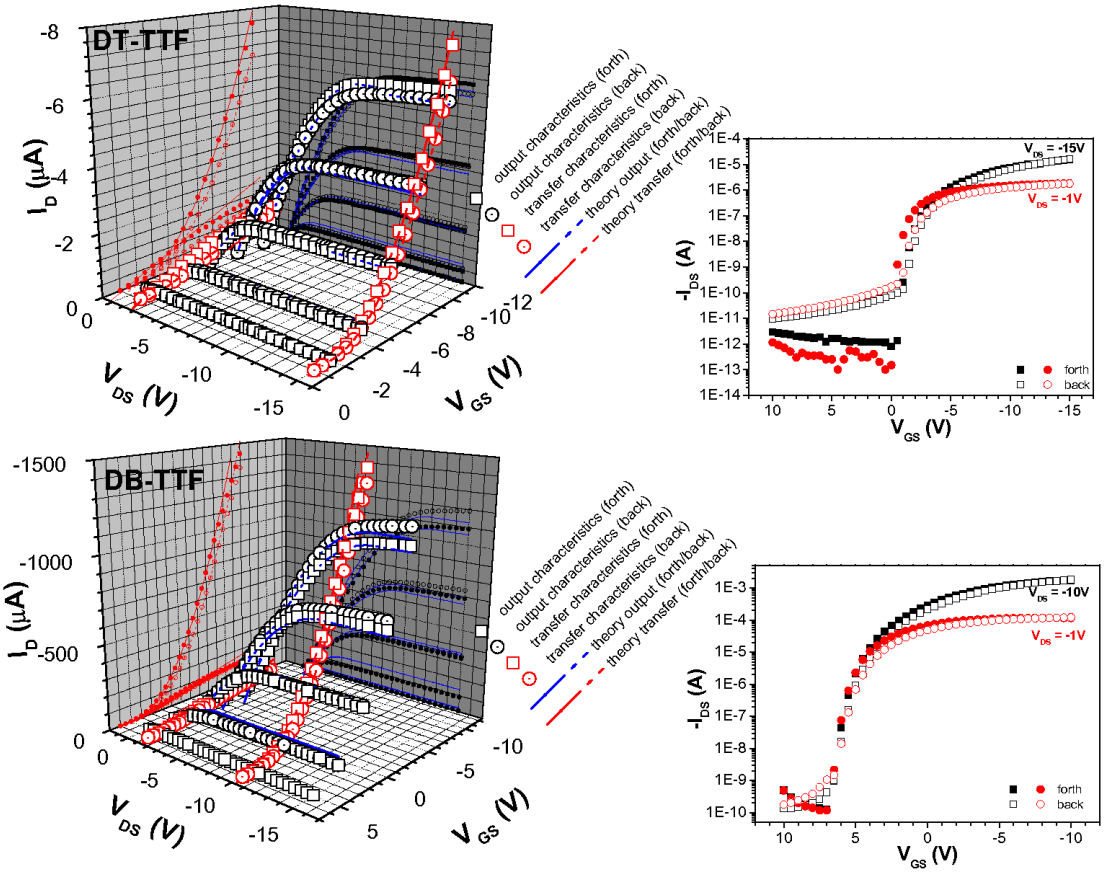


Figure 6.11: *Characteristics (output and transfer) of DB- (top) and DT-TTF (bottom) in a three dimensional representation. The symbols represent the experiment, the lines are fits to the data according to textbook models (cf. chapter 4).*

The behaviour is the same as for DB-TTF. Here, the mobility increases for L $\leq 5\mu$m and subsequently stays at the same level. However mobility values from linear and saturation regime match down to L = 7 μm. Then they diverge in favour of a higher saturation value. The latter as well as the supplementary difference for the small DB-TTF channels can be interpreted as an oncoming effect of short channel behaviour. The enhanced lateral electrical field in saturation contributes to the mobility. The general increasing behaviour below a certain channel length is in contrast to the results observed for DH4T. This may be caused by a channel length in the range of the grain size. The evaporation process indeed results in micrometer size grains that grow together. However, in comparison with DH4T the average layer height is enhanced by a factor of ten and beyond for a complete and dense film (12 nm for DH4T compared to $\sim$150 nm for DB-TTF, cf. appendix D), which will also introduce bulk effects when decreasing the channel. The general behaviour of the threshold voltage and the subthreshold slope are identical in the two evaporated materials. However the shift of both parameters is much more pronounced in the DB-TTF layers, which can be identified by the different scaling of the ordinates in the mid diagrams. For DT-TTF the range of S- and V_{TH} values is as narrow as 0.2 V/decade and 4 V, respectively, when varying the channel length between 1 μm and 100 μm. For DB-TTF the range is as

high as 1.6 V/decade and 5 V, respectively, already when considering a smaller variation of channel length. When the channel lengths decrease the subthreshold swing becomes larger and the threshold voltage more positive. In section 5.3 the channel length dependence of V_{TH} is expressed by equation (5.14). The explanation is the increasing influence of space charge zones (SCZ) in the devices that shorten the channel. Additionally, it can be influenced by the drain induced barrier lowering effect (DIBL), where the shift of V_{TH} is induced by the lateral electrical field. At least the contribution of DIBL is confirmed by the stronger shift in V_{TH} from the saturation (higher field) region. The similar devolution in S is connected to the increasing off-current for smaller channels. This is displayed in the two bottom diagrams. Big triangles represent the on/off-ratios (left ordinate) adjusted to the geometry influence found in the devices, the corresponding on- and off-current values are also plotted (right ordinate). Below L values of 10 μm and 20 μm the DB-TTF FETs strongly reduce in on/off-ratio, which is caused by an increasing off current. Ideally, the off-current should be independent of the channel length, but this is not the case for both materials. However all off-currents in DT-TTF are below 10^{-10} A, which as a whole results in a high on/off-ratio for DT-TTF FETs in the investigated range.

From this it follows that the main difference compared to DH4T is induced by oncoming short channel behaviour. Interestingly, in the DB-TTF transistors the thinner oxide (d_{ox} = 50 nm) is applied compared to the DT-TTF and DH4T (d_{ox} = 100 nm). The layer by layer deposition in DH4T also results in reduced grain-boundary effects. The effect of the contact resistance thus is not dominated by grain boundary effects. Such a domination of the grain boundaries on transport can explain the scaling behaviour in the TTF material, where the contact resistance influence can hardly be attributed. Additionally, in yet unfinished Raman and x-ray spectroscopic studies (unpublished) at the university of Bologna a different crystalline structure compared to the single crystalline material is found in the same evaporated layers which can be a further reason for the inferior transport properties compared to the single crystal results. Further results on the scaling effects will be discussed in Chapter 9 by analysing the sub-micrometer channel length results. The indication of oncoming short channel behaviour in the micrometer channel length range, especially in the evaporated DB-TTF films confirms the need for an adaption of the vertical electrical field by an increased gate capacitance.

6.3 Amorphous: polytriarylamine

The polytriarylamine (PTAA) material is deposited via spin cast deposition from solution of toluene. The best results on SiO_2 templates are obtained when using an OTS-pretreatment step. The resulting contact angle beyond 90°, however, can cause dewetting problems of the solution. Usually the spin cast films at 1000 rpm, which are not affected by this issue, are of a thickness of 150 nm $\pm$ 40 nm (by DEKTAK analysis). An optical micrograph of a metal transistor structure on SiO_2 with PTAA is shown in fig. 6.13. The layers undergo a 10 min phase of relaxation and a one hour annealing at 100 °C, before the char-

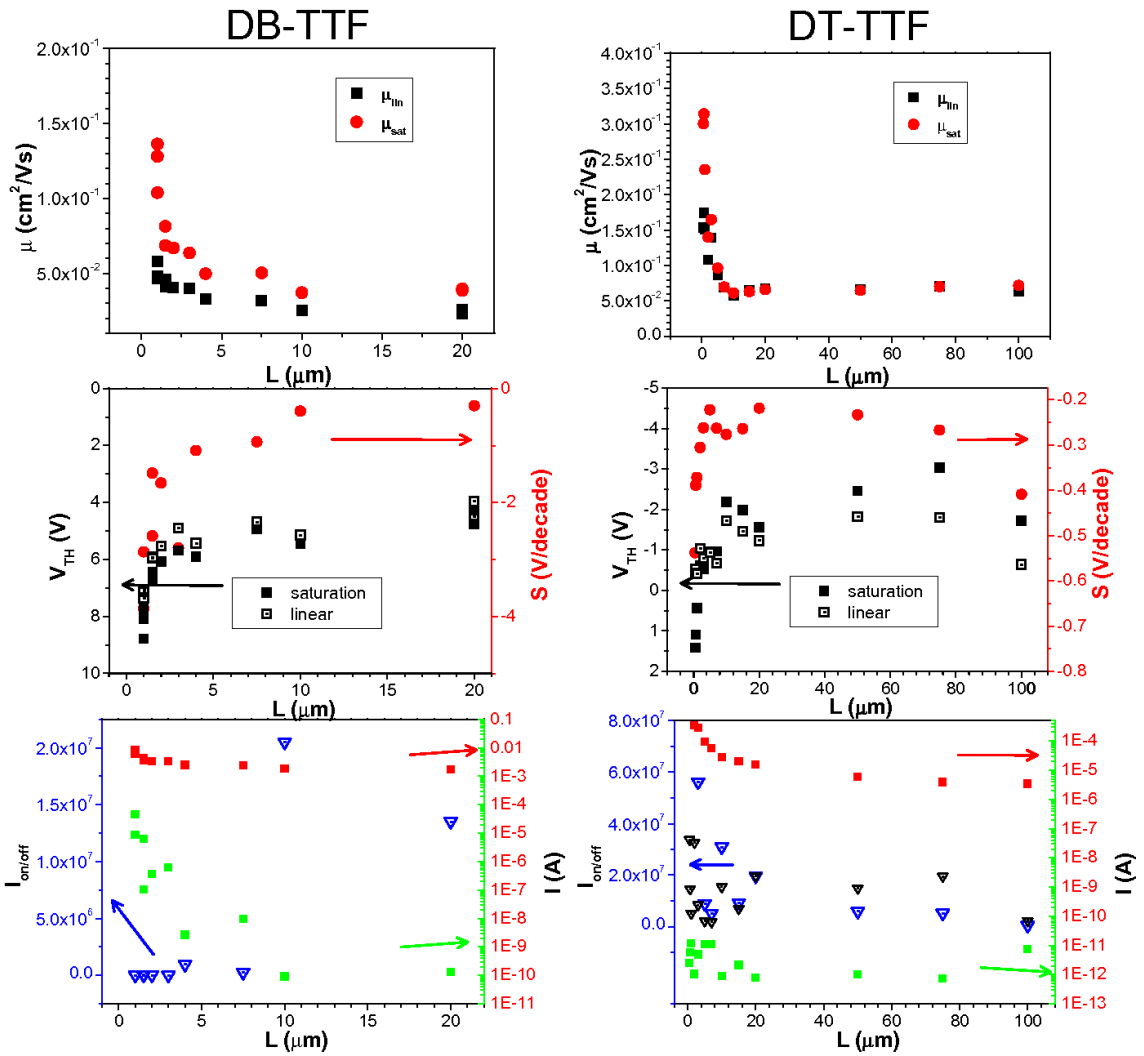


Figure 6.12: *Mobility, threshold voltage, on/off-ratio and subthreshold swing from OFETs of DB- and DT-TTF in the micrometer channel range.*

acterisation. This process induces the removal of remaining solvent and the cross-linking of the amorphous polymer and results in a better performance of the devices.

The PTAA is dissolved in toluene (1 wt%, see fig. 2.7 for the structural formula). The material is optimised for the use in plastic electronics, thus, in combination with an organic dielectric [45]. The higher mobility results from using non-polar dielectrics. The use of SiO_2 as a dielectric is reported to result in a lower mobility compared to lower k organic dielectrics [46]. However, our results show a good transistor behaviour and a mobility in the order of 10^{-3} cm^2/Vs, which is one order of magnitude higher than the reported maximum mobility [45, 46] in case of SiO_2 dielectric. An example of PTAA FET characteristics is presented in fig. 6.14 and the resulting device parameters in table 6.5. The mobility in the device is about $4 \cdot 10^{-3}$ cm^2/Vs. The value from the linear regime results higher compared to the saturation value. The two values for the threshold voltage also vary

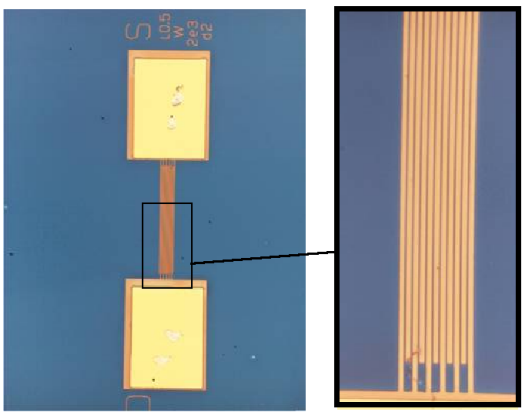


Figure 6.13: *Micrograph of a polytriarylamine (PTAA) OFET and inset. The channel length is 500 nm, channel width is 2 mm. The PTAA is homogeneous and covering the whole sample.*

by more than a factor 2 (this time linear is smaller compared to saturation). The origin of both differences lies in the fitting, due to a deviation from textbook behaviour of the saturation curve around V_{TH}. This may be related to the isotropic conductance of the material which will favour perpendicular current injection at higher V_{DS} controlled electrical fields at low V_{GS} (no or reduced accumulated charge carrier in the channel) due to the better vertical contact from spin-casting the material. The fact that V_{TH} is more positive in the saturation regime indicates the influence of the electrical field. The on/off-ratio follows the increase of the on-current in saturation, which is not accompanied by an increase in off-current (e.g. due to leakage). The latter is also represented in the scaling behaviour of the on/off-ratio, on-, and off-current (fig.: 6.15 (c)). The low subthreshold slope of -0.23 V/decade for both regimes is already visible in the logarithmic plot of fig. 6.14. There the differences in forward and backward curves are placed electrically around the threshold voltage. This indicates charging, which takes effect on the dynamic behaviour of the characteristics. The following discussion of the scaling behaviour of the device parameters includes the behaviour of the parameters derived from forward current and backward current transfer characteristics as well as from the linear and the saturation regime.

	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
PTAA	10	10^5	66	3.39 (4.77) 10^{-3}	1.85 (0.73)	74,3 (6.3) 10^4	-0.23 (-0.23)

Table 6.5: *Device parameters from an optimised OFET with polytriarylamine from solution of toluene. The device parameters in brackets are from the linear regime, the others from saturation.*

The scaling behaviour in the micrometer range is represented in fig. 6.15. The mobility behaviour varies depending on the applied V_{DS}. In the linear regime a comparable result to the thin layer results of DH4T is achieved. The decrease of the mobility with decreasing channel length can be directly attributed to the contact resistance. The results from the saturation regime, however, increase with decreasing channel length so that for $L < 5$ μm the two differently derived values of mobility diverge from each other. An explanation follows the above mentioned high electrical field in saturation that contributes to transport by an increase of bulk effects in the layer (10 times thicker than DH4T). Additionally there is no

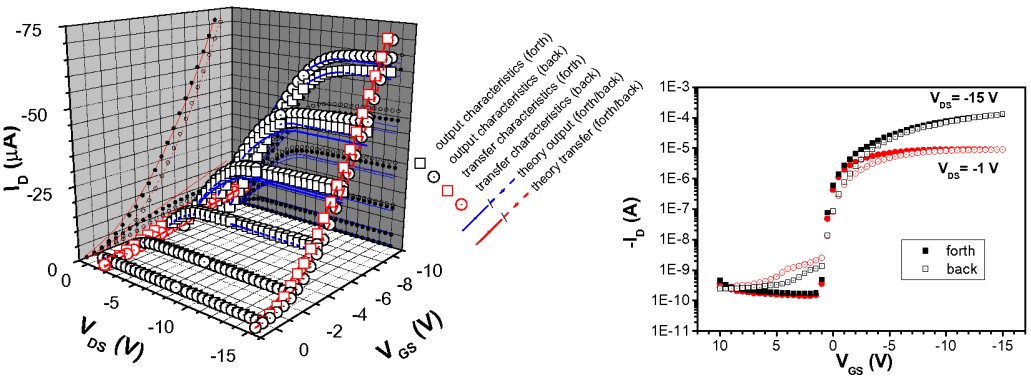


Figure 6.14: *Left: Three-dimensional representation of the measured characteristics and best fits to the data of a PTAA OFET with L = 10 µm at T=295 K. The fitting follows the theory of chapter 4. The two-dimensional representation is presented by the projections to the I_D-V_{DS} and I_D-V_{GS} plane for the output and transfer curves, respectively.*
Right: Standard plot in logarithmic current scale of the transfer characteristics of the same OFET.

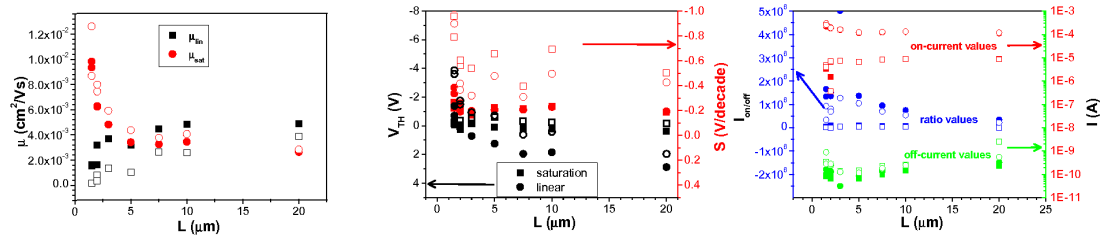


Figure 6.15: *The scaling behaviour of the mobility (a), the threshold voltage (b)(left axis), the subthreshold swing (b) (right axis), and on/off-ratio (c) (with corresponding behaviour of off- and on-current) from OFETs of PTAA in the micrometer channel range. The electrical parameter values are derived from linear (squares) and saturation (circles) transfer characteristics and both in forward (plain symbols) and backward (open symbols) voltage direction.*

conductance anisotropy in the amorphous polymer. A high field induced increased vertical injection from the contact into the bulk semiconductor is probable. However the extracted mobility in the linear regime for channel lengths larger than 5 μm is higher than the corresponding saturation value. The principle curve is confirmed for the backward values. The differences can be attributed to the differences in transfer curves as in fig. 6.14, which then are translated by fitting the data. Regarding the scaling behaviour of the threshold voltage the mid diagram of fig. 6.15 shows a reduction of V_{TH} for decreasing channel length. Here the saturation values are more positive compared to the linear values and also the backward values compared to the forward. The subthreshold slope increases (more negative values) also for smaller channels, which is in agreement with the DH4T results. There are nearly no differences between saturation and linear values, but the backward values result higher, which is attributed to charging effects when turning off the device. In the third diagram the values of the on/off-ratio and corresponding on- and off-currents are plotted against the

channel length for a constant W/L-ratio. The latter should give the same current level in on-status. Therefore, the scaling in the linear regime is nearly constant, but the increase in the saturation for decreasing channel length is an indication for bulk and/or electrical field effects in the smaller channels. The behaviour is confirmed for both current directions.

Another interesting aspect of the material is its use in a lithography process, where the PTAA film can be lithographically structured using etching or lift-off methods. It indicates the high manufacturability and robustness in different chemical environment of the PTAA thin films. The methods and effects of the treatments on the transport properties will be described in detail in chapter 10.

6.4 Ageing and environmental effects on devices

With regard to a possible use in applications the stability of organic semiconductors is the critical aspect besides the general transport properties. Degradation due to ageing or environmental (chemical) effects are detrimental in organic electronics [112]. A general overview would go beyond the scope of this work. It would include the complex chemistry of organic semiconductor materials and the isolation of all possible affecting effects. In a beneficial consideration it would be possible to exploit these effects if they could be separated. There is a growing interest in sensor applications based on organic materials including OFETs [113]. Usually the principle is simple, e.g. based on the change of a device parameter monitored by electrical measurement. There are many different possibilities that apply to the different fields of application.

Therefore, the following experimental results will just open a small window of examples on the effects of the environment and/or ageing. Results of DT-TTF OFETs, which are obtained within a comparatively short term investigation (2 and 3 weeks, respectively), are investigated with respect to the differences of the single crystal material compared to the vacuum evaporated films of the material. Additionally, the reaction of device parameters of vacuum deposited DH4T OFETs in ambient atmosphere will be presented.

6.4.1 Ageing and environmental influence in DT-TTF OFETs

The investigated device parameters of the different DT-TTF OFETs are the mobility and the threshold voltage. They are decisive for a stable operation of transistors in e.g. integrated circuits. The threshold voltage V_{TH} is the separator between on and off-status of the transistor, and therefore a good example for a parameter whose change can easily be monitored by the electrical current in the OFET device. The mobility of the material is essential in each switching application as well as the subthreshold slope, which defines the possible switching speed. The DT-TTF FETs of both morphologies are measured in

air directly after fabrication. The single crystal FETs are stored in air and measured again after 2 weeks. The vacuum deposited devices are first measured in air, then are brought to vacuum (10^{-4} mbar) for two days with measurements at the beginning and at the end and then measured again directly after re-exposure to ambient. Afterwards the sample is also stored in air and measured again three weeks after fabrication.

The results on μ and V_{TH} of single crystal DT-TTF in the top two diagrams of fig. 6.16 show the change of these key parameters after two weeks. The mobility reduces by a factor of about two in the investigated devices and except for the L = 100 μm device the threshold voltage shift rates within a range of about 1 V. The bottom two diagrams of fig. 6.16 show

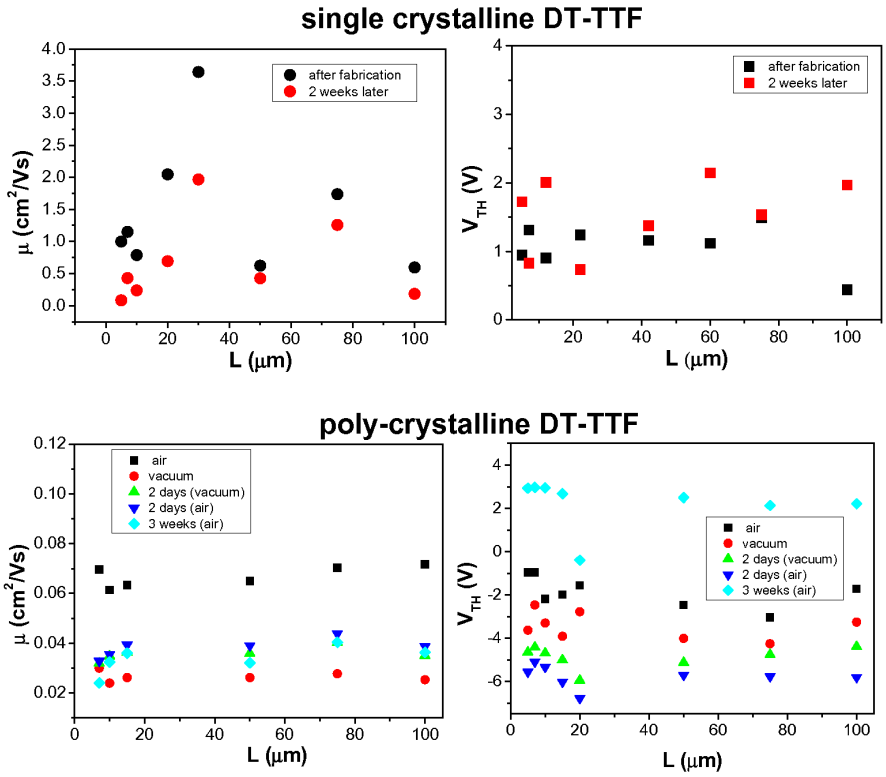


Figure 6.16: ***Top:*** *Results on single crystalline DT-TTF FETs from fig. 6.4 (forth) and corresponding mobility and threshold values of the same devices measured after 14 days in ambient atmosphere.*
Bottom: Mobility and threshold voltage values including those of fig. 6.12 for L > 5 μm OFET devices. The active layer material is vacuum evaporated poly-crystalline DT-TTF. The results compare the effects due to ageing and pumping during 3 weeks.

the situation in the devices with vacuum evaporated material. The channel length range is from 7 μm to 100 μm, which excludes the grain size effect described in the scaling behaviour of evaporated DT-TTF above (fig. 6.12). The mobility values observed in air change inconsistently within the channel length range and over the investigated period. When comparing the initial and final status (squares, normal black and 45° turned cyan, respectively) a reduction of a factor of 2 results. Only in the L = 7 μm device the reduction

is more enhanced. The range of the percentaged change is clearly lower than for the single crystals. The largest reduction of the mobility takes place during the installation of the vacuum. The reaction in vacuum (red circles, green triangle top upwards) is relatively small. It results in a reduction of the threshold voltage and a small increase of the mobility. The consequence is that the air has a positive doping effect on the mobility. However, when analysing the threshold level in the V_{TH} diagram between after fabrication in air, after 2 days in air, and after 2 weeks, the threshold decreases first but finally it increases again to a level of approx. 4 V more positive than at the beginning which usually indicates one of the following two option: a material change like an oxidation or the incorporation of ambient molecules, the latter usually at the interfaces.

Our interpretation of these observations is as follows: The DT-TTF has an increased resistivity against oxidation, compared to the bare TTF-molecule (chapter 2). The influence of atmospheric gases on the performance of organic semiconductors has been discussed a lot. The large degrading influence on p-type organic semiconductors is thereby attributed to humidity [112, 114, 115] and oxygen [112]. However, the latter is reported to have only a doping effect affecting the subthreshold region and no degrading effects in the case of OFETs with the p-type small molecule OSC pentacene [116].

Our results on mobility show a slight reduction in the case of single crystalline DT-TTF and the behaviour in the poly-crystalline material was relatively stable within the three weeks of investigation. However, in the latter case the high-vacuum environment of $< 10^{-3}$ mbar first decreases the mobility slightly followed by a complete recovery within 2 days in the vacuum. The only slight reduction of mobility in the single crystalline results allows the assumption that the stability compared to other organic semiconductors (cf. [114], and the following section) is good so that an oxidation process within the aromatic system can be excluded. Any change within the $\pi\pi$-stacking would have stronger effects on mobility. The reduction of mobility in single crystalline DT-TTF can rather be attributed to a change in the injection behaviour (contacts).

A more pronounced reaction is observed for the threshold voltage. When using the connection between trap states and V_{TH} from 5.1 the explanation for the change of V_{TH} is that trap states are filled due to the ambient atmosphere. The material is doped in the sense of a passivation of the traps. Therefore, the threshold shifts to less negative values (open channel). The trap dominated poly-crystalline DT-TTF shows exactly this behaviour, because the high number of grain boundaries facilitates the assembly of donor or acceptor atoms in these regions. The tendency within single crystalline DT-TTF is also to more positive values, but less pronounced. This makes sense regarding the reduced number of trap states compared to the poly-crystalline film.

6.4.2 Reaction of DH4T FETs in ambient air

The devolution of the characteristic in ambient air is considerable in thin layers of DH4T. Ageing effects in thiophene oligomers are known [117]. The diagrams in fig. 6.17 show the field of output characteristics of the same device measured *in situ* in UHV and after 40 days exposure to ambient air. V_{TH} has shifted about 6 V and increasing hysteresis effects appear directly after the exposure to air. The effect is one reason for the use of DH4T in an *in situ* analysis of gas influence [118]. Upon restoring the samples in UHV the effects do not 'heal' out completely. In the same way a degradation of the layer occurred. Therefore, if not mentioned otherwise all the ex situ results are achieved straight after the deposition in UHV in order to guarantee comparable results.

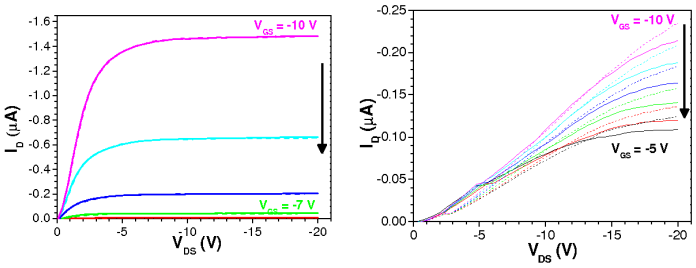


Figure 6.17: *The behaviour of DH4T output characteristics in UHV and 40 days after exposure to air.*

Chapter 7

Temperature dependent transport behaviour

The transport mechanism in organic semiconductors is crucial for an understanding of charge transport and the evaluation of the semiconductor for applications, because it reflects the effects of material impurities and imperfections, interfacial effects, and environmental influences. One way to get information about the relevant transport model (see also the discussion in chapter 3) is the monitoring of the temperature dependence of the OFET device performance parameters. In the following the temperature dependent results of the field-effect mobility μ and the drain-current I_D (more directly related to the conductivity of the material) for crystalline DB- and DT-TTFs in OFET devices are presented and discussed. This will lead to the characteristics of the density of states within the semiconductors' band gap, the so-called band tails, and the finding of energetic impurity levels by means of electrical transport measurements. In addition to the theoretical concept considerations given in chapter 3, the following sections will give an extended background and intensify the understanding of the meaning of density of states and the formation of band tails in organic semiconductors.

7.1 Density of states and band tails in organic semiconductors

The behaviour of the density of states in combination with the transport mechanism (band-like, trapping and release, hopping) defines the temperature dependence of the electrical transport. In the ideal case, the thin-film transistor is a two-dimensional device. Therefore, a simple ansatz for the two dimensional density of states $\mathrm{N}_{2D}(E)$ is used. It is defined as the number of free charges per area and per energy

$$N_{2D}(E) = \partial n_0^{2D} / \partial E$$

with $n_0^{2D} = Q/e$ the number of elementary charge units. This expression can be written as

$$N_{2D}(E) = \frac{1}{e}(\partial C_i \cdot V_{GS}/\partial E_a)$$

and

$$N_{2D}(E) = \frac{C_i}{e} \cdot (\frac{\partial E_a}{\partial V_{GS}})^{-1} \tag{7.1}$$

Under the condition of a low percentage of free (in the sense of untrapped) charge carriers [119] the distribution of trapped charge carriers in the gap can be identified by the above equation using the activation energy values, obtained from transport measurements. Butko et al calculate a percentage of only 4 % of free charge carriers in single crystal pentacene OFETs. The percentage in the solution processed tetrathiafulvalenes is thus expected to be even lower, as well as for the polycrystalline vacuum-deposited materials (section 6.2). Before explicitly presenting the experimental results, the notion of band tails will be explained.

Band tails are extensions of the density of states into the energy gap of a semiconductor. They were first observed and proposed 1953 in an early work of F. Urbach [120] by absorption spectroscopic methods. They originate from a perturbation of the bands by ionised impurities (donor/acceptor states) [121]. The randomly distributed impurities cause local interaction depending on the local density of impurities. The local energy gap remains constant, but the density of states distribution which integrates the number of states at each energy globally results as extended on both sides (conduction and valence band) into the energy gap (cf. fig. 7.1). In other words: band tailing is an effect of the lack of long range order in the material. The systems investigated by Urbach were photographic

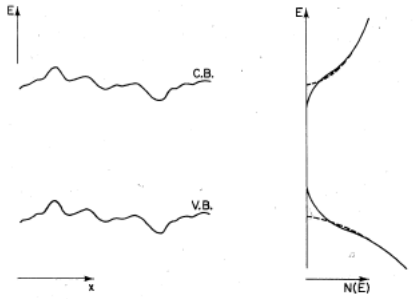


Figure 7.1: *Left: perturbation of the band edges by Coulomb interaction with inhomogeneously distributed impurities. Right: the formation of band tails due to the perturbation, the dashed lines represent the unperturbed case (from [121]).*

emulsions (AgBr), a similar behaviour was observed for Ge, TiO_2 and CdS. The tailing was temperature dependent [120, 122]. The behaviour of the temperature dependence in inorganic material follows [121, 123]

$$N(E) \propto exp(-\beta E_a/nk_BT), \tag{7.2}$$

where E_a is the activation energy, related to E (difference from relevant band edge to E), $n \propto 1$ with, and β is a parameter representing the tail's width Later results [123] showed

that for amorphous inorganic semiconductors a uniform band tail over a large temperature range can be expected. Equation (7.2) is transformed into

$$N(E) = N_0 exp(-\beta E_a) \tag{7.3}$$

where N_0 is the density of states at the band's edge. Applying the latter expression, the activation energy from electrical transport measurements can be used for the analysis of band tails in the investigated tetrathiafulvalene compounds DT-TTF and DB-TTF.

7.2 Band tails in solution processed single crystal TTF-derivatives

Single crystal materials allow the investigation of intrinsic properties in the most ordered of all modifications of an organic semiconductor. Thus, the material can be tested for application using the - in general - best performing modification. The micrometer channel characteristics discussed in the previous chapter of the TTF single crystal materials have proved the high performance of the OFETs due to the single crystal transport in the solution processed materials (DB- and DT-TTF). The temperature dependence of the device parameters allows a closer look on the intrinsic properties. Organic single crystal transport has recently attracted much attention in several reviews [16, 22, 124]. As already discussed in chapter 3 in the purest single crystal materials even band transport similar to high crystalline inorganic semiconductors is observed (cf. section 3.2). However, the transition to a trap dominated multiple trapping and release mechanism is rather gradual. The influence of impurities and imperfections in the van der Waals bound organic crystals is often found to imply a transport by trapping and release [57, 119, 125]. Thus, the density of traps in the material is the crucial parameter [16]. Only in ultra-pure crystals and in a limited temperature range the phonon influence expressed by a decreasing mobility with increasing temperature is observed (cf. section 3.2). In the case of the solution processed TTFs a higher density of impurities is expected although no post-processing of the crystals (e.g. contacting the crystals) is necessary. In all single crystal devices a higher density of traps compared to the bulk occurs at interfaces, so that in the solution processed single crystals band transport with a decreasing mobility with increasing temperature (phonon influence) is not to be expected. The results in the following prove the temperature activated transport. For a detailed investigation of the transport properties a modified model of multiple trapping and release (MTR) by trap states [119] is applied. The induced band tails dominate the transport properties, leading to an exponential thermal activation of the mobility, characterised by the lowest energy state of the band tail [68]. This situation is generally encountered in both organic and inorganic amorphous materials [16, 68, 80, 121, 123]. Recently, it was shown that a similar exponential activation also exists in single crystalline organic semiconductors [80] where the trap states are located at or near the interface and thus can be modeled using a quasi two dimensional density distribution whose exact properties are determined by the gate insulator [95]. The analysis continues by the mobility behaviour with respect to MTR and will then follow the formalism as in [80] in order to

investigate the band tailing in the TTF single crystals. The subject forms the basis for the publication [26].

7.2.1 Activation of the field-effect mobility

Each transport model is characterised by the temperature behaviour of the mobility. Thus, when expecting a trapping and release mechanism an exponential increase of the mobility following equation (3.11) should result. The mobility values are extracted by a polynomial fit to the transfer curves in saturation at different temperatures (cf. equation (4.14)). The analysis in the high V_{DS} regime reduces contact effects with the result that the temperature dependence of these effects cannot influence the device parameter. The fitting range is chosen so that for each transfer curve the fitted V_{GS}-range is in the same distance to the V_{TH} value, obtained for this specific device. Thus, they average a possible effect of the gate voltage dependent mobility and still remain unaffected from injection or threshold voltage effects. Using the second derivative instead of a polynomial fit, an additional information on the V_{GS} dependence of activation is gained. The diagram in fig. 7.2 monitors the $\mu(V_{GS})$ behaviour instead of averaging for a single value of μ. A similar plateau formation of the mobility has been reported for high transverse electrical fields [11]. A monotonously increasing μ (V_{GS}) as predicted for V_{GS}-dependent mobility in [86] is not found in the analysed devices under the applied voltages. The Arrhenius plot (I_D in

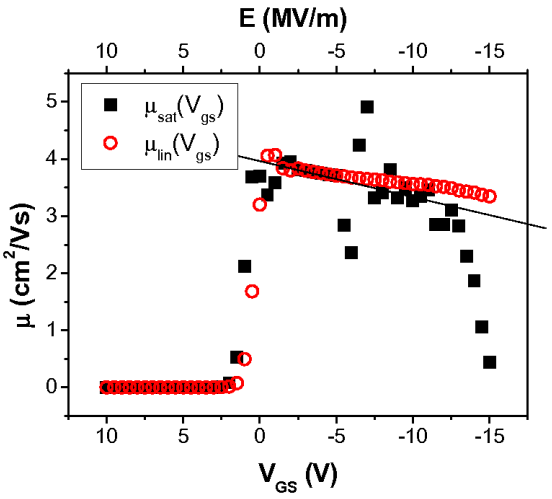


Figure 7.2: *Mobility versus gate-source voltage determined from a single crystal DT-TTF OFET by the first (linear regime) and second (saturation regime) derivative of the transfer characteristics (cf. section 5.1).*

logarithmic scale vs. $1/T$) of the mobility data of DT- and DB-TTF is presented in figure 7.3. The MTR activation energy can be directly extracted from the slope. It is evident that a non uniform slope is present over the investigated temperature range (50 K to 400 K). Apparently around 200 K a change in the dominating trap influence occurs. For DB-TTF we find a constant mobility between 50 K and 200 K and an exponential activation with an activation energy of 58 meV above 200 K. The mobility of DT-TTF, however, follows a bi-exponential activation. In a first ansatz we assume a superposing of two trap level and

extend equation (3.11) to

$$\mu_D(T) = \mu_0(\alpha' exp(-E_{a'}/k_BT) + \alpha'' exp(-E_{a''}/k_BT)),. \tag{7.4}$$

The DB-TTF data satisfy this equation with the second energy value equals zero and thus a constant offset mobility contribution. The bi-exponential fit to the DT-TTF data shows the two activation energies to be 15 and 108 meV.

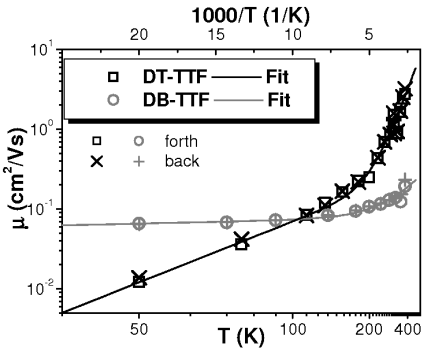


Figure 7.3: *Temperature dependence of the field-effect mobility as determined from transfer characteristics of DT-TTF (black) and DB-TTF (grey) OFETs for increasing (forth) and decreasing current (back) direction. The solid lines are bi-exponential fits to the data (cf. equation (7.4)).*

7.2.2 Activation of the drain current and density of states

While the above simplified analysis only shows the presence and the approximate depth of the band tails, a deeper insight can be gained by using a method as in ref. [80]. In this method the temperature dependence of the I/V characteristics is used to obtain a detailed picture of the energy distribution of the gap states and possible impurity levels. For this analysis, we first measure the current in saturation (V_{DS} = -15V) for different values of V_{GS} and at various temperatures between 50 and 400 K. In the band model representation

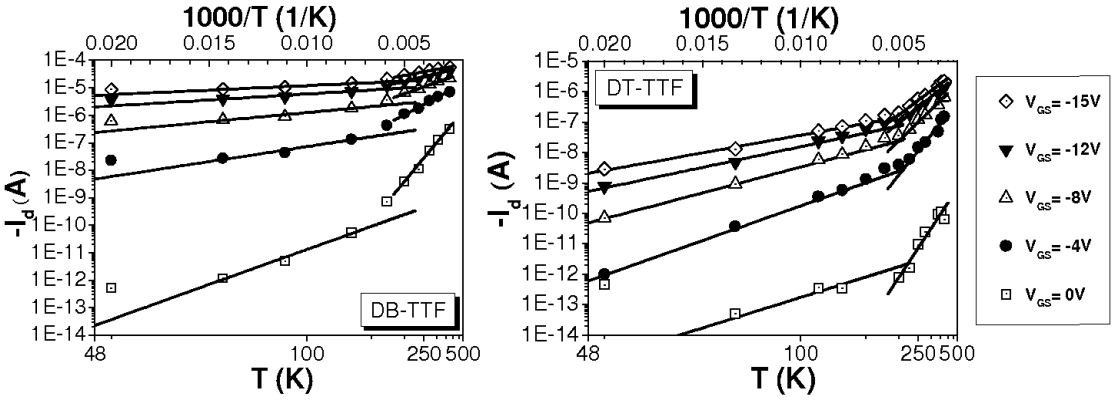


Figure 7.4: *Drain current I_D (logarithmic scale) in saturation ($V_{DS} = -15V$) at different V_{GS} plotted versus the inverse temperature for DB-TTF (left) and DT-TTF (right) OFETs. The straight lines correspond to exponential fits.*

a changing of the gate voltage towards more negative values sweeps the Fermi energy

through the gap towards the HOMO level (cf. section 4.3). During the sweep, more and more states contribute to the transport and by analysing the activation energy at each gate voltage we can identify the energy position of these trap states. Plotted versus the inverse temperature (fig. 7.4), the data reveal similar results for the two materials. For both we observe bi-exponential activation with two distinct ranges of activation energies below and above 200 K, respectively.

From the thermal activation of the saturation currents the activation energy of the states in the gap is subsequently plotted which then is plotted versus the respective gate voltages (fig. 7.5), yielding two data sets for each material corresponding to the low temperature ($T < 200$ K) and high temperature regime ($T > 200$ K). For the DB-TTF traps can be observed over the whole energy range between 10 and 130 meV. Below 10 meV the trap energies are too close to the HOMO to yield a useful signal. Trap energies above 130 meV are too high to be observable in the temperature regime investigated in our experiments. For the DT-TTF the situation is more complex. Here the two datasets leave an energy range between 75 and 95 meV where the density of states is too low to yield any significant influence on the I/V curves and is thus undetectable by this method. For further evaluation

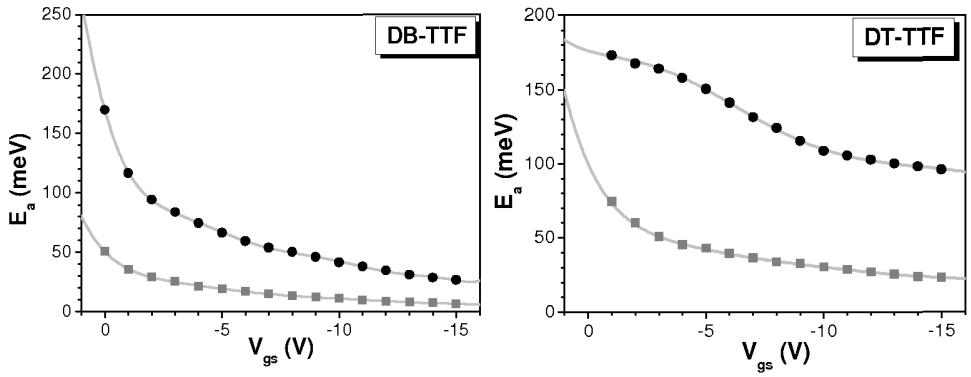


Figure 7.5: *Activation energy E_a (extracted from the data in fig. 7.4) plotted against gate voltage for DB-TTF (left) and DT-TTF (right). For both materials we distinguish two separate regimes with different ranges of activation energies, extracted from the measurements below (grey) and above 200 K (black). E_a is the energy above the HOMO level. The solid lines are the polynomial fit.*

we fit the data points of fig. 7.5 by a continuous (polynomial) function which allows us to determine its derivative at any voltage. We then use

$$N(E) = h \cdot \frac{C}{e}[dE_a/dV_{GS}]^{-1} \tag{7.5}$$

in order to determine the density of states in the gap (h approximates the trap depth from the interface into the semiconductor layer, e is the electron charge and C the capacitance per area of our gate dielectric which we calculate to be 33 nF/cm^2 for 100 nm thick SiO_2). In fact h converts the area density of equation (7.1) into a volume density. Following [126], the trap depth near the interface in organic layers is between 5 nm and 10 nm. The value of h is assumed to be 7.5 nm. The results are plotted in fig. 7.6. We have been careful

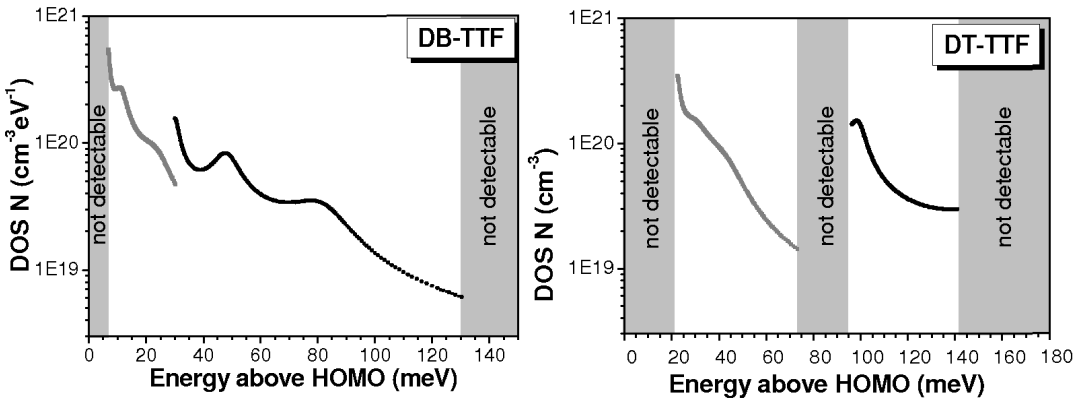


Figure 7.6: *Density of impurity states (DOS) plotted against their activation energy E_a above HOMO for DB-TTF (left) and DT-TTF (right). For DB-TTF a band tail emerges from the HOMO and exhibits two maxima at 50 and 85 meV. For DT-TTF there is a maximum at approx. 20 meV. The DOS decreases until it becomes undetectable at 75 meV. A second maximum can be found at 100 meV with the DOS decreasing again with increasing energy. The datapoints were calculated from the two datasets in fig. 7.5 (grey: below 200 K, black: above 200 K)*

not to evaluate parts of the fit which extend beyond or even contain the highest or lowest data points of the curve in fig. 7.5. In these parts of the curve the fit typically starts to develop small ripples, usually leading to large artifacts in the extracted density of states, which is extremely sensitive to small changes in the derivative of the fit function. In the density of states of the DB-TTF (fig. 7.6 left) we observe a band tail extending from the HOMO which has two pronounced local maxima, one at approx 50 meV corresponding to the activation energy determined using MTR and another maximum at approx. 85 meV. The second peak, however, indicates a much lower density of states explaining why it could not be observed using MTR.

For the DT-TTF we observe two separate regimes. The lowest observable energy region of the band tail starts at 20 meV, however, with a density of states three times higher than for the same energy in DB-TTF. We can assume that a maximum exists here, supported by the MTR evaluation (yielding 21 meV activation energy). With increasing energy the density of states decreases, becoming undetectable at approx. 75 meV. At 95 meV we see the density of states increasing again (now extracted from the data for $T > 200$ K) towards a maximum at 100 meV corresponding to the 104 meV activation energy determined by MTR. We see that the results obtained from MTR and the more detailed determination of the density of states are in good agreement. However, the latter yield a more detailed picture of the band structure. On the other hand, the MTR model is more straight-forward and yields results which are not sensitive to polynomial fitting parameters. For example a large trap density in DT-TTF at 21 meV is clearly visible in MTR. In the density of states plot (fig. 7.6), the density of states at 20 meV might just as well increase further towards lower energies without yielding a local maximum. The most reliable approach thus seems to be a combination of both methods as performed on our materials.

Besides the existence of these impurity states, the characteristics also demonstrate an untrapped carrier concentration which yields a finite current even at lower temperature. Especially in the case of the DB-TTF the mobility and carrier concentration remain more or less constant below 200 K. This finite carrier concentration also causes the weak dependence of threshold voltage on temperature. A plausible explanation could be that we observe transport either in states which are as close as a few meV to the HOMO or by pure hopping (i.e. not thermally assisted), two effects which cannot be distinguished in the investigated range of temperatures.

Chapter 8

In situ electrical characterisation of DH4T and DB-TTF

This chapter presents results on *in situ* electrical characterisation of the organic semiconductor in the ultra high vacuum (UHV) of the organic molecular beam deposition chamber (OMBD). The system setup is shown briefly in Appendix A, a detailed technical description of the deposition chamber and the setup for *in situ* characterisation can be found in several diploma theses (e.g. [108, 109]). The *in situ* investigations of organic materials are performed at a base pressure below 10^{-8} mbar and the temperature range of the built-in flow cryostat for the sample temperature control is 100 K to 400 K. The schematic measurement setup is presented in fig. 8.1.

The *in situ* measurement technique allows the electrical characterisation of vacuum deposited organic thin film materials on electrically contacted pre-patterned transistor templates (cf. fig. 8.1). It must be differentiated between a during growth characterisation, where the dependence on the layer thickness (or dependence on the growth mode (see appendix A) of the deposited material) is investigated, and an after growth characterisation where the intrinsic properties of deposited films are investigated. In both cases, the advantage is the exclusion of extrinsic effects, e.g. the exposure to ambient air which in thin film growth means a source of doping and/or oxidation or light irradiation, any post-deposition treatment, or fluctuations in ambient temperature by temperature control of the *in situ* sample holder. These properties make the *in situ* characterisation a very suitable tool for the material characterisation and the optimisation of growth parameters for the desired transport properties, because of the observation of purely intrinsic material behaviour. Moreover, exploiting the before mentioned advantage, another interest of the following analysis lies in the observation of possible effects that take influence on the active layer material of a transistor as there are the effect of applied voltages, which will be denoted to as stress in the following and the effect of a controlled exposure to various gases on the device performance. Especially the last types of investigations need well-controlled reproducible starting conditions. The use of electrode structures fabricated by a special

undercut profile electron beam lithography technique (cf. appendix B) and electron beam evaporated titanium/gold (1 nm Ti under 24 nm Au) in ultra-high vacuum (base pressure below 10^{-8} mbar), as well as good control of the pre-treatment step guarantee the comparability of the different transistor templates. In the following the dihexylquaterthiophene

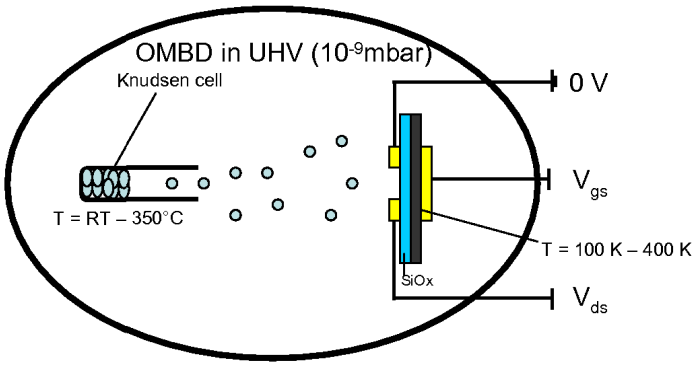


Figure 8.1: *Schematic of the setup for the in situ electrical characterisation of OFETs in the OMBD.*

(DH4T) and dibenzene-tetrathiafulvalene (DB-TTF) will be studied, where the larger part is dedicated to the DH4T. The DB-TTF exhibits a different behaviour due to the different growth mode and resulting morphology of the films (cf. appendix D), which is confirmed by electrical transport in comparison with the DH4T results.

8.1 *In situ* studies of evaporated DH4T

The section sums up observations and interpretations that are later compared with those of DB-TTF. It addresses to the stability of device parameters which is essential for reasons of comparison and for the interpretation of the investigated effects. The during growth characterisation of DH4T constates the two dimensional growth mode of the material. It proves that the *in situ* electrical characterisation is very suitable for comparison with morphological analysis, which is a critical aspect in organic semiconductor physics. The end of the section turns to a controlled application of stressing voltage on devices and the monitoring of the response. This is also investigated in dependence of temperature. The final subsection gives an interpretation of the stressing reactions.

8.1.1 Parameter stability and during growth study of DH4T

The first experimental results presented here, are to prove that the material exhibits excellent long term stability and that the more elaborate method of the *in situ* analysis is an excellent tool for the monitoring of intrinsic effects of organic semiconductors. According to the results of fig. 8.2 a possible intrinsic degradation in vacuum can be excluded. The two diagrams in fig. 8.2 present a long term study of the mobility and threshold voltage of transistors under *in situ* investigation over 90 hours. The two key parameter of the device

performance stabilise after slight changes during the first day. They can be supposed to be independent of age from then on. In addition to the data of fig. 8.2, very long term studies

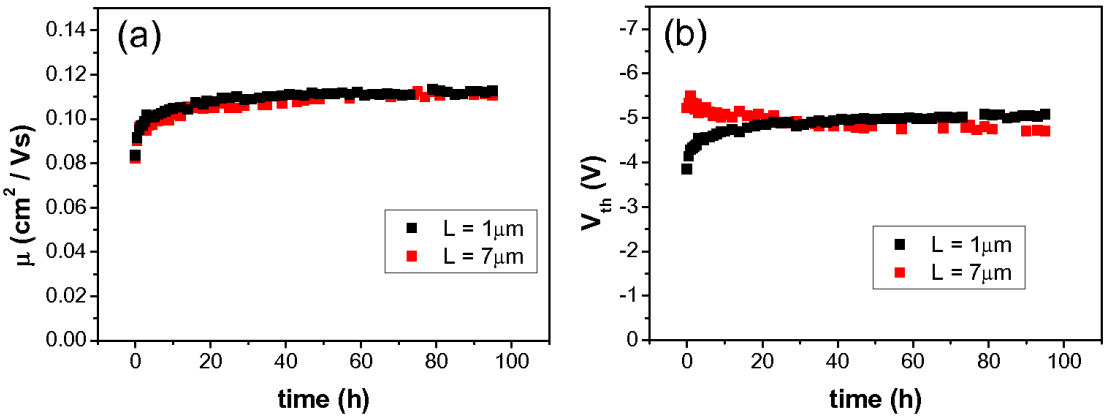


Figure 8.2: *A long term study of the mobility (a) and threshold voltage (b) of two DH4T transistors in an in situ study. A period of more than 90 hours after the deposition was monitored. Additionally the mobility value of more than 0.1 cm²/Vs, was confirmed during the 80 days including plenty of measurements.*

showed that the high level of mobility at around 0.1 cm^2/Vs was constant for at least 80 days (the end of the study!). The results presented in the following exhibit mobility values of a similar high level. This proves the comparability of the different *in situ* analysis and of the different transistor templates. Thus, the method is ideal for analysing the intrinsic properties and responses of the thin films.

The mobility in the OFETs increases during the first day. This cannot be attributed to the temperature dependence of the mobility, because the data represent the mobility and threshold voltage starting after the growth at 90 °C and slow cooling (passively for 30 min) of the sample to a value near room temperature. Moreover, the following days include change in room temperature of up to 3 °C which did not show a comparable reaction. According to [127] a local anisotropy of the density in the monolayers is claimed as a result of the cooling from the smectic phase under whose condition the DH4T was deposited. They may give rise to constraints in the structure which heal out at room temperature on considerably long time scale. This would explain the change in mobility because of the higher degree of order after the relaxation of the crystalline structure in the monolayers, as well as a change in threshold voltage to more positive values. The fact that in fig. 8.2 (b) the sign of threshold voltage change differs for the two devices with considerably different channel length (L = 7 μm vs. L = 1 μm), rather favours two mechanisms that take influence on V_{TH} with different signs depending on the channel length L. Another assumption is the relaxation effect due to the incorporation of residual atoms in UHV in the organic film. The pressure of the order of 10^{-9} mbar means a covering time of surfaces in the order of 1000s. Residual molecules should mainly be hydrogen and water, where at least the hydrogen has proved to stabilise dangling bonds in silicon technology. Such a beneficial aspect might play a role in our case, too.

The next paragraph discusses the development of the device parameters directly during growth. The during growth analysis of the transport characteristics of DH4T OFETs reveals the two-dimensional growth mode of the thin film material. The results in fig. 8.3 show mobility (a) in logarithmic scale and threshold voltage (b) values of DH4T OFET with two different growth temperatures for the mobility plot (room temperature (black) and 90°C (red)) versus the deposited layer thickness. The layer thickness is monitored during growth by the setup microbalance. The plot of the threshold voltage (b) compares the V_{TH} extracted from linear and saturation transfer curves for the 90°C deposition. In [34] the height of a monolayer of DH4T molecules in a crystalline formation is given by 2.8 nm. The diagrams' top axis uses this calibration factor. The beginning of the characteristic

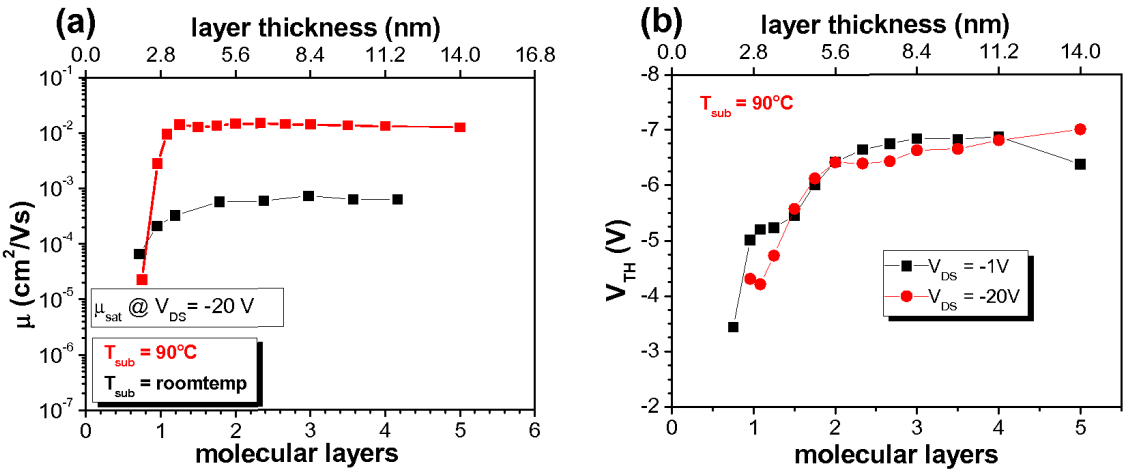


Figure 8.3: *In situ during growth study of DH4T. Diagram (a) represents the behaviour of the mobility (from the saturation regime) in logarithmic scale for a room temperature grown and a 90°C grown OFET versus the deposited layer thickness. Diagram (b) shows the threshold voltage from the linear and the saturation regime for the 90°C growth temperatures.*

monitoring coincides with the formation of a first channel between the electrodes. Regarding now diagram (a): for both growth temperatures this is at 0.75 ML. The growth at 90 °C (in the smectic phase) results in a saturating mobility shortly after 1 ML of thickness is deposited. This means a nearly ideal two dimensional growth of the material and proves the effective first monolayer for the device transport characteristics. At room temperature the saturation occurs later at 1.8 ML, which is explained by the material growing partly three dimensionally in islands due to the different growth mode at room temperature. The reduced ordering is mirrored in the lower mobility of the room temperature grown sample by more than one order of magnitude. Already in this plot at the elevated temperature two local maxima of the mobility in the saturation are visible, the first directly after the filling of the first layer and the second after the filling of the second layer at 1.2 ML and 2.2 ML, respectively. The diagram in fig. 8.4 (from [100]) confirms the results with an increased number of data and resolution in the electrical current measurement. The interpretation is that the two local maximum mobility values correspond to the filling of the first and the second monolayer. The dips afterwards are caused by interference of the next still incom-

plete layer, by a trapping mechanism of the charge carriers. In diagram (b) of fig. 8.3 is shown that the threshold voltage of the device also saturates in both cases (linear and saturation regime) to a value near -7 V. However, it decreases (scale is reversed!) until the filling of the second layer. Shortly after the first layer is filled, a small plateau of the curve is built before decreasing to the saturation value. These two distinguished points correlate with the local maxima observed in the mobility plot of diagram (a). This is a further proof of the sensitivity of the parameter V_{TH} towards the layer to layer growth and an indication of the new formation of traps. The fact that V_{TH} decreases means that the formation of new traps relatively takes more effect on transport compared to the completion of new current path. The during growth results prove the effective transport channel to be within the first few

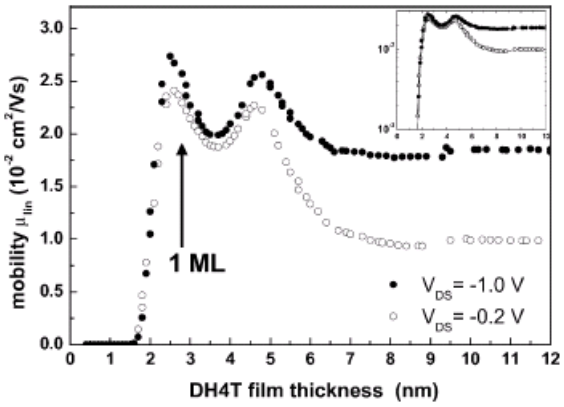


Figure 8.4: *In situ during growth study of DH4T OFETs from Muck et al. [100].*

monolayers, which first has been proposed by [128] in an *in situ* study of sexithiophene. Thus, from aspects of a two-dimensional device, the DH4T OFET comports according to the ideal assumptions of section 4.3.1. However, the formation of traps indicated by the decrease of the threshold voltage continues to take effects on the transport until the filling of more than the first two layers. Bulk effects, however, can be neglected for thicker layers which makes the material favourable for an investigation in the sub-micrometer channel regime (see next chapter).

The following two subsections will be more device specific and show how the mobility and threshold voltage react on stress, on the variation of temperature or on the combination of both.

8.1.2 *In situ* stress effects by applied voltages

As already mentioned above the meaning of “stress” in this context will be a change of device performance due to applied voltages. For the OFETs these are an influence of the channel voltage between source and drain V_{DS} and the gate to source voltage V_{GS}. Stressing a device with applied voltages qualitatively means the filling or depletion of traps in the bulk semiconductor material, at the interfaces, or/and in the insulator. Following

the first part of the thesis (chapter 4), the most sensitive device parameter for a change in trap density is the threshold voltage V_{TH}. The following results illustrate the dependence of V_{TH} on stress and are explained by a consideration of traps. In the schematic of fig. 8.5 the employed stressing cycles are shown. The main parameters besides the number of measurements and stress phases n in a cycle are the two constantly applied voltages V_{DS} and V_{GS} during the stress phases, the time of the application of the voltages t_s and the relaxation time t_r after a cycle. Due to the measurement setup, there is an additional approx. 5 s of monitoring time for the transfer curve that is used to investigate the device parameters and switching to the next stress phase. During the stressing time t_s, the constant stress voltages V^s_{DS} and V^s_{GS} are applied. A transfer curve is recorded after every stressing period. The present mobility and threshold voltage are calculated. The voltage sweep during the transfer curve is kept between the threshold voltage and the value of the applied stressing voltage V^s_{GS}. In this way it is guaranteed that the measurement does not counteract the stress effects by a voltage before V_{TH} (in the closed device status), or contribute to the stress in a considerable fraction by voltages above V^s_{GS}. In the case of zero applied V^s_{GS}, the contribution to stress of the measurement itself can be analysed. After a number n of these measurements and a relaxation time t_r the next cycle starts. The stressing results

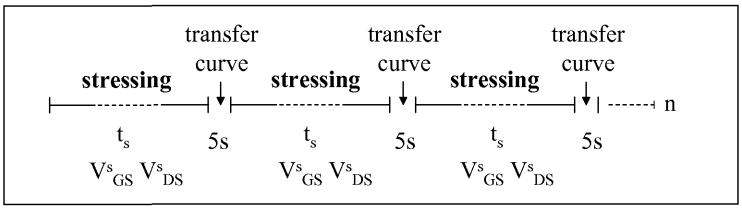
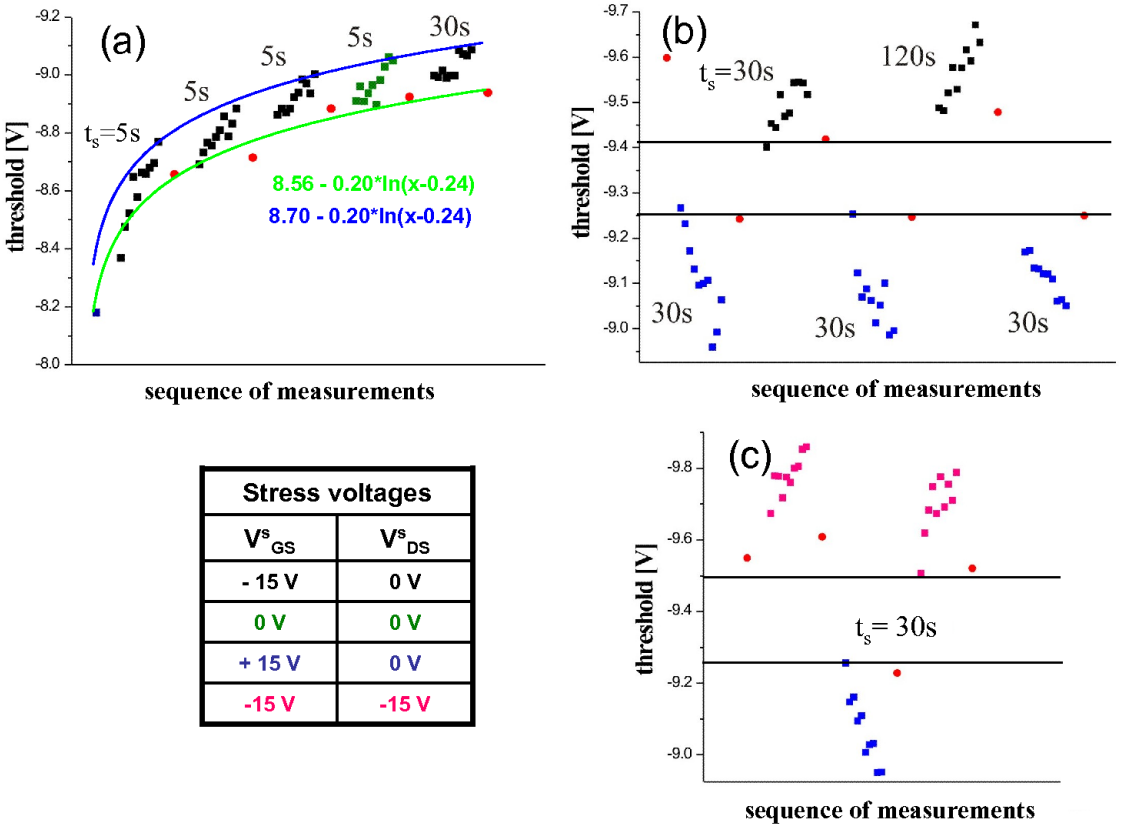


Figure 8.5: *Schematic of measurement cycles for the investigation of stress effects on OFETs from applied voltages.*

of DH4T at room temperature are presented in the three diagrams of fig. 8.6. The first diagram (a) proves an irreversible shift of the threshold voltage at the start of stressing when only an accumulating V^s_{GS} of -15 V is applied. The ten black (or green) squares of each cycle represent the values determined during the stressing phases, the blue circle is the initiation value before the first stress cycle, and the red circles are the V_{TH}-values after a regeneration phase of 1 h. The regeneration of the threshold voltage saturates at a value near -9 V. The first three sequences with the same stressing interval time t_s of 5 s apart from the first four data points show a comparable shift of the threshold voltage to more negative values due to the stress voltage V^s_{GS}. Interestingly, the fourth sequence (in green) fits well into this series although zero V^s_{GS} is applied. This aspect of a strong influence of the measurement itself on the material's reaction can be attributed to a strong influence of an additionally applied channel stress V^s_{DS}, which is also confirmed by the third diagram (c). The applied $V_{DS} = -15$ V during the monitoring of the transfer characteristic (2-3 s) seems to act in a similar way as a phase of stressing inbetween. The last sequence with increased t_s to 30 s does not cause a stronger reaction. The two fit lines of diagram (a) to the regeneration data points (green fit) and to the last (negative maximum) value of a stressing cycle (blue fit) are logarithmic

$$V_{TH} = P1 + P2 \cdot ln(\frac{time}{[time]} - P3).$$

The characteristics of these data points allow to fix parameters P2 and P3 for both fits and an offset value of 0.14 V between the fits can be extracted. In this way the two fits confine the values where an accumulating V^s_{GS} takes effect. In the second diagram (b) depleting



Stress voltages	
V^s_{GS}	V^s_{DS}
- 15 V	0 V
0 V	0 V
+ 15 V	0 V
-15 V	-15 V

Figure 8.6: *Three diagrams reflecting the behaviour of the threshold voltage of DH4T OFETS in in situ stressing studies described by the schematic in fig. 8.5. Stressing time t_s and applied stress voltages are denoted in the diagrams or the tabular (itemised by colour): (a) irreversible shift of the V_{TH} value as an effect of an accumulating V^s_{GS} during the first stressing applied,(b) a memory effect in consequence of application of accumulating and depleting V^s_{GS} ,(c) enhancement of accumulating stressing by an additional V^s_{DS} (on-status of the device). The memory effect remains as before.*

(positive) and accumulating (negative) V^s_{GS} are applied (15 V and -15 V, respectively). The data are not consecutive to that of diagram (a) but a different transistor device after a positioning of V_{TH} comparable to diagram (a). This is a proof for the reversibility of the effects after the first irreversible shift from diagram (a). The variation of threshold voltage between different *in situ* investigated DH4T samples was between -8 V and -10 V in large channels ($L > 5\mu$m). A depleting V^s_{GS} (blue circles) has a reverse effect, V_{TH} shifts to more positive values. Again the regeneration values (in red circles) after 1 h do not fully recover but reach the value after the first stressing measurement. As a consequence the effect defines a voltage regime confined by the two horizontal bars in diagram (b) of approximate width of 0.15 V. Comparable memory effects of the transistor could be established in all DH4T devices that were investigated by *in situ* stressing methods. Moreover, it is an

intrinsic effect in the material or at the interface which makes it interesting for a usage of the parameter of threshold voltage in sensor or memory application. Regarding the two different relaxation values of diagram (b) it is temporally stable. The size of the effect is also influenced by fabrication and pretreatment of the device. As already mentioned, the third diagram (c) in the series of fig. 8.6 includes a V^s_{DS} of -15 V in combination with the accumulating V^s_{GS}, which means the on-status of the OFET. It results from consecutive measurements to diagram (b). The shift of V_{TH} is strongly enhanced and the memory effect still exists to a comparable extent. The mobility is not affected in the room temperature sequences which confirms the result from the beginning of this section.

8.1.3 *In situ* temperature dependence of the stress effects

This subsection will address to stressing at different temperatures applied in *in situ* measurements of the kind described in the schematic of fig. 8.5. An overview of the investigated reactions of V_{TH} and μ is given by the two diagrams in fig. 8.7. The analysis considers temperatures between 107 K and 363 K. Following the chapter on temperature dependent transport this includes a large variation of the parameters due to their pronounced temperature dependence. Therefore, the representation of the reactions on stress in the diagrams is relative to the first relaxation value at each temperature before the start of the stressing sequences. The stressing parameters are included in table 8.1. Black data points are after accumulating stress V^s_{GS} = -12 V, green are depleting stress V^s_{GS} = 10 V and blue are "operating" stress $V^s_{GS} = V^s_{DS}$ = -12 V. Red data points reflect the parameter value after a relaxation of 30 min. In the left diagram the values of the shift of V_{TH} are plotted versus time. The right diagram shows the relative shift of the mobility. In summary, there is a

Stress voltages of fig. 8.7			
V^s_{GS}	- 12 V	+ 10 V	-12 V
V^s_{DS}	0 V	0 V	-12 V

Table 8.1: *Stress voltages applied to DH4T OFETs in temperature dependent in situ stress experiments. The colour itemises the voltages regarding the data points in the diagrams of fig. 8.7.*

strong influence of temperature on the reaction to stress in DH4T OFETs. These effects can be considered as reversible for both parameters V_{TH} and μ. Below room temperature the effects are reduced. This applies even more below 200 K. Above room temperature the reactions are large monotonously increasing with the temperature. Considering the threshold voltage: an accumulating stress (black points) is moderately shifting V_{TH} to more negative values, the effect is clearly increased in operating mode (blue), when additionally a V^s_{DS} is applied. A depleting stress reverses the effect. For the mobility the behaviour is the same for temperatures above room temperature. At room temperature and below, the parameter value is rather reduced or unaffected. Effectively, the investigated stability of the mobility in long term measurement including stressing measurement as reported above, reflects this temperature behaviour and may be material specific for DH4T.

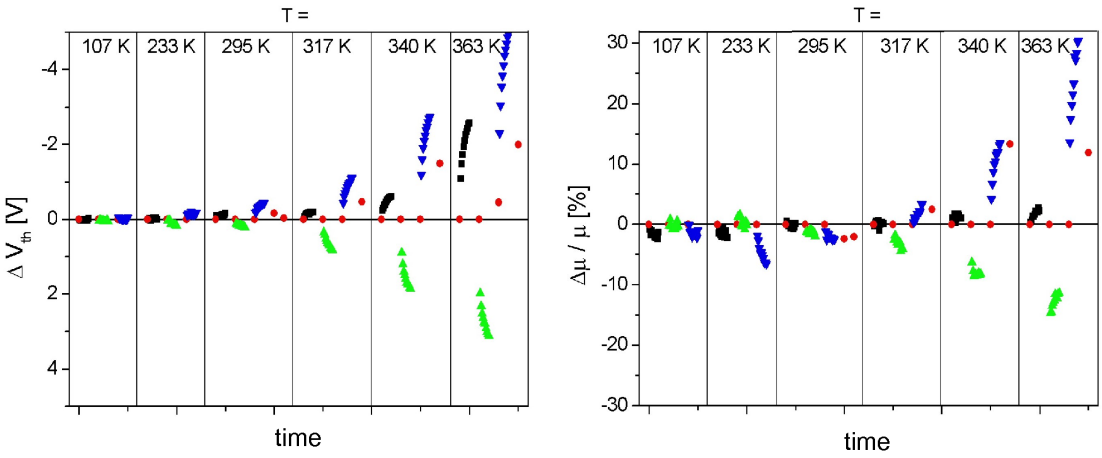


Figure 8.7: *Two diagrams reflecting the change of the threshold voltage (left) and the mobility (right) of DH4T OFETs in temperature dependent stressing measurement. The characterisation has been performed in situ with cycles similar to the schematic in fig. 8.5. Black points consider the sole stressing by an accumulating V^s_{GS} of -12 V, the green points are under depleting V^s_{GS} of 10 V, and the blue points are under operating stress of $V^s_{GS} = V^s_{DS}$ = -12 V (cf. table 8.1). The red points are from measurements after relaxation of about 30 minutes, or before the stressing.*

8.1.4 Modelling and interpretation of the mechanism

In an early work in the field of organic thin film transistors, Brown et al. already proved the stressing to be a relaxation process and not a degradation effect in polymer thin films [83]. Reversible reaction of the threshold voltage combined with a constant mobility (the shape of the transfer curve does not change) is also described in [129, 130] for vacuum deposited thiophene material. These data, however, are measured *ex situ* and are lacking of data on the temperature dependence as presented above. A possible explanation of the temperature dependent behaviour is given by bias induced trapping of charge carriers in less mobile states. The slow release of charge carriers from these traps would explain the relaxation effect, which is expected to be increased by a charge carrier depleting stress voltage. The origin of the traps is supposed to be in the insulator and in the active layer material near the interface of the two materials. A microscopic schematic is given in fig. 8.8. In this way the trapped positive charges shield the applied V_{GS} to a certain degree and the threshold voltage for the onset of transport is shifted [130]. In silicon and amorphous silicon TFT technology the threshold voltage shift is also a critical issue. Models relate more to the effect of dangling bonds in the semiconducting material [131]. In contrast to OFETs a full relaxation requires an annealing of the TFT [131, 132]. The mechanism in OFETs is thus still under examination. Work from Street et al [133] specifies that the formation of immobile Bipolarons from two holes in the presence of traps causes the shift. A more quantitative model can be attributed under the assumption of traps in the insulator material. A tunnelling mechanism of accumulated charge carriers in the insulator follows

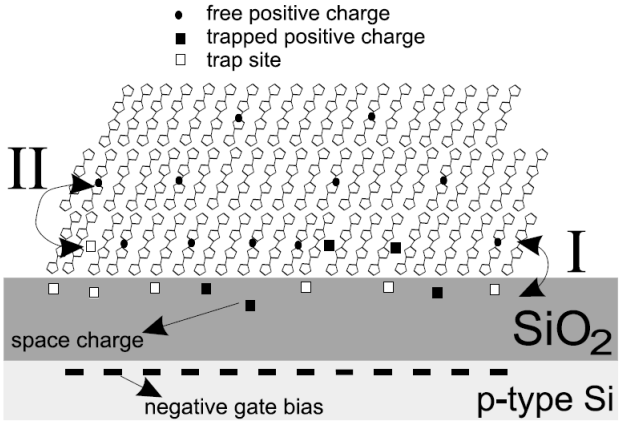


Figure 8.8: *Schematic describing a model mechanism for the bias–stress induced shift of the threshold voltage, from [134]. Charge carriers are trapped and released near the interface of insulator and semiconductor.*

with a logarithmic time dependence of filled trap density N_t on stress time [135]

$$N_t(t) \propto ln(\frac{t}{t_0} + 1) \tag{8.1}$$

with t_0 describing the time parameter of the tunnelling. This, however, is directly connected to the shift of the threshold voltage expressed in the equation

$$\Delta V_{TH}(t) = r_d \cdot ln(\frac{t}{t_0} + 1) \tag{8.2}$$

with the material specific parameters r_d and t_0. From empirical results a potential dependence of the threshold shift on stress time is also proposed in literature [136].

$$\Delta V_{TH}(t) = \Delta V_0 \cdot t^{\beta} \tag{8.3}$$

Here, V_0 and β are the controlling parameters. In fig. 8.9 the resulting threshold shifts from fig. 8.7 depending on stress time are plotted for the different temperatures. The diagram (a) only considers accumulating V^s_{GS}, whereas the diagram (b) shows the operating stress results. For reasons of comparison the two plots are in the same scaling. The effect of an operating stress (device in on-status) is twice as strong as the mere accumulating stress. Interestingly, both fits following the two different ansatzs, which lead to equations (8.2) and (8.3) suit the data very well. The logarithmic fitting appears to be nearer to the data for lowest and highest stressing times. However, there cannot be made a characteristic choice from the results.

8.2 *In situ* study of DB-TTF

The section will give a brief insight into the transport properties of evaporated DB-TTF observed in *in situ* measurements. The fact that the observed behaviour differs a lot from the results described in the sections above on DH4T confirms the crucial meaning of the

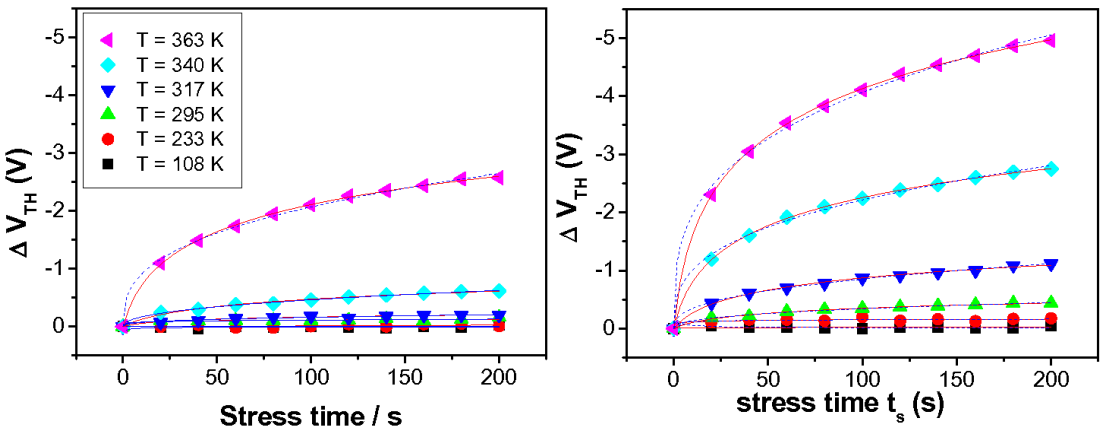


Figure 8.9: *Threshold voltage shifts depending on stress time at various temperatures from 108 K to 363 K. The ΔV_{TH} increases with increasing temperature. Two models that result in equations (8.2) (logarithmic behaviour, red lines) and (8.3) (potential behaviour, dashed blue lines) fit the data very well.*

structural ordering in the materials on their transport properties. In appendix D the corresponding structural analysis with atomic force microscopic methods is presented. Under the investigated growth conditions the DB-TTF has proved to grow three-dimensionally in the Vollmer–Weber growth mode (cf. appendix A). The denoted layer thicknesses average the deposited material as described in appendix D.

8.2.1 During growth study

The diagrams of fig. 8.10 present the results of the during growth analysis of a DB-TTF OFET corresponding to those shown for DH4T in fig. 8.3. The obvious difference is that there is no saturation of the mobility depending on the layer thickness. The layer to layer distance of the known DB-TTF structure is 4 Å (cf. section 2.2.1 of Chapter 2). Even when assuming an unknown ordering with more upright molecule formation in the evaporated films, the scale of the diagrams indicates that no thin film is formed. The mobility increases with more and more material deposited, which can be explained by the filling of gaps due to the growing together of material islands. It is also possible that a bulk contribution to the mobility is responsible for the increase with increasing average layer thickness. This hypothesis is most likely, because the mobility also shows a strong dependence on V_{DS}, although the general behaviour in linear and saturation regime is the same. However, from fig. D.6 the theoretical complete surface coverage of the evaporated DB-TTF is given for an average layer thickness of 154 nm, in this case beyond the investigated thickness range. In diagram (b) is shown that both the threshold voltage in the saturation and the linear regime saturate after an average layer thickness of 60 nm, which indicates that the bulk contribution to mobility is the cause of the non-saturating mobility and that traps in the bulk do not contribute to the threshold change in a comparable amount as the interface

states. The difference in threshold voltage value between the two regimes of more than 1 V after the saturation may be due to the same cause that is responsible for the dependence on V_{DS} of the mobility. Another obvious difference between DB-TTF and DH4T is the positive value of the threshold voltage for DB-TTF, which indicates a generally different ratio of charge carrier to trap density in the two materials. In the next subsection the difference between the materials will further be proved by the *in situ* stressing behaviour of evaporated DB-TTF.

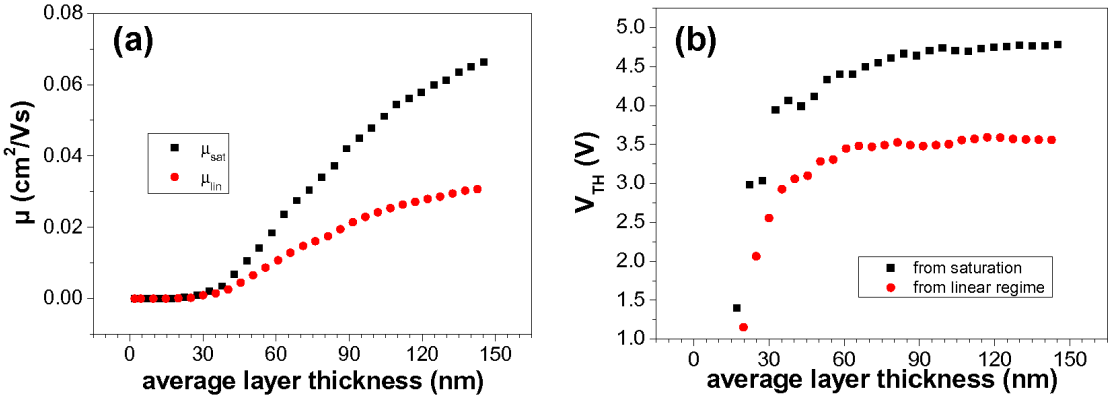


Figure 8.10: *(a) Mobility depending on average layer thickness of an evaporated DB-TTF OFET measured in situ during growth.*
(b) Corresponding diagram of the same device for the threshold voltage extracted in the linear and saturation regime.

8.2.2 Stressing effects on DB-TTF

The stressing of DB-TTF is combined with the influence of a fractional amount of atmospheric gases. The diagrams (a) and (b) of fig. 8.11 follow from nine stress cycles at room temperature applied to a DB-TTF OFET after growth and without breaking the vacuum ($p < 2 \cdot 10^{-9}$ mbar). After the three first consecutive cycles (black squares) and the next day the pressure is changed to $p = 10^{-5}$ mbar for another three cycles (blue squares), and then after re-installing the base pressure of $p < 2 \cdot 10^{-9}$ mbar (again the next day) the final three cycles (black open squared) follow. In each of the three groups the first cycle applies an accumulating stress (V^s_{GS}= -15 V), the second an operating stress (V^s_{GS}= -15 V, V^s_{DS}= -15 V), and the last a depleting stress (V^s_{GS}= 15 V). The stressing time t_s is always 30 s and the duration of relaxation t_r = 30 min (no voltage applied) after each cycle. The data points after relaxation are denoted in red. First of all the diagram (a) proves that only a depleting stress (V^s_{GS}= 15 V) causes a shift of the threshold voltage, the increase of the coverage by air molecules of the DB-TTF film enhances this reaction. However, apart from that an accumulating and even operating bias provokes no reaction of V_{TH}, even in the higher pressure regime, which means that the trap distribution is not influenced in that case. When applying a positive gate voltage, the V_{TH} shifts to more positive values (the

channel opens). Thus, the depleting stress mode influences the trap distribution in such a way that the trapping and release mechanism is reduced. This shift is not fully reversible. The last relaxation value of each of the three cycle groups is lower than the final stress value (between $\frac{1}{4}$ and $\frac{1}{2}$ of the total shift), but the over all trend is the increase of V_{TH}. The level of the last relaxation value is the start for the next group one day after, which proves that already 30 min of relaxation is enough to install a stable parameter condition and that the mere installation of the higher pressure does not cause the shift. Figuratively, it appears that the traps are driven out of the material or conducting channel by the depleting stress mode. In the band model this may be a change in energy level from shallow to deep trap, or the compensation of a charged trap due to the applied voltage.
The mobility of the OFET reduces slightly under stress and during the measurement (in the order of days). Again, the strongest reaction is in the high pressure regime. Moreover there is a memory effect only under increased air influence. The relaxation values of the other two groups are on the same level. The experiment proves that the material in its

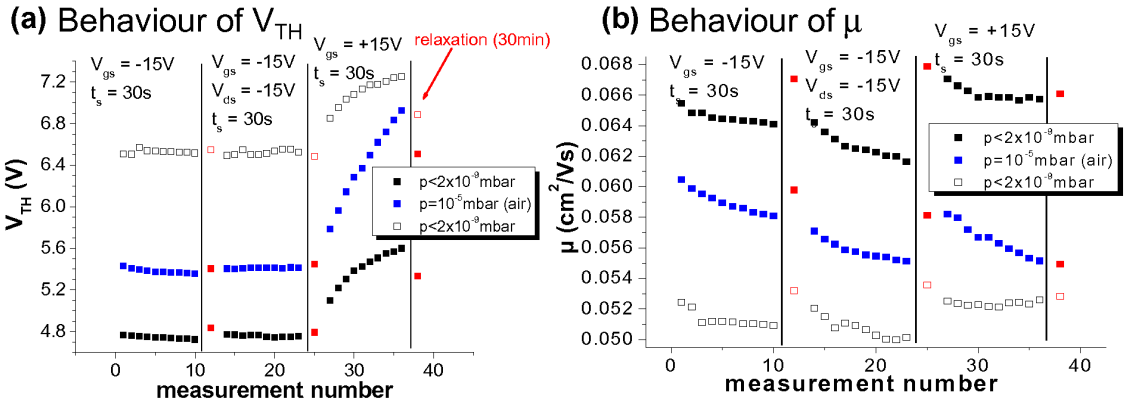


Figure 8.11: *(a) Behaviour of the threshold voltage of an evaporated DB-TTF OFET. A series of accumulating (V^s_{GS}= -15 V), operating (V^s_{GS}= -15 V, V^s_{DS}= -15 V), and depleting (V^s_{GS}= 15 V) stress cycles is applied after growth without breaking the base pressure chamber vacuum of $p < 2 \cdot 10^{-9}$ mbar, after installation of $p = 10^{-5}$ mbar, and after re-installing $p < 2 \cdot 10^{-9}$ mbar, respectively. Each cycle consists of 10 stressing periods (30 s) with one monitored transfer curve and the monitoring of a relaxation value after 30 min of no voltage applied.*
(b) Corresponding diagram of the same device presenting the behaviour of the mobility.

vacuum deposited variant is very sensitive to air, but very stable considering an operating device mode. Furthermore, the developing of V_{TH} under stress in the case of p $= 10^{-5}$ mbar appears to be far from a saturation. The above is of interest for a sensor application. Due to the influence of air molecules an interaction between them and trap states under the presence of a depleting voltage suggests itself as the major hypothesis.

Chapter 9

Electrical properties of sub-micrometer channels

This chapter is dedicated to the behaviour investigated in small channel organic field-effect transistors. In this context small means sub-micrometer channel. The minimum channel length of the investigated devices was 50 nm. From Moore's law in silicon technology [137] the meaning of miniaturisation for a whole business becomes evident. The standard silicon CMOS technology meanwhile works at lithography techniques allowing 45 nm channel lengths MOSFETS (32 nm on the roadmap) on ultrathin oxide (1.2 nm) or alternatively, on high-k dielectrics. The integration of devices meanwhile is as high as 10^9 transistors per integrated circuit [138] with even higher figures announced for the near future. In the field of organic electronics the motivation for a miniaturisation of devices and circuits is comparable, although not challenging at all the eager plans of silicon technology. The basic approach is to go to higher switching frequencies and generally enhanced performance at lower power consumption by making the devices smaller. Moreover the crucial parameter for the OFET is its channel length L. A short motivation has already been given in section 5.3. The following results will treat the physical effects of the reduction in size of OFETs with different active layer material and morphology. The effects will be investigated by the characteristics of OFET devices with different channel lengths. These are results of the scaling behaviour of the device parameters (field-effect mobility μ, threshold voltage V_{TH} and on/off-ratio I_{on}/I_{off}). The aspects of the semiconductor morphology and the thickness of the dielectric play a crucial role. DH4T and DT-TTF are compared, and the variation of the insulating SiO_2-layer thickness is investigated. An interest also lies in giving possible options for a reduction of the channel length while keeping a good device performance. 'Good' will be generally dealt with as the long-channel behaviour as described in chapter 4. In order to do this the appearing deviations from textbook (=long-channel) behaviour will be presented and explained following the effects described in section 5.3 on short-channel behaviour.

The chapter will first address issues on sub-micrometer device fabrication and then

give the results for the vacuum evaporated materials dihexylquaterthiophene (DH4T) and dithiophene-tetrathiafulvalene (DT-TTF). The results will start with the DH4T which represents the material most suitable for the reduction of sizes in the device. The previous chapters on experimental results have proved the high quality of the DH4T thin film in terms of device properties and also its two-dimensional transport in the fist monolayers (section 8.1.1) in OFETs due to the inherent current anisotropy in thin evaporated films (cf. section 2.2.2). This is the reason for its better performance in sub-micrometer devices where bulk contribution to transport play a decisive role. The results will be compared with those of vacuum deposited DT-TTF.

9.1 Device fabrication

The technical aspects of the device fabrication, which includes high resolution lithography (electron beam lithography (EBL)), is treated in appendix B. Here, the final "output" is presented. The applied fabrication technology (EBL with lift-off for the electrode structuring) generates thin-film transistors in the bottom gate, bottom contact setup as schematically presented in fig. 4.1 of section 4.3. The devices follow the same layer by layer treatment as for the standard micrometer OFETs. The transistor source and drain electrodes consisting of high workfunction material (usually thin Au (19 nm) and an adhesion layer of 1 nm Ti) are structured on oxidised silicon wafers. A result for a L = 50 nm source and drain electrode structure is presented in fig. 9.1. The challenge of the electron beam lithography with metallisation and lift-off technique is to guarantee the small channel length homogeneously (± 10 nm) over the whole channel width of usually as in this case 200 μm. The solution is a thin two-layer resist of PMMA with different molecular weight of the two layers that allows the necessary resolution and undercut profile in the resist for a homogeneously working lift-off (cf. appendix B). The contacting pads are fabricated in a next step by UV optical lithography, metallisation and lift-off. In order to investigate

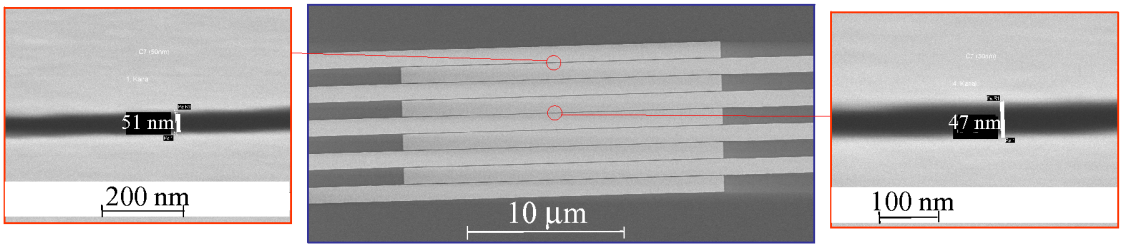


Figure 9.1: *Source and drain electrode structure consisting of (19 nm gold on 1 nm titanium) on SiO_2. The channel length L is about 50 nm with a maximum variation of only ± 10 nm over the whole channel width W of 200 μm.*

long-channel behaviour in small channel devices, the results have proved that an access to smaller channel lengths is best possible in combination with the thinnest used SiO_2 dielectric layer of 10 nm thickness. Comparable results to fig. 9.1 with an even more reduced L

(20 nm) were achieved in a students project work [139] using the same fabrication method with a further optimised resist system.

The templates undergo the same treatment as for the standard OFET fabrication. The pretreatment is done by OTS in chloroform (cf. appendix C). The final step is the deposition of the organic semiconductor. An impression of a finished L = 400 nm dibenzene-tetrathiafulvalene (DB-TTF) device is given by the atomic force micrographs of fig. 9.2. The film of DB-TTF is deposited via vacuum evaporation which results in island growth (cf. appendix D). Regarding its growth mode it is comparable with the here investigated DT-TTF. However, concerning the performance in sub-micrometer FETs the DT-TTF exhibits the better results. The interference with the electrode tends to result in a higher coverage of material at the interfaces of electrode finger (finger width is 1 μm) and channel (lines).

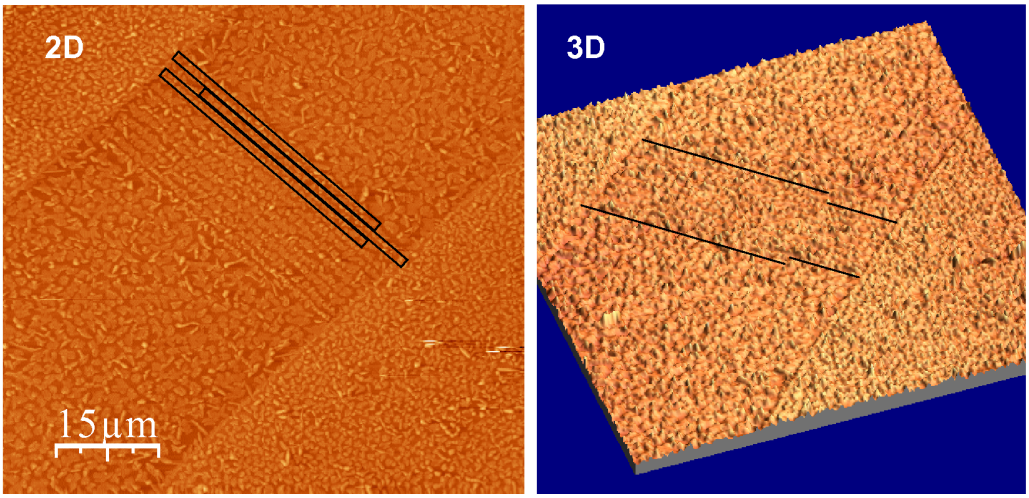


Figure 9.2: *Atomic force micrographs of source and drain finger electrodes with vacuum deposited DB-TTF. Left: the two-dimensional representation, the black lines are the borders between fingers of 1 μm size and channel (L = 400 nm). Right: a three-dimensional representation of the AFM data*

9.2 Dihexylquaterthiophene

The maintenance of the gradual channel approximation (cf. section 4.3.1) plays a key role in keeping textbook (long-channel) behaviour while reducing the channel length of a transistor. The reduced channel length L favours the longitudinal, drain-source voltage controlled electrical field compared to the transverse electrical field. Thus, in order to maintain long-channel conditions the gate voltage controlled transverse electrical field must be increased [140]. The easiest way to achieve this at constant voltage is a thickness reduction of

the gate dielectric. The series of output characteristics from L = 2 μm to L = 100 nm DH4T FETs in fig. 9.3 show the influence of the reduction of SiO_2 thickness d_{ox} from 100 nm (a) to 30 nm (b). For both oxide thicknesses the micrometer channel exhibits long-channel behaviour with a linear regime and full saturation of currents at high V_{DS}. For a d_{ox} of 100 nm the saturation of current ceases already at L = 400 nm, which is caused by the channel length modulation (CLM) effects (cf. section 5.3) due to the large longitudinal electrical field. The characteristics for the 100 nm channel are an example for the next grade in short channel behaviour: the punch through (PT) effect, the current increases more than linear with increasing V_{GS}. The thinner insulator, however, results in long-channel behaviour even for the 200 nm channel. A direct comparison of the output of L = 100 nm OFETs

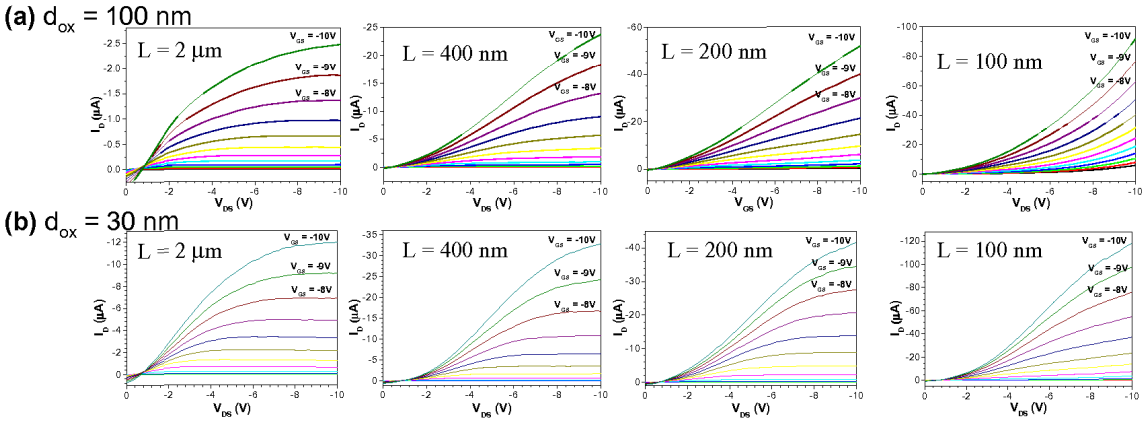


Figure 9.3: *The output characteristics of DH4T FETs with a channel length from 2000 nm to 100 nm for a SiO_2 insulator thickness of 100 nm (a) and 30 nm (b). The DH4T layer thickness is 13 nm, grown at T_{sub} = 90 °C at ≈2 Å/min (standard conditions)*

with different d_{ox} is presented in fig. 9.4 part (a). The two first fields of output characteristics from 9.3 are compared with a third OFET of L = 100 nm on 10 nm SiO_2 using the same V_{DS}-scaling and all three devices having a channel width of 200 μm. This series indicates the transition from punch through (d_{ox} = 100 nm), over channel length modulated (d_{ox} = 30 nm) to long-channel behaviour (d_{ox} = 10 nm) merely by the choice of the oxide thickness. The thinnest oxide, however, limited the applicable V_{GS} to 6 V in order to avoid irreversible oxide breakdown. The effect of a reduction of the channel length below 100 nm for SiO_2 thickness of 100 nm and 10 nm, respectively, is presented in the output characteristics in part (b) of the same fig. 9.4. The d_{ox} = 100 nm devices show both the PT effect. The field-effect by the controlling V_{GS} is still expressed for both channel length (80 nm and 50 nm). The third diagram in fig. 9.4 (b) shows a 80 nm channel OFET on 10 nm oxide still exhibiting quasi long-channel behaviour, the characteristic value for the CLM λ is calculated to -0.3 V^{-1} (V_{early} = 3.6 V, cf. fig. 9.8) and linear transfer curves (at V_{DS} = -1 V) have a considerably low off-current value of 10^{-9} A. This is comparable to the value monitored in the right diagram of fig. 9.5 for the L = 100 nm device.

The transfer characteristics give direct access to the key parameters mobility, threshold voltage, and on/off-ratio. In the following, these parameters will be taken for the evaluation

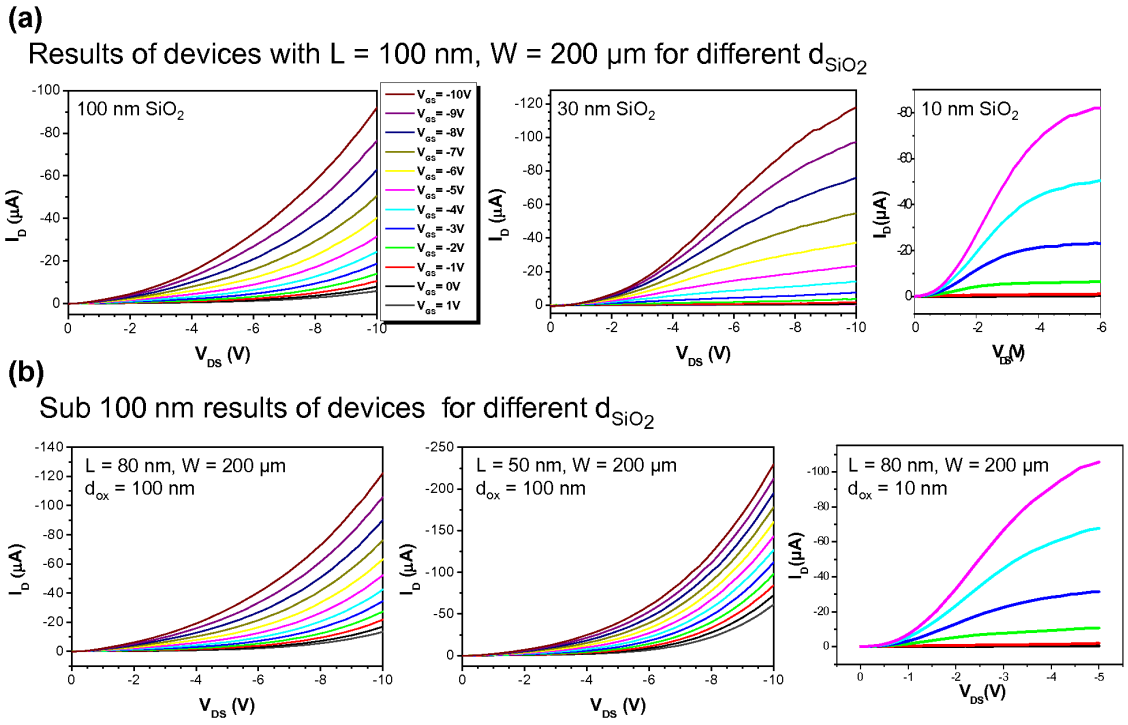


Figure 9.4: *a) The transition from punch through over channel length modulated to long-channel behaviour in output characteristics of L = 100 nm DH4T FET devices, when reducing the oxide thickness from 100 nm over 30 nm to 10 nm, respectively. b) Sub-100 nm channel DH4T FETs on 100 nm and 10 nm SiO_2.*

of the scaling behaviour. The left diagram of fig. 9.5 shows the corresponding transfer characteristics to the output of the L = 200 nm device shown in fig. 9.3 (b). The curves in the linear regime as well as the one of the saturation regime have a low off-current of 10^{-10} A (which was the resolution limit of the measurement). Although the cross section of the prolonged subthreshold slope with the ordinate is shifted for the saturation current this behaviour indicates a long-channel behaviour as confirmed by the output characteristics above. The shift of the cross section is equivalent to a dependence of V_{TH} on V_{DS}, which is a first indication of a drain induced barrier lowering (DIBL) at the contact (cf. section 5.3). Interestingly, this DIBL is not accompanied with additional aspects of short channel behaviour. The transfer characteristics of the L = 100 nm device with the thinner 10 nm oxide show a difference in off-current for the linear (10^{-9} A) and the saturation regime (10^{-7} A). This is typical of the thin oxide's characteristics which show increased charging and displacement currents adding to or subtracting from I_D depending on the potential difference between gate and channel, and due to the increased capacitance in the lower oxide which results in a different time constant RC (R channel resistance, C capacitance) compared to the thicker oxide.

The scaling behaviour of DH4T devices (L = 80 nm to 1 μm) is presented for the mobility (a), the threshold voltage (b), and the on-off ratio (c) in the fig. 9.6. The parameters are calculated both from the linear (left diagrams) and the saturation (right diagrams) regime,

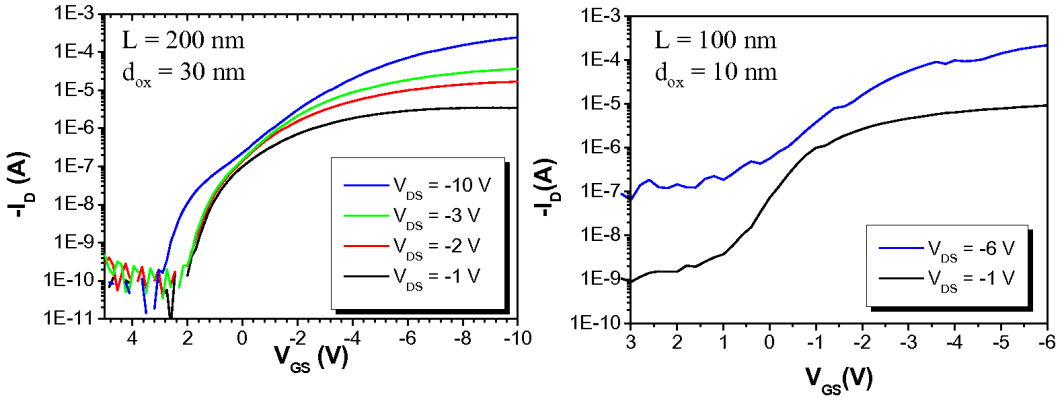


Figure 9.5: *The transfer characteristics of two DH4T FETs on 30 nm SiO_2 (left) with channel length L = 200 nm and on 10 nm SiO_2 (right) with L = 100 nm. The blue curves represent the saturation regime, the others are from the linear regime, the current is in logarithmic scale.*

and for oxide thickness of 10 nm (red points) and 50 nm (black squares). The mobility in the devices increases with increasing channel length in all investigated cases. In this way the still existing influence of the contact resistance in the devices is proved. As expected no influence of grain boundaries in the investigated channel length regime can be found, which would reduce the mobility for the longer channels. The values of μ are lower than the maximum achieved in micrometer devices. However, the 50 nm values in saturation for L $>$ 200 nm are comparable to the micrometer results. All this fits well into the model of a contact limited mobility when reducing the channel. The threshold voltage reveals the beginning of the channel length modulation regime: for 50 nm in the linear regime V_{TH} is constant at a level of $\sim$ 0.6 V for L $\geq$ 200 nm, in saturation at about 1 V for L $\geq$ 400 nm below these channel lengths the V_{TH}-values rapidly increase, so that the characteristic figure of merit for the short channel effect (SCE, cf. section 5.3) ΔV_{TH} is -3.5 V and -5.1 V for linear and saturation values, respectively (cf. tabular 9.1). The calculated value is relative to the maximum investigated channel length of 1 μm. The same evaluation for the 10 nm thick SiO_2 results in a clearly reduced effect. In the linear regime V_{TH} is stable at $\sim$-1 V for L $\geq$ 150 nm with a ΔV_{TH} of -0.5 V and in saturation V_{TH} stays at $\sim$-1.6 V for L $\geq$ 200 nm with a ΔV_{TH} of -1.7 V. The conclusion is that the short channel effect is enhanced by the higher longitudinal electrical field in the saturation regime, which is due to its direct influence on the gradual channel approximation, and the thinner oxide allows an additional reduction of the channel length before the effect appears. Regarding the diagrams of the on/off-ratio scaling in the third row of fig. 9.6, the results confirm the advantages of the thinner oxide concerning the oncoming of short channel behaviour. The values for the 10 nm SiO_2 are larger than the 50 nm results which proves that the off-ratio is not drastically increased for the thin oxide (eg. due to increased leakage or displacement currents). All devices have the same channel width W = 200 μm. The fact that the V_{GS} is usually at a maximum of -6 V for 10 nm instead of -10 V for 50 nm SiO_2 due to the higher risk of oxide breakthrough and the fact that the gate capacitance of the 10 nm SiO_2 is increased by a factor of five results in a higher on-ratio of the thin oxide FETs. The saturation values

(right diagram) also show that for 50 nm SiO_2 the steep reduction of I_{on}/I_{off} already starts below 400 nm whereas for the 10 nm SiO_2 the L = 100 nm value still is on a high level of over 10^5.

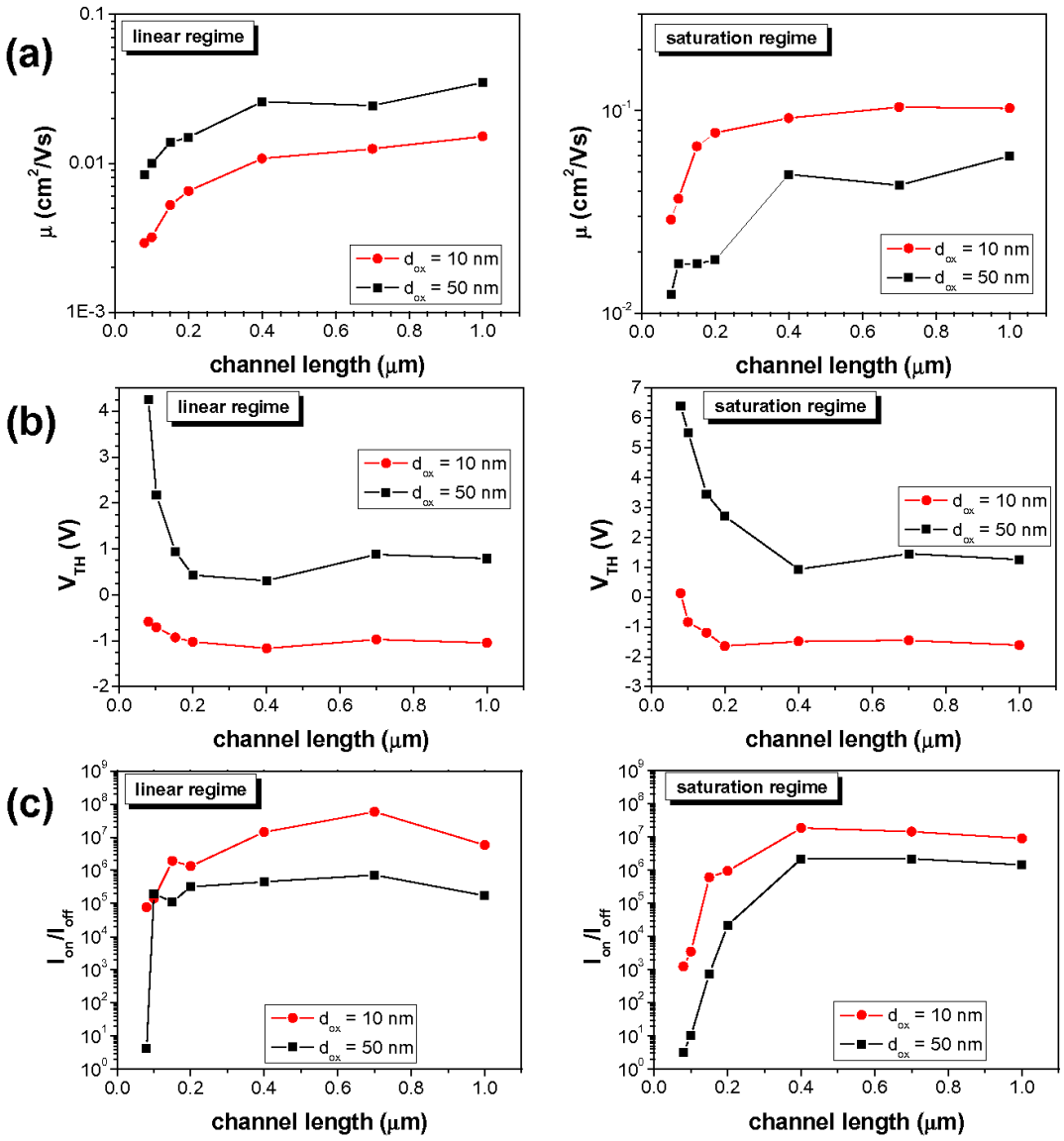


Figure 9.6: *The scaling behaviour of the mobility, threshold voltage, and the on/off-ratio depending on applied insulator thickness (10 nm and 50 nm) of DH4T devices with channel length of 1 μm and below.*

material	d_{ox} (nm)	ΔV_{TH} (V)
DH4T	10	-1.7 (-0.5)
	50	-5.1 (-3.5)

Table 9.1: *ΔV_{TH} values for DH4T FETs with d_{ox} of 10 nm and 50 nm as a measure for the figure of merit of the short channel effect (SCE, cf. section 5.3). The values of the linear regime are in brackets. The threshold voltage difference between L = 100 nm and L = 1 μm devices are taken for the evaluation of SCE.*

9.3 Evaporated dithiophene-tetrathiafulvalene

The following results apply vacuum deposited DT-TTF on transistor templates with 10 nm SiO_2 and channel lengths from 100 nm to 1 μm. They underline the advantage of DH4T concerning the oncoming of short channel behaviour most probably due to the structure of the resulting films. DT-TTF grows three-dimensionally in islands, whereas DH4T forms two-dimensional thin films of large crystalline domains (cf. chapter 2 and especially for DT-TTF appendix D). In fig. 9.7 four fields of output characteristics of DT-TTF FETs are presented. They show the change from short channel to long channel behaviour, when going from the lowest channel length L = 100 nm to the highest L = 1 μm. The characteristics of the device with the smallest channel length (L = 100 nm) mirrors the punch through effect with diode-like, more than linear increase of the current with increasing voltage. The next diagram represents the change to channel length modulated (CLM) behaviour. Here, the characteristics have a nearly linear slope. The next two diagrams (L = 400 nm and L = 1 μm) show the separation in linear and saturation regime, however, with CLM in the saturation. The effect is explicit in the smaller device's characteristics and reduced in the 1 μm OFET. Although the device's channel geometry is a constant W/L = 400 ratio which should scale linearly with the current, the current level depending on V_{GS} decreases for increasing channel length. In the punch through device currents up to 500 μA are reached, whereas the 1 μm OFET only reaches 10 μA. This is another proof for the different transport mode under short channel behaviour, and is a proof for different effective channel width depending on channel length.

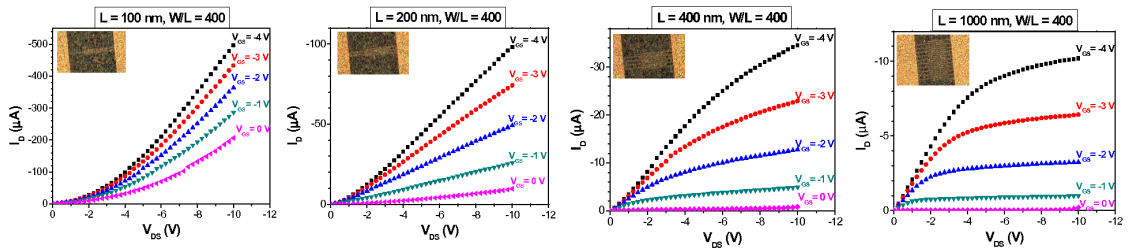


Figure 9.7: *The developing of the output characteristics of vacuum deposited DT-TTF FETs for different channel lengths (L = 100 nm to L = 1μm, W/L is kept constant at 400 μm)*

Using the figure of merit λ for the CLM expressed in output characteristics developed in

section 5.3, the behaviour of the vacuum deposited DT-TTF can be evaluated and compared with the output characteristics of DH4T in fig. 9.3. λ is defined as the negative reciprocal value of the ordinate crossing from the backward extrapolation of the linear increasing saturation current λ = -1/V_{early} (cf. equation 5.16). For p-type characteristics as here, this defines characteristics with $\lambda \approx 0$ V^{-1} and $\lambda < 0$ V^{-1} to express long channel behaviour, and the more negative λ is the more expressed is the CLM effect. By further extending this figure of merit to the characteristic showing PT effect, positive values of λ result from this next grade of short channel behaviour, the nearer to 0 V^{-1} the more expressed is the PT effect. The diagrams of fig. 9.8 present the fitting results of V_{early} and the resulting λ for all above output characteristics and additional ones. The DT-TTF values for the L = 100 nm OFET showing PT is $\lambda = 0.3$ V^{-1}, and for L = 200 nm near 1.7 V^{-1} ($V_{early} \approx 0$ V). The DH4T exhibits better results for 10 nm and 30 nm oxide thickness, in a direct

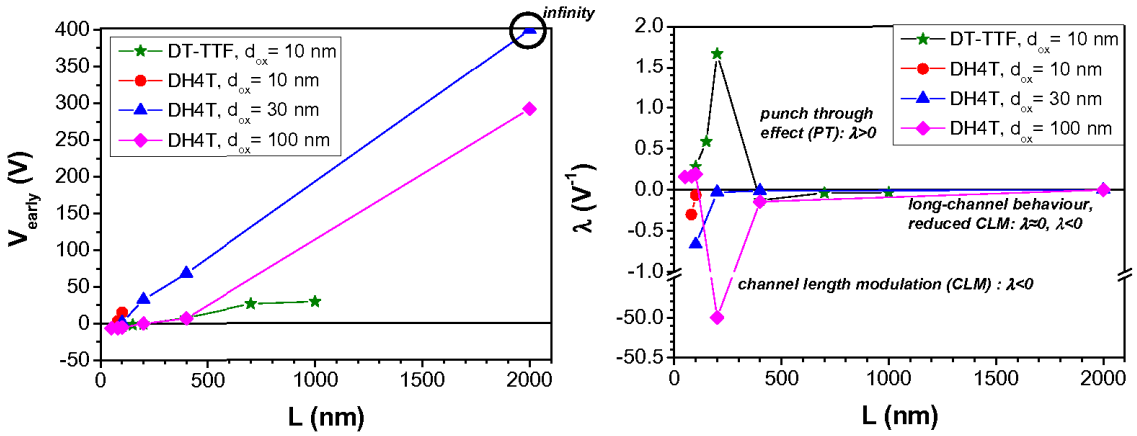


Figure 9.8: *Evaluating figures of merit for short channel behaviour of DH4T and DT-TTF devices.*

comparison the d_{ox} = 100 nm results resemble most the DT-TTF on d_{ox} = 10 nm results, with the exception that the L = 200 nm channel in the case of DH4T still has a positive V_{early} (peak in λ-plot to negative values instead of positive).

The diagram of fig. 9.9 presents a strong DIBL effect on the transfer characteristics investigated with the evaporated DT-TTF FETs of channel length L $\leq$ 1 μm on d_{ox} = 10 nm (corresponding to the output characteristics of fig. 9.7, and additional devices of the same sample). The transfer characteristics in the linear regime (V_{DS} = -1 V) are presented in logarithmic current scale. Their subthreshold regime shifts towards more positive values of V_{GS} for decreasing channel length L. Additionally, the subthreshold slope increases for the smaller channel length. The DIBL effect thus starts for channel length L $<$ 700 nm. However, the off-current level does not change for the different devices. It persists between 10^{-11} A and 10^{-12} A depending on the shifted subthreshold regime. On the one hand, this means that the short channel behaviour is not accompanied by increased leakage or displacement currents and on the other hand, the increasing current level of the on-status for decreasing channel length indicates that the transport is influenced by grain boundaries or a bulk contribution due to the increased longitudinal electrical field

in the smaller channel devices. Because of the same W/L ratio of the compared channel lengths the current level should be equal. Both options, the grain boundary influence and an increased bulk contribution due to higher electrical fields are likely to be present, because of the three-dimensional growth mode of the vacuum deposited DT-TTF (for DB-TTF cf. appendix D). The average layer thickness is more than 10 times higher as for DH4T (>150 nm compared to 13 nm) in order to guarantee a complete film, and the DT-TTF islands grow together from numerous crystallisation centres in the deposition process, which increases the number of grain boundaries relative to the large DH4T single crystalline regimes (of reported size beyond 10 μm [36]).

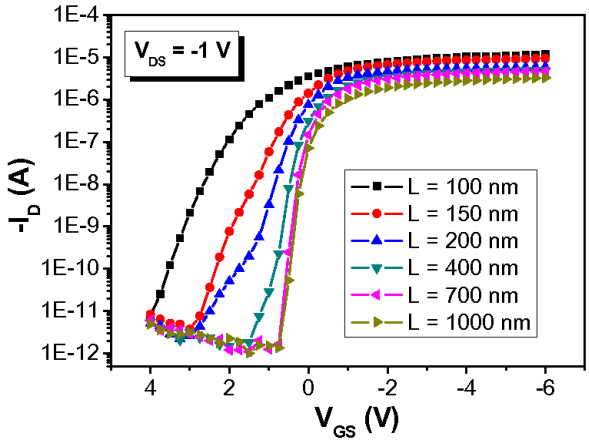


Figure 9.9: *The developing of the transfer characteristics in the linear regime (V_{DS} = -1 V) of vacuum deposited DT-TTF FETs for different channel lengths (L = 100 nm to L = 1 μm, W/L is kept constant at 400 μm). The diagram applies a logarithmic current scale.*

Chapter 10

Lithography on organic layers, the influence on transport

This last experimental chapter is dedicated to the interesting aspect of lithography techniques on the organic semiconductor (OSC). The subject is very appealing from the point of view of the applied aspect of technical physics, because a structuring of the organic semiconductor in any plastic electronics application is necessary. While in the chapters presented before the semiconductor was deposited as a whole layer in a finalising process, the application in e.g. integrated circuits desires a selective deposition (e.g. printing techniques) or the post-deposition structuring of the layer.

Conventional lithography will offer the latter option, if technical and material specific aspects enable compatibility of the steps and materials applied within the processing. In the following the devolution of the transport properties of polytriarylamine (PTAA) FETs will be discussed. The results describe two different lithographic structuring techniques. The first method is a negative lithography process (properly spoken an inverted positive process) on the OSC that structures it using the structured resist as an etching mask in an oxygen plasma (O-plasma) process. The second method is a lift-off process where the PTAA is spin-coated onto a structured layer of photo resist on a transistor electrode template and lifted-off in acetone where it does not stick directly to the SiO_2 or metallised surface. Supplementally to the properties described in the previous chapters, the influence of the conventional lithography and structuring steps on the devices will be analysed from the untreated polymer layer directly after the deposition to the fully O-plasma etch structured layer, and the final result of the lift-off structuring process with PTAA. The special interest lies in the transport properties after the significant processing steps. The finalised transistor in both cases is presented in the micrographs of fig. 10.1. The image a) shows gold (19 nm) on titanium (1 nm) source and drain electrode structures on SiO_2 with the structured OSC on the overlap of the electrode fingers. The remaining PTAA is covered with the photo resist, which served as a shield in the o-plasma etching. Image b) shows similar transistor electrode structures covered with PTAA on the overlap of the fingers. In this case the result

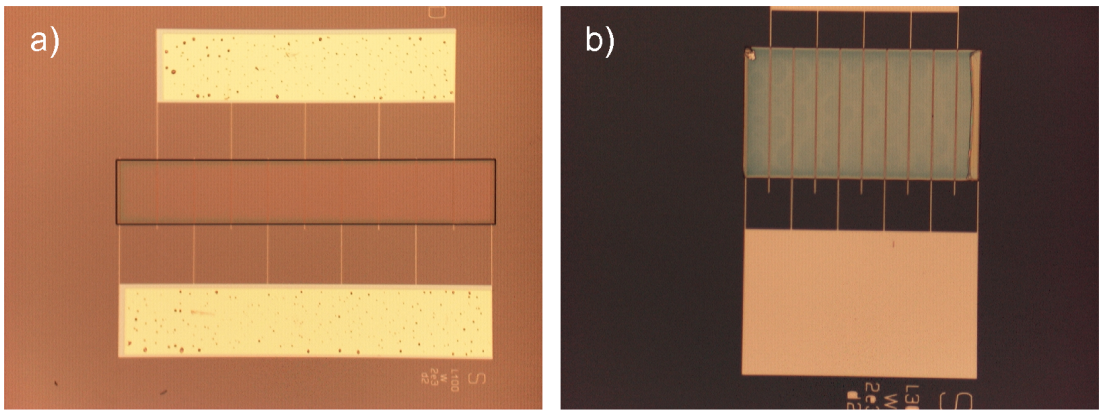


Figure 10.1: *Source and drain electrode structure consisting of 19 nm gold on 1 nm titanium on SiO_2 with a structured layer of PTAA on the overlap of the fingers. a) The result was achieved in an inverted positive lithography process on the organic layer, oxygen plasma etching and lift-off of the remaining resist. b) The structured PTAA results from a lift-off step (cf. appendix B for details).*

was achieved via a lift-off process. The edges of the OSC indicate the different origin of the structured material. In a) they are smooth, while in b) the lift-off process results in rougher and sticking out edges due to the tearing off of the PTAA film in the lift-off.

The lithography technique employed is described in detail in appendix B. The standards in material (resist, developer, lift-off in acetone) were not changed with respect to the standard lithography process applied for metal electrode fabrication. Thus, the method offers a huge variety of applications for the material.

10.1 OFET results of PTAA structured with oxygen plasma etching

The experimental work in this process considers three main steps in the processing of the PTAA FETs including a lithography step and O-plasma etching:

- 1. the spin-coating deposition of the PTAA layer on the electrode structured and pretreated Si/SiO_2 wafer
- 2. the lithography on the PTAA layer (resist deposition, UV exposure, invert bake, UV flash exposure, development of resist)
- 3. the o-plasma etching of the exposed parts of PTAA
- 4. optional: the lift-off of the remaining resist on the PTAA in aceton

Step 4 is denoted as optional. It removes the covering resist from the structured PTAA. In this way it does not bear any advantage for the characterisation method applied here. However, in other processing methods with e.g. additional layers on top of the semiconductor the option might play an important role. The influence of each step on the characteristics of the devices is investigated. In order to give an overview of influences the main device parameters (μ, V_{TH}, and I_{on}/I_{off}) and their scaling behaviour are investigated between the steps. Table 10.1 summarises the observed values for a device with channel length L = 20 μm and a final channel width of 1.8 mm (overlap of the fingers and channel width of the unstructured film is 2 mm). The mobility is not effected much from the lithographic processing it is constant at about 5.5 $\cdot 10^{-5}$ cm^2/Vs. The threshold voltages, however, changes significantly from a positive value of 2.4 V to -3.1 V. The on-off ratio increases after lithography (from 9.5 $\cdot 10^3$ to 2.9 $\cdot 10^4$) but decreases by an order of magnitude after the O-plasma etch to 2.9 $\cdot 10^3$.

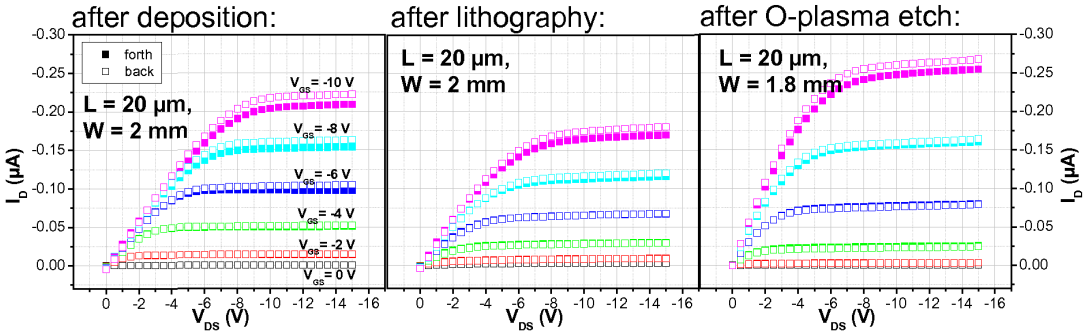


Figure 10.2: *Three fields of output characteristics of a PTAA FET in a lithographic structuring with O-plasma etch. The left diagram describes the characteristics directly after deposition, the middle is after the finished lithography process that covers the active layer on top of metal electrodes, and the right diagram is after structuring in O-plasma leaving only the electrode fingers covered with organic and remaining resist on top. All diagrams apply the same scaling, the characteristics are displayed in forth and back current direction with a gate-source voltage from 0 V to - 10 V in -2 V steps.*

The three diagrams of fig. 10.2 compare directly the resulting output characteristics of the above device after each of the first three steps. From the curves for forth current and backward current direction no significant difference is visible. There is no development of any increased hysteresis in the characteristics. The current of the output characteristics after lithography (middle) is reduced. This is explained by the reduction of the threshold voltage. The corresponding scaling behaviour (L = 1 μm to 75 μm) of the parameters is shown in the three diagrams of fig. 10.4, where the trend of a reduction of V_{TH} between Step 1 and 2 is confirmed for all investigated devices, whereas the mobility for L = 15 μm and L = 20 μm is only slightly reduced (for other devices: decrease by a factor of 2). A significant change of the output characteristics in the third diagram (after structuring, right) is the increase of saturation current for the same V_{GS}, although the channel width is reduced to 1.8 mm and the threshold voltage decreases further. This indicates the reduced

dynamic effects on the characteristics in the case of the now separate to other devices, active semiconducting layer. The parasitic currents (displacement) as in the unstructured complete film disappeared. The transfer characteristics bear another interesting aspect:

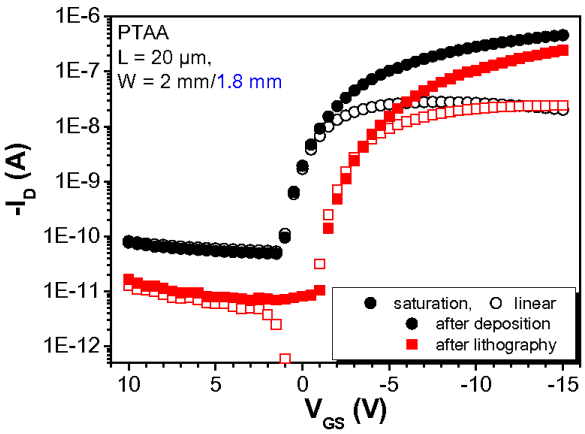


Figure 10.3: *Devolution of the transfer characteristics of a PTAA FET in a lithographic structuring with O-plasma etch. Displayed are the curves in the linear (V_{DS} = -1 V, open symbols) and in the saturation regime (V_{DS} = -15 V, full symbols). The characteristics directly after deposition are in black, the ones after the lithography process covering the active layer on top of metal electrodes are in red.*

while directly after deposition, the devolution of the off-current in saturation and linear regime is the same, the two curves split after the lithography step. This comes hand in hand with the reduction of threshold voltage (for all devices, cf. fig. 10.4). Both effects together can be explained by an increase in trap density in the device. Interestingly, the highest on/off-ratio of the device is after lithography (28966), which is confirmed for all devices in fig. 10.4. The on/off-ratio (fig. 10.4, right diagram) is smallest for the structured

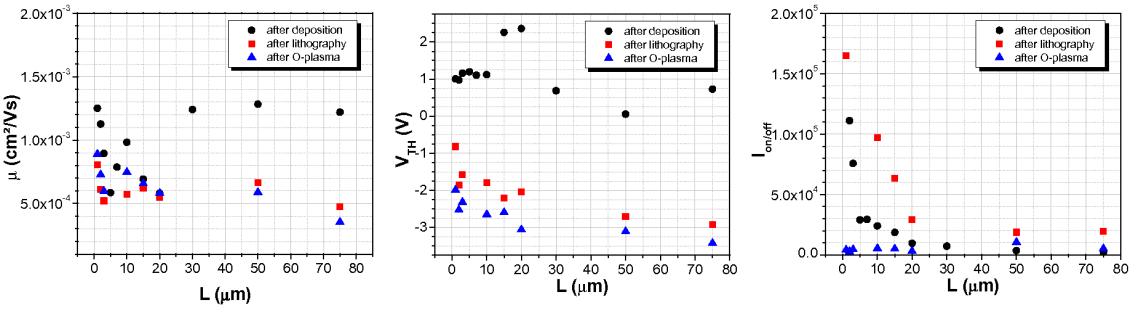


Figure 10.4: *Devolution of OFET device parameters (μ, V_{TH}, I_{on}/I_{off}) depending on channel length during the processing in a lithography process with O-plasma structuring of the PTAA layer.*

device, which indicates the incorporation of oxygen or even an oxidation of the PTAA layer.

The time dependent devolution of the mobility in devices with a channel length from 700 nm to 100 μm during 28 days after a structuring with the O-plasma process is presented in fig. 10.5. The values directly after structuring are day 0, the values before indicate the status after deposition. For smaller channel lengths the structuring results in the increase of mobility, which indicates, that displacement currents in this channel length regime have more influence on characteristics, and in this way on the calculation of the mobility, than

steps	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off} (V/decade)
after deposition	$5.81 \cdot 10^{-4}$	2.4	9504
after lithography	$5.49 \cdot 10^{-4}$	-2.0	28966
after O-Plasma etching	$5.81 \cdot 10^{-4}$	-3.1	2928

Table 10.1: *Comparison of device parameters of a PTAA FET in each step during a lithographic structuring with O-plasma of the active layer. The parameters are calculated from transfer characteristics in the saturation regime.*

for the large micrometer size channels. Before the measurement on day 4 the devices are again (as directly after deposition) annealed to 100 °C for one hour. This has a positive effect on mobility and may be due to reorganisation of the structured layer or final removal of remaining chemicals from the lithography process. After 28 days the average reduction of the mobility relative to its maximum value is about 50%. This is also a realistic value for the ageing influence on the PTAA stored in air.

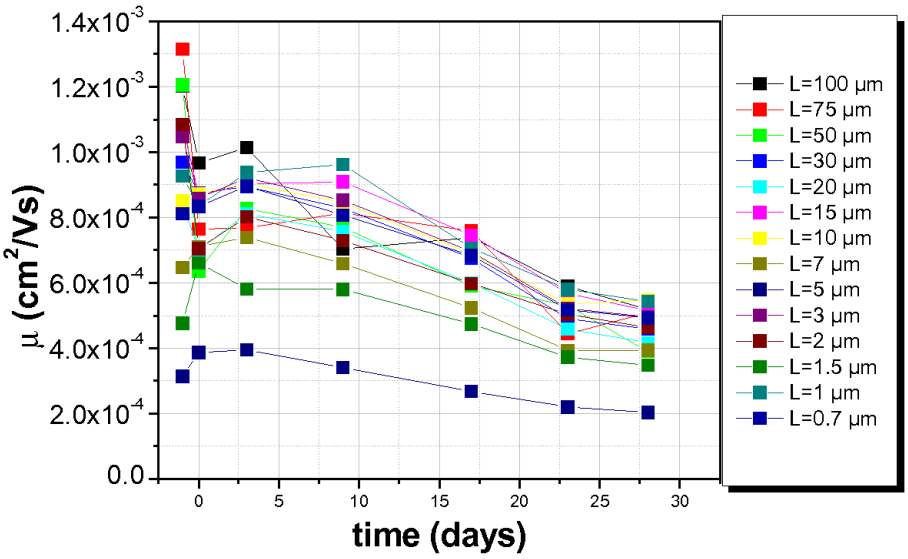


Figure 10.5: *Devolution of the mobility during 28 days of PTAA FETs with channel length from 700 nm to 100 μm in the lithographic structuring with O-plasma process.*

10.2 OFET results of PTAA in a lift-off process

The fabrication of the devices in a lift-off process is carried out in a conventional way, a photo resist on the transistor templates is structured using UV-lithography and an aligned mask that allows the opening of windows in the resist directly over the channel area of the electrodes. Then the PTAA is spin-coated on the patterned resist. The lift-off is done in an acetone bath within 1 minute. Afterwards, the transistor sample is rinsed in water for 10 s. Before characterisation the transistors undergo the standard 100 °C anneal in nitrogen atmosphere for 1 h, to cross-link the PTAA chains.

In order to get sufficient coverage of the PTAA solution (dissolved in toluene) during spin-coating, a thin Novolak resist layer was applied. The layer thickness ratio of PTAA film to resist layer in this case was approximately 100 nm to 600 nm. Additionally, in order to grant a working tearing-off of the film, the resist was overexposed, which yields in relatively flat edges of the opened windows. However, The lift-off in acetone consequently produced an inhomogeneous tearing off of the PTAA layer which is evident from the image of a resulting device in fig. 10.1. At the edges the PTAA film is lifted up.

The output characteristics after the process for two devices (L = 30 μm, L = 75 μm) are presented in the diagrams of fig. 10.6. Due to the approximately double channel length the current scale in the diagram after lift-off is divided in halves for the right diagram (L = 75 μm). From the curves a slight hysteresis between forth current and backward current direction is observed. The device parameters calculated from saturation transfer characteristics for the two devices are listed in tabular 10.2. The mobility is reduced in comparison with the O-plasma structuring results by one order of magnitude. This may be due to the obsolete surface pretreatment of the SiO_2, which was omitted because the PTAA was spin-coated on the structured resist, and also due to the different coating process on a resist patterned substrate. The positive threshold voltage values and the low on/off-ratios, however, indicate that the PTAA layer changed in the lift-off process, it is possible that the acetone solvent influences the film properties by entering into the PTAA or by chemically taking influence.

	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off} (V/decade)
L = 30 μm, linear	$6.36 \cdot 10^{-5}$	0.6	1106
, saturation	$5.85 \cdot 10^{-5}$	1.1	1413
L = 75 μm, linear	$6.61 \cdot 10^{-5}$	0.3	110
, saturation	$6.24 \cdot 10^{-5}$	0.9	235

Table 10.2: *The resulting device parameters of two PTAA FETs structured in a lift-off process.*

The two presented methods give an interesting example of the variety of properties inherent in the many organic semiconducting materials. The polymer layer of PTAA can be manipulated in a way which offers huge possibilities concerning device fabrication. Moreover, the results were obtained without optimising the applied process technology

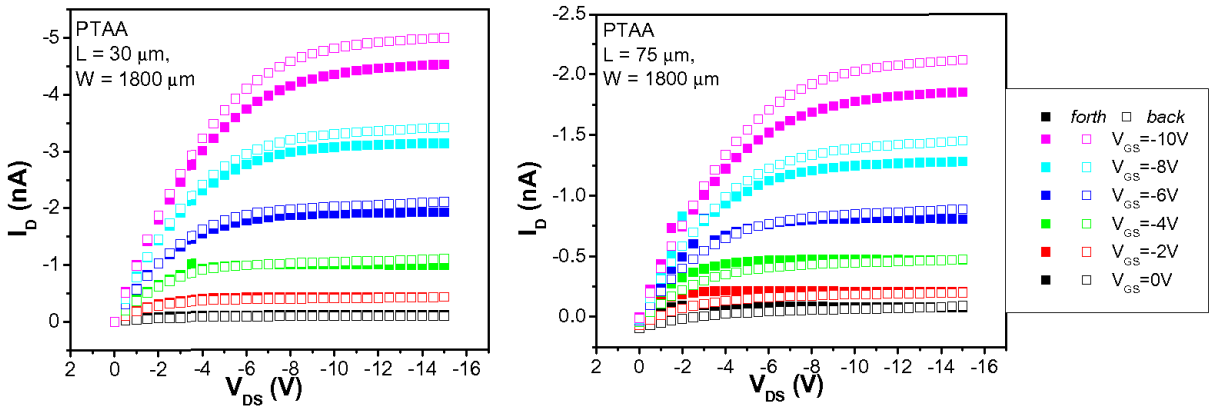


Figure 10.6: *The output characteristics of PTAA FETs (L = 30 µm, L = 75 µm, both W = 1.8 mm) with structured PTAA layer in a lift-off process.*

steps to a great extent. Instead, a very conventional method was applied, which means a huge potential of further optimisation in both presented processes.

Chapter 11

Résumé

Aim and motivation
The present thesis investigates the electrical transport properties of different π-conjugated organic semiconductors applied as active semiconducting material in organic field-effect transistor (OFET) devices.
Theses organic materials are $\alpha\omega$*-dihexylquaterthiophene (DH4T)*, the tetrathiafulvalene (TTF) derivatives *dibenzene-tetrathiafulvalene (DB-TTF)* and *dithiophene-tetrathiafulvalene (DT-TTF)*, and *polytriarylamine (PTAA)*. The latter material is an amorphous polymer, the three others are small molecule oligomer materials.

Materials and their structure
The TTFs were analysed using different deposition methods. One method was the dissolving of the material and the drop-cast deposition of the solution onto prepared transistor templates. After the evaporation of the solvent this yields a crystalline structure of several micrometer size crystals of the TTF. The other method applied was the vacuum evaporation in an organic molecular beam deposition (OMBD) process which results in polycrystalline TTF thin films.

For all DH4T studies the vacuum deposition method was applied. In this case this leads to highly ordered, two-dimensionally orientated thin films of the thiophene derivative. A complete film of 10 nm thickness and even lower can be achieved. In the crystalline phase the DH4T has a very large π-orbital overlap of neighbouring molecules ($\pi\pi$-stacking), which is mirrored in very good intermolecular electronic transport properties. Together with the ability of the hexyl substituents to induce a long-range ordering in thin films the results of the optimised vacuum deposition are highly ordered polycrystalline films with mono-crystalline domain sizes of 10 μm and beyond.

The PTAA is a polymer semiconductor dissolved in polar solvents (e.g. toluene) and spin-coated yielding thin films of the organic semiconductor (thickness of about 100 nm). The material is not designed for the highest electrical transport properties (e.g. high mo-

bility), but for robustness in processing.

Investigations and analytic methods
On the one hand, the investigations in this thesis treat the pure characterisation of the above materials with their different properties in OFET devices. On the other hand, the aim was to observe and analyse general rules and effects in OFETs depending on the structure, previous history, and the device scaling. Therefore, different tools and special analysing methods were developed and applied.

First of all a ***standard characterisation method*** was built up which allowed the direct comparison of different organic semiconductors under the same starting conditions and independently of the transistor template. In order to do that conventional UV-lithography and electron beam metallisation were used to define transistors on silicon wafers with thickness-controlled, thermally grown SiO_2. With this method a series of transistor channel length in the wide range from 500 nm to 100 μm was produced, and moreover, the channel width of transistors and the interdigitated finger size were varied. The controlled fabrication of these templates allows the optimisation for a given organic semiconductor with respect to the pre-treatment and the deposition method. Furthermore, it enables the evaluation of different semiconducting materials and their comparison.

Secondly, the ***temperature dependent electrical characterisation*** allows the investigation of the transport mechanisms inherent in different materials. The large variety in organic semiconductors develops various models ranging from a thermally assisted hopping of localised and polarised states in rather disordered organic semiconductor (e.g. in the case of PTAA), to band-like transport (as known from crystalline anorganic semiconductors (Si, Ge)) in the most ordered systems. Usually the models for band-like transport comprise narrow band influences and trapping and release mechanisms of the charge carriers, as for the poly-crystalline vacuum deposited materials, although they can yield relatively long-range ordered mono-crystalline domains (e.g. in the case of DH4T). In this context the influences of electronic trap states and band tails of the density of states (DOS) into the gap between HOMO and LUMO (**H**ighest **O**ccupied and **L**owest **U**noccupied **M**olecular **O**rbital, respectively) were quantitatively evaluated for the crystalline TTFs.

The in situ measurement method used in connection with the OMBD is presented as a newly developed powerful tool for the characterisation of intrinsic transport properties of organic semiconductors. The special setup permits the electrical characterisation of transistor structures during the finalising deposition of the active organic semiconductor. This offers the chance to observe the during growth behaviour in the growing layers. Moreover, it renders possible the characterisation of OFETs in the ultra high vacuum ($< 10^{-8}$ mbar) of the deposition chamber excluding extrinsic effects, and it allows the evaluation of specific, targeted effects, like the influence of bias stress on the transistor and the influence of atmosphere or defined gases. Additionally, the setup permits the temperature control in the range of $\sim$100 K to 370 K. This method was applied to the DH4T and analogically to the DB-TTF.

In the context of ***downscaling the devices***, the 500 nm limit of the channel lengths range in the standard characterisation was further reduced using electron beam lithography with a special resist system. In this way *sub-micrometer and nanometer channel lengths* were achieved down to 50 nm while keeping a relatively large, technologically challenging channel width beyond 100 μm yielding a high current level and better signal to noise ratio. In the range of sub-micrometer channels the limiting effects of the gate insulator thickness (thermally grown SiO_2) become evident due to the gradual channel approximation (cf. sections 4.3.1 and 5.3). The higher the transversal electrical field ($\propto 1/d_{ox}$, by the capacitance of the gate oxide), the more the oncome of short channel behaviour is reduced. The thickness of the applied SiO_2 layers was reduced from 100 nm down to 10 nm. The oncoming of short channel behaviour, which is a collective term for different effects that deviate from textbook (=long channel) behaviour, was observed and evaluated by several figures of merit (FOM) of the influencing effects. By the variation of channel length and oxide thickness the responsible parameters for the short channel behaviour were investigated and the comparison between the two most appealing candidates in nanometer channels, the DH4T and the DT-TTF, was done.

The PTAA offered opportunities for an interesting technical application. Two different processing techniques which allowed ***the lithographical structuring of the PTAA film*** were applied. Then the resulting OFET devices were analysed relative to the processing with respect to device parameter development and scaling. On the one hand, a standard UV-lithography process was performed on top of the PTAA film, and the layer was structured afterwards by an oxygen plasma etch. On the other hand, the PTAA was structured in a lift-off process that deposited the semiconductor film on top of a structured resist layer and acetone was used to remove (lift-off) the resist and the PTAA selectively on resist. The feasibility of these processes were demonstrated and the electrical results were analysed.

Results and properties of the materials
DH4T: The DH4T is the 'work horse' in this thesis, because of the vaste experience with the vacuum deposited material in the scientific group. The DH4T thin films under investigation are of reproducible and controlled quality so that it was used for the observation of device specific effects, as reference material for new materials, and for the evaluation of measurement methods.

The deposition on 90 °C heated standard templates (oxidised Si-wafers with Titanium-Gold contacts) pretreated with *octadecyltrichlorosilane* (OTS) molecules (cf. appendix B) results in long-range ordered poly-crystalline thin ($\sim$10 nm) films. The reason for this is the growth in a smectic phase of two-dimensional growth of the material at temperatures above 80 °C (cf. sections 2.2.2 and 6.2.1). The best confirmation for the long-range ordering are the achieved high mobility values, which are usually in the order of magnitude of 0.1 cm^2/Vs (up to 0.2 cm^2/Vs). The highest values reported in literature are 0.23 cm^2/Vs [33].

In the thesis the highest values were achieved in the micrometer channel length regime for $L > 10$ μm where the influence of the metal to organic semiconductor contact resistance was neglectable (cf. calculation of the influence of an ohmic contact resistance: equation

5.12 in section 5.2). Regarding the contact material, high work function metals like Gold, Platinum, and Palladium proved good contact to DH4T with pure Palladium achieving the best contact. It yielded a specific resistance value of 0.2 MΩ/mm (cf. section 5.2). Moreover, another result confirmed the essential influence of the often necessary Titanium adhesion layer to SiO_2 under the high work function metal. The highest effective mobility was achieved for 2 nm and below Titanium layer thickness.

This was in close connection with the key results for DH4T in the *in situ* during growth study (cf. section 8.1.1), where the development of the mobility with increasing layer thickness saturated after the first monolayer was completed. On the one hand, this indicated the relevancy of only the first monolayers at the insulator organic interface for the transport in the device. On the other hand, this reflected the nearly ideal two-dimensional growth mode of the films, which was additionally confirmed by an AFM study. Further development in the *in situ* measurement technique yielded the proof of the influence of the filling of the next monolayer on the previous ones by dips in the mobility curve [100]. This was interpreted as a charge carrier trapping mechanism in the incomplete topping layer.

The DH4T films were also used for the *in situ* observation of bias stress influences on the OFET device performance (cf. section 8.1.2). The influence of applied voltages (V_{DS} and V_{GS}) on the characteristics was investigated by keeping the ultra-high vacuum conditions ($< 10^{-8}$ mbar) of the growth chamber after finalising the DH4T-FET, and by excluding the extrinsic effects on the devices at room temperature the stability of the mobility under different working conditions ($\equiv$ bias influences) could be verified for at least 80 days. The sensitive device parameter for bias stress was the threshold voltage V_{TH}. Negative stressing values of V_{GS} reduced V_{TH} (more negative $\equiv$ more closing channel), more positive values of V_{GS} led to a partial recovery of V_{TH} (more positive $\equiv$ more opening channel). The additional application of a drain source voltage V_{DS} in the semiconducting channel (always negative as for driving a p-type device) contributed to the reduction of V_{TH}. The analysed devices showed an irreversible shift of V_{TH} to a relaxation voltage level following the first stressing. This can be explained by a structural relaxation in the thin film. At this relaxation level any supplemental stressing proved reversible, where the relaxation could be characterised by a memory effect concerning the 'stressing sign' before the relaxation (V_{DS} or V_{GS} negative opposite to V_{GS} positive). This memory effect was found characteristic of the DH4T and comprised a V_{TH}-range of $\sim$0.15 V. The origin of the discovered effects is supposed to be in the microscopic structure of the interfaces. Models are based on traps in the semiconductor material, in the insulator, or at the interface of both, which lead to reversible trapping and detrapping mechanisms in connection with a polaronic charge carrier transport.
The temperature dependent analysis of the stressing behaviour (cf. section 8.1.3) supported these models. It proved that also the mobility is influenced by temperature values higher than room temperature. All shifts were relatively increased with increasing temperature.

In submicrometer devices (cf. chapter 9) the thin films of DH4T were the best candidates among the investigated materials for the downscaling of the channel length while avoiding short channel behaviour (cf. section 5.3) and keeping the textbook behaviour. The

reduction of channel lengths down to 50 nm on reduced insulator layers (thickness down to 10 nm SiO_2) led to L = 80 nm devices showing only first indications of a short channel behaviour. The good properties in sub-micrometer devices of the DH4T are attributed to the highly ordered two-dimensional structure that avoids perturbing effects in the bulk material.

TTF derivatives: The TTF materials are new candidates among the organic semiconductor materials. The variation of the structure from single crystalline by a drop-cast deposition to poly crystalline by the vacuum evaporation was a further attracting aspect of the thesis. The standard characterisation of the crystalline DT-TTF yielded the highest mobility (3.65 cm^2/Vs) achieved for the TTFs, the single crystalline DB-TTF ranged an order of magnitude lower in mobility (cf. section 6.1). Moreover, the value is, to the best of our knowledge, the highest mobility reported for a solution processed OFET. This exemplary result clarified the potential in the TTF material group. Furthermore, other published single crystalline OFET outcomes usually resulted from elaborate growing and device processing techniques and had no comparably low channel length (below 100 μm) as investigated on the standard templates.

The influence of traps in the materials was analysed in temperature dependent measurements (cf. chapter 7). The temperature dependent behaviour of the mobility was explained by a multiple trapping and release, band-like transport that showed a bi-exponential activation of the mobility. Furthermore, from the activation of the drain current in transfer curves a calculation of exponentially decreasing band tails of the density of states (DOS) into the forbidden gap of the materials was derived. The two methods independently found trap levels at 20 meV and 100 meV for DT-TTF and at 50 meV and 85 meV for DB-TTF above the HOMO energy level. The results comfirmed, that the solution processing of the materials still yielded a relatively high trap density, which differentiated them from some other single crystal result showing no or even negative temperature activation.

The vacuum deposited variants of the two TTFs built a poly-crystalline thin film structure. An extensive atomic force microscopy analysis for the DB-TTF proved a Vollmer-Weber growth of the molecule (cf. appendix B) also confirmed for the DT-TTF. This three-dimensional growth in islands that grow together was a major difference in comparison with the also vacuum deposited DH4T. Therefore, grain boundary influences were much more present in the TTFs. As a consequence the mobility in comparison with the single crystalline results decreased to more than an order of magnitude lower with the maximum found in DT-TTF poly-crystalline FETs of 0.07 cm^2/Vs (cf. section 6.2.2). Moreover, the behaviour of DT-TTF in sub-micrometer channel FETs was inferior to DH4T (and DB-TTF even worse), presumably due to the increase of bulk material influence. Regarding the short channel behaviour the DT-TTF films in 10 nm SiO_2 behaved comparably to DH4T on a thicker 100 nm SiO_2 (cf. section 9.3).

For DB-TTF the characteristics of the mobility in *in situ* during growth studies (cf. section 8.2) also differed from DH4T. The two-dimensional growth specific saturation of the mobility was missing. Instead, the mobility increased with increasing layer thickness. On

the one hand, this can be attributed to a reduction of the grain boundary influence because more and more islands continuously grew together and completed the film between the electrodes, but on the other hand, it also indicates a strong influence of the volume material on the extraction of the mobility from transfer characteristics. This fundamental difference to DH4T continued in *in situ* stressing experiments, where for DB-TTF the V_{TH} was only influenced under stress by a depleting, positive V_{GS}, and due to a breakage of the ultra-high vacuum.

PTAA: The last material of the investigation, the PTAA achieved values of mobility in the order of 10^{-3} cm^2/Vs in the standard characterisation. These values competed well with reported literature values (cf. sections 2.3.1 and 6.3). The low results relative to the oligomer materials's mobilities were caused by the reduced order accompanied by a hopping transport mechanism in the amorphous polymer films. The excellent properties of the material concerning robustness in fabrication processes could be proved by the successful integration of PTAA films in conventional UV-lithographical structuring processes. Here, a oxygen plasma etch of PTAA as active material in OFETs using a structured photoresist mask as well as a lift-off of PTAA on structured photoresist in acetone yielded promising results.

Conlusion

Concluding, the below table summarises the exemplarily relevant OFET device parameters resulting from the standard characterisation of the investigated materials.

material	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DH4T	100	1400	33	0.13 (0.13)	1.75 (0.92)	2.4 (0.3) $\cdot 10^5$	0.50 (0.46)
DT-TTF (cryst)	30	10	33	3.65 (3.65)	1.16 (1.20)	5.1 (1.2)$\cdot 10^7$	-0.45 (-0.51)
DT-TTF (poly)	20	2000	33	0.066 (0.068)	-1.57 (-1.23)	2.0 (0.1) $\cdot 10^7$	0.22 (0.13)
DB-TTF (cryst)	2	100	33	0.41 (0.24)	1.09 (1.08)	0.8 (4.1)$\cdot 10^5$	-1.82 (-1.1)
DB-TTF (poly)	20	$2 \cdot 10^5$	66	0.039 (0.023)	4.75 (4.50)	1.4 (0.1) $\cdot 10^7$	0.30 (0.33)
PTAA	10	10^5	66	3.39 (4.77) 10^{-3}	1.85 (0.73)	74.3 (6.3) 10^4	-0.23 (-0.23)

Table 11.1: *Geometry and device parameters for optimised OFET of all investigated materials. The device parameters in brackets are from the linear regime, the others from saturation. Single crystalline and vacuum deposited poly-crystalline TTF material are denoted (cryst) and (poly), respectively. L is the channel length of the OFET, W the channel width, C_i the gate insulator capacitance per area, μ the mobility, V_{TH} the threshold voltage, $I_{on/off}$ the on-off ratio, and S the subthreshold swing (cf. section 5.1).*

Chapter 12

Zusammenfassung (German)

Ziel und Motivation
Die vorliegende Dissertationsarbeit untersucht die elektrischen Transporteigenschaften mehrerer π-konjugierter organischer Halbleiter. Diese werden zu diesem Zweck in organische Feldeffekttransistoren (OFET) als aktive halbleitende Schicht eingebaut.
Bei den halbleitenden Verbindungen handelt es sich um $\alpha\omega$-*Dihexylquaterthiophen (DH4T)*, die Tetrathiafulvalenverbindungen (TTF) *Dibenzen-Tetrathiafulvalen (DB-TTF)* und *Dithio-phen-Tetrathiafulvalen (DT-TTF)* und um *Polytriarylamin (PTAA)*. Bei letzterer Verbindung handelt es sich um ein amorphes Polymer, die drei anderen sind oligomere Verbindungen.

Materialeigenschaften und -strukturen
Die Tetrathiafulvalene DB- und DT-TTF wurden in der Arbeit auf zwei verschiedene Arten abgeschieden. Zum einen wurden die Materialien gelöst als Flüssigkeit im Drop-Cast-Verfahren auf fertige Transistortemplate aufgetropft. Dieses Verfahren bildet nach Verdampfen des Lösungsmittels Einkristalle der Stoffe von einigen Mikrometern Länge. Zum anderen wurden sie im Verfahren der organischen Molekularstrahldeposition (engl.: organic molecular beam deposition , OMBD) im Ultrahochvakuum ($p<10^{-8}$ mbar) aufgedampft. Auf diese Weise entstehen polykristalline Dünnschichten der Materialien.

Beim DH4T wurde ausschließlich die Vakuumdeposition (OMBD) verwendet. Hierbei bilden sich besonders langreichweitige, zweidimensional geordnete Dünnschichten des Thiophenderivats. Ein geschlossener Film von 10 nm Dicke und geringer ist im Verfahren mit dem Material möglich. In seiner kristallinen Phase hat das DH4T einen großen Überlapp der π-Orbitale zwischen benachbarten Molekülen (engl.: $\pi\pi$-stacking). Dieser Überlapp spiegelt sich in sehr guten zwischenmolekularen elektrischen Transporteigenschaften wider. Ein Vorteil der Hexyl-Substituenten, im Vergleich zu unsubstituiertem Quaterthiophen, ist zudem eine verbesserte langreichweitige Ordnung der dünnen Filme. Daher ergeben sich aus der optimierten Vakuumdeposition des DH4T hochgeordnete Dünnschichten mit monokristallinen Bereichen bis 10 μm und größer (in einer Richtung).

Das PTAA hingegen ist ein polymerer, also langkettiger organischer Halbleiter, der in polaren Lösungsmitteln gelöst, nach der Spin-Coating-Deposition eine geschlossene Dünnschicht bildet (Schichtdicken etwa 100 nm). Das Material zeigt auffallend gute Widerstandsfähigkeit gegenüber verschiedenen Prozesstechniken und wird im Rahmen der Dissertation lithographisch strukturiert in OFETs angewendet. Die Eigenschaft der amorphen Schichten ermöglicht etwa die Untersuchung anisotroper Transporteigenschaften, die etwa durch den Bauteilaufbau hervorgerufen werden.

Untersuchungen und analythische Methoden
Zum einen werden im Zuge dieser Dissertationsarbeit die Eigenschaften der oben genannten organischen Halbleiter untersucht und charakterisiert. Zum anderen war das Ziel der Arbeit, allgemein gültige Gesetzmäßigkeiten und Effekte in OFETs zu erklären. Hierbei wird speziell der Einfluss der Struktur der Halbleiter, ihre Zeit- und Umweltbeständigkeit und die Abhängigkeit von der Bauteilskalierung untersucht. Verschiedene Apparaturen und Analysemethoden wurden zu diesem Zweck genutzt und teilweise dafür entwickelt.

Zuallererst wurde eine ***Methode zur Standardcharakterisierung von Bauteilen und Halbleitern*** entwickelt. Sie ermöglicht den direkten Vergleich verschiedener organischer Halbleiter unter gleichen Voraussetzungen unabhängig von den verwendeten Transistortemplaten. Hierzu wurden mittels konventioneller UV-optischer Lithographie und Elektronenstrahlmetallisierung Transistorstrukturen auf thermisch oxidierten Siliziumwafern hergestellt. Diese sind ausgehend vom Substrat gleich. So wurden Template bereitgestellt, die einen großen Kanallängenbereich von 500 nm bis 100 μm abdecken, sowie Transistoren mit variierender Kanalbreite und Elektrodenfingerbreite vorweisen. Das erlaubt zum einen die Untersuchung und Optimierung der Templatvorbehandlung und der Materialdeposition bei den untersuchten organischen Halbleiter. Zum anderen ermöglicht es den direkten Vergleich unterschiedlicher Materialien.

Desweiteren wurden ***temperaturabhängige elektrische Charakterisierungen*** durchgeführt. Hierdurch erhält man Informationen über den vorliegenden Transportmechanismus im Materialsystem. Die große Vielfalt an organischen Halbleitern resultiert in zahlreichen unterschiedlichen Transpormodellen. Sie reichen von einem thermisch angeregten “Hopping”-Transport in lokalisierten und polarisierten Zuständen, vorliegend in ungeordneten Systemen wie z.B. dem PTAA, bis zu bandartigem Transport in den am meisten geordneten organischen Halbleitern, wie er etwa von anorganischen kristallinen Halbleitern (Si, Ge) bekannt ist. Störungseinflüsse bei den organischen Halbleitern sind deutlich erhöht. Sie sind etwa in den Modelle zum Band-Transport durch die Schmalbandtheorie oder allgemeiner das Einwirken von elektrischen Fallenzuständen durch einfangen und thermisch induziertes freilassen der Ladungsträger (engl.: multiple trapping and release, MTR) erfasst. Dieser Transportmechanismus liegt in vielen poly-kristallinen Halbleitern aufgrund der Korngrenzen zwischen den einkristallinen Domänen vor, wie z.B. beim DH4T. In dem Zusammenhang werden der Einfluss elektronischer Fallenzustände und der Verlauf der Zustandsdichte (engl.: density of states, DOS) im Energiebereich zwischen HOMO und LUMO (engl.: **H**ighest **O**ccupied bzw. **L**owest **U**noccupied **M**olecular **O**rbital) analysiert. Diese sogenannten “band tails” wurden für einkristallines TTF quantitativ ausgewertet.

Eine neu entwickelte und sehr aussagekräftige Analysemethode im Zusammenhang mit der Vakuumdeposition (OMBD) ist die ***in situ Messmethode***. Sie wurde im Rahmen der Dissertation zur Untersuchung intrinsischer Transporteigenschaften organischer Halbleiter genutzt. Der spezielle Aufbau gestattet die elektrische Charakterisierung von Transistorstrukturen während der abschließenden Vakuumdeposition des aktiven Materials. Dadurch kann das Verhalten des Bauteils während des Schichtwachstums beobachtet werden. Außerdem ermöglicht die Methode, die OFETs nach Fertigstellung und ohne Unterbrechung des vorliegenden Ultrahochvakuums ($< 10^{-8}$ mbar) zu charakterisieren. Hierdurch werden extrinsische Effekte ausgeschlossen. Somit ist die *in situ* Analyse ideal, spezifisch und gezielt Effekte zu untersuchen, wie etwa den Einfluss von Stress durch angelegte Spannungen oder das Einwirken von Atmosphäre und Einzelgasen durch selektiven Einlass. Zusätzlich zu diesen Möglichkeiten kann die am OFET vorliegende Temperatur zwischen $\sim$100 K und 370 K variiert werden. Mit dieser Methode wurde das DH4T und ebenso das DB-TTF untersucht.

Im Zusammenhang mit der ***Herunterskalierbarkeit von Bauteilen*** wurde das untere Kanallängenlimit der OFETs von 500 nm der Standardcharakterisierungstemplate mittels Elektronenstrahllithographie auf speziellen Resistsystemen weiter reduziert. Auf diese Weise wurden Kanallängen im *Submikrometerbereich bis zu Nanometerkanälen* bis 50 nm erzeugt. Zudem wurde hierbei die Kanalbreite technologisch herausfordernd auf über 100 μm gehalten. So konnten die Vorteile der kleinen Kanallängen, wie etwa ein verringerter Einfluss von Korngrenzen, verbunden mit einem hohen Stromlevel (skaliert mit W/L) und dadurch besserem Signal-zu-Rauschen-Verhältnis untersucht werden. Im Bereich der Submikrometerkanäle wurde der Einfluss des Dielektrikums (thermisch gewachsenes SiO_2) deutlich. Der Einfluss ist durch die "Gradual Channel"-Näherung begründet, die eine Voraussetzung des idealen OFET darstellt. Sie besagt, dass das elektrische Feld im Kanal zwischen "source" und "drain" des Transistors hinreichend klein gegenüber dem transversalen Feld, gesteuert durch die Gatespannung, bleibt. Das elektrische Feld im Kanal steigt mit sinkender Kanallänge. Durch Reduzierung des standardmäßig 100 nm dicken SiO_2 auf bis zu 10 nm konnte die Kapazität pro Fläche erhöht und das transversale Feld entsprechend angepasst werden. Das Auftreten von Kurzkanalverhalten, ein Überbegriff verschiedenster Effekte, stellt eine Abweichung vom Standardverhalten dar. Diese Effekte wurden mit Hilfe ihnen zugeordneter Größen beobachtet und bewertet. Durch die Variierung von Kanallänge und Oxiddicke wurden die Einfluss nehmenden Größen untersucht und dahingehend DH4T mit DT-TTF verglichen, die zwei besten Kandidaten unter den untersuchten Materialen für Nanometerkanäle.

Das PTAA bot die Möglichkeit für eine interessante technische Anwendung: zwei verschiedene Prozesstechniken, die OFETs unter ***lithographischer Strukturierung des PTAA-Film*** herstellen, wurden hier angewandt. In der ersten Prozesstechnik wurde auf der PTAA-Schicht mittels konventioneller UV-optischer Lithographie ein Lackfilm strukturiert und danach das PTAA gezielt in Sauerstoffplasma geätzt. In der zweiten wurde das PTAA in einem "Lift-off"-Prozess strukturiert. Dieser brachte zuerst die Halbleiterschicht auf einen lithographisch strukturierten Lack auf und entfernte selektiv mittels Aceton (lift-off) das PTAA mit dem Lack darunter. Die mit Hilfe dieser Techniken entstandenen OFETs wur-

den auf ihre Kenngrößenentwicklung und ihr Skalierungsverhalten hin untersucht und verglichen. Die Machbarkeit dieser Prozesse wurde demonstriert und die elektrischen Ergebnisse analysiert.

Ergebnisse und Materialeigenschaften
DH4T: Das DH4T stellt das "Arbeitspferd" der Dissertation dar, da zu diesem vakuumdeponierte Material in der Arbeitsgruppe die umfangreichste Erfahrung vorliegt. Die aufgebrachten und untersuchten Dünnschichten des DH4T sind von hoher Qualität und Reproduzierbarkeit. Aus diesem Grund diente das Material zur Untersuchung bauteilspezifischer Effekte, als Referenzmaterial für neue Materialien und zur grundsätzlichen Bewertung von Messmethoden.

Durch Aufbringen auf 90 °C temperierte Standardtransistortemplate (oxidierte Si-Wafer mit Titan/Gold Kontakten), die mit *Octadecyltrichlorosilan* (OTS) Molekülen (vergleiche Anhang B) vorbehandelt sind, entstehen langreichweitig geordnete polykristalline Dünnschichten (nur etwa ∼10 nm Dicke). Dies ist bedingt durch das Wachstum in einer zweidimensional ordnenden Phase des Materials bei Temperaturen über 80 °C (vergleiche die Abschnitte 2.2.2 und 6.2.1). Der beste Beweis für die langreichweitige Ordnung sind die erzielten hohen Beweglichkeitswerte, die üblicherweise in der Größenordnung von 0,1 cm^2/Vs liegen. Die höchsten erzielten Werte von bis zu 0,2 cm^2/Vs) sind vergleichbar mit in der Literatur berichteten Höchstwerten von 0,23 cm^2/Vs [33].

In der Dissertation wurden diese maximalen Beweglichkeitswerte für das DH4T im hohen Mikrometerkanallängenbereich erreicht ($L > 10\ \mu m$). Hier ist der Einfluss des metall-organischen Kontaktwiderstandes vernachlässigbar (siehe Gleichung 5.12 in Abschnitt 5.2). Diesbezüglich ergab sich für Kontaktmaterialien mit einer hohen Austrittsarbeit wie Gold, Platin und Palladium der beste Kontakt zum DH4T. Unter ihnen hatte das Palladium den geringsten Kontaktwiderstand mit einem Wert für den spezifischen Widerstand von 0,2 MΩ/mm (vergleiche Abschnitt 5.2). Weiterhin bestätigte sich, dass die oftmals nötige Titanhaftvermittlungsschicht zwischen Edelmetall und SiO_2 entscheidenden Einfluss auf den Widerstand zur DH4T-Schicht hat. Die effektiv höchsten Beweglichkeiten wurden für Titandicken unter 2 nm unter Gold erreicht.

Der letzte Sachverhalt ist in engem Zusammenhang mit dem Hauptergebnis zum DH4T der *in situ* Studie während des Schichtwachstums (vergleiche Abschnitt 8.1.1) zu sehen. Es zeigte sich bei der Entwicklung der Beweglichkeit mit wachsender Schicht bereits unmittelbar nach Deposition der ersten Monolage eine Sättigung. Einerseits weist dies die Bedeutung der ersten Monolage für das Gesamttransportverhalten im Bauteil nach, andererseits spiegelt das Ergebnis das nahezu ideale zweidimensionale Wachstum der Schicht in der Vakuumdeposition wider. Dies wurde durch eine Rasterkraftmikroskopiestudie der Schichten bestätigt. Durch eine Weiterentwicklung der Messtechnik im *in situ* Verfahren gelang der Nachweis, dass nach jedem Füllen einer Lage die Beweglichkeit kurz abfällt. Hier zeigt sich der Einfluss der noch nicht zusammenhängenden nächsten Monolage auf die komplette darunterliegende Lage [100]. Dieser Effekt wurde mit dem Einfangen von Ladungsträgern in der unvollständigen nächsten Schicht interpretiert.

Die DH4T Dünnschichten wurden weiterhin dazu benutzt, mittels *in situ* Messmethoden den Spannungsstresseinfluss auf die Leistungsfähigkeit der OFETs (vergleiche Abschnitt 8.1.2) zu beobachten. Der Einfluss angelegter Spannungen (V_{DS} und V_{GS}) auf die Transistorkennlinien wurde ohne vorherige Unterbrechung des Ultrahochvakuums ($< 10^{-8}$ mbar) in der OMBD-Anlage nach Abschluss der Deposition untersucht. Damit schließt man extrinsische Einflüsse auf den fertigen DH4T-FET weitestgehend aus. Die Stabilität der Transistoren bei Raumtemperatur und unter verschiedensten Anwendungsbedingungen ($\equiv$ Spannungsansteuerungen) konnte für einen Zeitraum von mindestens 80 Tagen nachgewiesen werden. Die beeinflusste Kenngröße in diesem Zusammenhang war ausschließlich die Schwellspannung V_{TH}. Negative Stressspannungen V_{GS} verringerten V_{TH} (Negatives $V_{TH} \equiv$ geschlossenerer leitender Kanal). Positivere Werte V_{GS} führten hingegen zur teilweisen Zurückführung des vorher verschobenen Wertes von V_{TH} (Positives $V_{TH} \equiv$ geöffneterer leitender Kanal). Ein zusätzliches Anlegen einer Kanalspannung zwischen "drain" und "source" V_{DS} im aktiven Kanal (Wert immer negativ wie bei Löcherleitungstypen üblich) trug weiter zur Verringerung von V_{TH} bei. Die untersuchten OFETs zeigten eine irreversible Verschiebung von V_{TH} bis zu einem Relaxationswertebereich direkt nach dem ersten Stress. Dies kann mit einer strukturellen Relaxation in der Dünnschicht durch Anlegen der Spannung erklärt werden. In diesem Relaxationswertebereich erwies sich zusätzliches Stressen des Bauteils als reversibel. Hierbei war die Relaxation charakterisiert durch einen Erinnerungseffekt bezüglich des Vorzeichens der angelegten Spannung (des Stressvorzeichens: einerseits V_{DS} oder V_{GS} negativ, andererseits V_{GS} positiv und V_{DS} = 0 V). Dieser Erinnerungseffekt stellte sich als spezifisch für DH4T heraus und umfasste in allen Fällen einen V_{TH}-Bereich von etwa 0,15 V. Die Ursache dieses neuentdeckten Effekts wird in der mikroskopischen Struktur der Grenzschichten vermutet. Vorgestellte Modelle basieren auf Fallenzuständen im Halbleiter selbst, im Dielektrikum oder direkt an deren Übergang ineinander. Diese führen zu einem reversiblen "trapping and release" Mechanismus im Zusammenhang mit polaronischem Ladungsträgertransport.
Die Analyse des temperaturabhängigen Stressverhaltens (vergleiche Abschnitt 8.1.3) unterstützt diese Modelle. Es stellte sich heraus, dass auch die Beweglichkeit bei Temperaturen über Raumtemperatur beeinflusst wird. Alle Verschiebungen nahmen mit steigender Temperatur zu.

Bei den Transistoren mit Kanallängen im Submikrometerbereich erzielten die DH4T-Dünnschichten bezüglich des Herunterskalieren der Kanallänge bei gleichzeitigem Erhalt des Langkanalverhaltens die besten Ergebnisse unter den untersuchten Materialien (siehe Kapitel 9). Durch Reduzierung der Kanallängen bis zu 50 nm auf bis zu 10 nm dünnem SiO_2 Dielektrikum entstanden Bauteile im Nanometerkanalbereich, die nur erste Anzeichen eines leichten Kurzkanalverhaltens (vgl. Abschnitt 5.3) zeigten. Dies gilt für Kanäle bis zu L = 80 nm. Die gute Eignung von DH4T in Submikrometertransistoren wird auf den hochgeordneten zweidimensionalen Aufbau der Schichten zurückgeführt, wodurch störende Effekte, etwa im Volumenmaterial, verhindert werden.

TTF-Derivate: Die TTF-Materialien sind relativ neue Kandidaten unter den organischen Halbleitern. Daher war für diese Arbeit der Unterschied durch die verschiedenen Her-

stellungsverfahren zwischen einkristalliner und polykristalliner Struktur von großem Interesse. Die Standardcharakterisierung des einkristallinen DT-TTFs erbrachte die höchste gemessene Beweglichkeit (μ = 3,65 cm^2/Vs) aller untersuchten Materialien (siehe Abschnitt 6.1). Das einkristalline DB-TTF rangierte hier etwa eine Größenordnung niedriger. Der Wert für DT-TTF stellt nach unserem besten Wissen den höchsten in der Literatur genannten Beweglichkeitswert für einen lösungsprozessierten OFET dar. Dieses beispielhafte Ergebnis macht das Potenzial der TTF-Materialien deutlich. Außerdem waren die meisten anderweitig veröffentlichten Ergebnisse zu einkristallinen organischen Halbleitern zumeist durch sehr aufwendige Reinigungs- und Aufbringverfahren verwirklicht und untersuchten deutlich größere Kanallängenbereiche als den interessanten Bereich unter 100 μm im Fall dieser Arbeit.

Der Einfluss von Fallenzuständen in den einkristallinen TTFs wurde anhand temperaturabhängiger Messungen analysiert (vgl. Kapitel 7). Das temperaturabhängige Verhalten der Beweglichkeit wurde dabei anhand eines MTR-Modells mit bi-exponentieller Temperaturaktivierung erklärt. Weiterhin konnten über das Aktivierungsverhalten des *Drain*-Stroms I_D in Transferkurven exponentiell abfallende "band tails" im Energiebereich zwischen HOMO und LUMO berechnet werden. Deren Verlauf und die Aktivierungsenergie aus dem MTR-Modell ergaben unabhängig voneinander Fallenzustandslevel bei 20 meV und 100 meV für das DT-TTF und bei 50 meV und 85 meV für das DB-TTF, jeweils oberhalb des HOMO-Levels. Diese Ergebnisse bestätigen, dass die lösungsbasierte Prozessierung der Materialien eine relativ hohe Fallenzustandsdichte hervorruft, was sie von anderen Einkristallresultaten organischer Halbleiter unterscheidet, bei denen keine oder sogar negative Temperaturaktivierung nachgewiesen wurde.

Die vakuumdeponierten Varianten der beiden TTFs bilden eine polykristalline Dünnschichtstruktur. Eine umfangreiche Rasterkraftmikroskopieanalyse des DB-TTFs wies ein *Vollmer-Weber* Wachstumsmechanismus der Moleküle auf SiO_2 nach (vgl. Anhang B). Es wurde auch für DT-TTF bestätigt. Dieses dreidimensionale Wachstum des Materials in zusammenwachsenden Inseln ist der Hauptunterschied im Vergleich mit dem ebenfalls vakuumdeponierten DH4T. Deshalb lag bei den TTF-Schichten ein größerer Einfluss von Korngrenzen vor. Eine Folge davon war, dass die Beweglichkeitswerte im Vergleich zu den einkristallinen Varianten, um mehr als eine Größenordnung sanken. Die maximalen Werte für OFETs erbrachte wiederum das DT-TTF mit 0,07 cm^2/Vs (siehe Abschnitt 6.2.2). Außerdem war die Leistungsfähigkeit des DT-TTFs in Submikrometerkanal FETs heruntergesetzt im Vergleich zu DH4T (DB-TTF rangierte hier noch schlechter). Die Ursache dafür ist der deutlich erhöhte Einfluss des Volumenmaterials. Bezüglich des Auftretens von Kurzkanalverhalten sind DT-TTF Dünnschichten auf vorteilhaftem 10 nm dünnen SiO_2 in etwa mit DH4T auf zehnmal dickerem SiO_2 (vgl. Abschnitt 9.3) vergleichbar.

Auch beim Vergleich des Beweglichkeitsverhaltens während des Schichtwachstums in der *in situ* Charakterisierung unterschieden sich DB-TTF FETs von DH4T FETs (vgl. Abschnitt 8.2). Das bei DH4T beobachtete Sättigungsverhalten der Beweglichkeit nach den ersten Moleküllagen ist durch das zweidimensionale Schichtwachstum und die hohe Leitfähigkeitsanisotropie senkrecht zur Kanalebene begründet. Dies galt nicht für die unter-

suchten DB-TTF Schichten. Hier stieg die Beweglichkeit kontinuierlich mit der Schichtdicke. Einerseits erfolgt dies durch das Zusammenwachsen der schichtbildenden Materialinseln im Kanal, wodurch der effektive Kanal vergrößert und Korngrenzeinflüsse verringert werden. Andererseits deutet es auch auf einen starken Einfluss des Volumenmaterials hin. Dieser fundamentale Unterschied zu DH4T setzte sich auch bei den *in situ* Stressexperimenten der OFETs fort. Bei DB-TTF konnten nur eine verarmende Stressspannung $V_{GS} > V_{TH}$ und der Bruch des vorherrschenden Ultrahochvakuums die Schwellspannung V_{TH} beeinflussen.

PTAA: Die für PTAA FETs erzielten Beweglichkeitswerte in der Standardcharakterisierung lagen in der Größenordnung 10^{-3} cm^2/Vs, was sich im Bereich der berichteten Literaturwerte bewegt (vgl. Abschnitte 2.3.1 und 6.3). Diese, relativ zu den vorher berichteten Oligomerergebnissen, niedrige Beweglichkeit ist bedingt durch die geringere Ordnung der amorphen Polymerschichten des PTAA, was einen "Hopping"-Transportmechanismus zur Folge hat. Durch die erfolgreiche Integration der PTAA-Schichten in konventionellen UV-Lithographiestrukturierungsprozessen konnte im Rahmen der Arbeit die sehr hohe chemischen Widerstandsfähigkeit und Prozessierbarkeit des Materials nachgewiesen werden. Hierbei wurde zum einen PTAA auf Transistorelektroden durch eine lithographisch strukturierte Photolackschicht in Sauerstoffplasma verascht. Zum anderen wurde PTAA auf eine strukturierte Photolackschicht auf Transistorelektroden aufgebracht und mittels "lift-off" in Aceton strukturiert. Mit beiden Methoden wurden erfolgreich OFETs hergestellt und charakterisiert.

Ausblick

Abschließend fasst die folgende Tabelle die Ergebnisse der Standardcharakterisierung von OFETs der untersuchten Materialien zusammen.

material	L (μm)	W (μm)	C_i (nF/cm^2)	μ (cm^2/Vs)	V_{TH} (V)	I_{on}/I_{off}	S (V/decade)
DH4T	100	1400	33	0,13 (0,13)	1,75 (0,92)	2,4 (0,3) $\cdot 10^5$	0,50 (0,46)
DT-TTF (cryst)	30	10	33	3,65 (3,65)	1,16 (1,20)	5,1 (1,2)$\cdot 10^7$	-0,45 (-0,51)
DT-TTF (poly)	20	2000	33	0,066 (0,068)	-1,57 (-1,23)	2,0 (0,1) $\cdot 10^7$	0,22 (0,13)
DB-TTF (cryst)	2	100	33	0,41 (0,24)	1,09 (1,08)	0,8 (4,1)$\cdot 10^5$	-1,82 (-1,1)
DB-TTF (poly)	20	$2 \cdot 10^5$	66	0,039 (0,023)	4,75 (4,50)	1,4 (0,1) $\cdot 10^7$	0,30 (0,33)
PTAA	10	10^5	66	3,39 (4,77) 10^{-3}	1,85 (0,73)	74,3 (6,3) 10^4	-0,23 (-0,23)

Table 12.1: *Geometrie und Kenngrößen optimierter OFETs mit aktiven Schichten aus den untersuchten Materialsystemen. Die aufgeführten Kenngrößen in Klammern stammen aus dem linearen Bereich, die anderen aus dem Sättigungsbereich. Die Ergebnisse einkristallinen bzw. vakuumdeponiertem poly-kristallinen TTF-Materials sind mit (cryst) bzw. (poly) unterschieden. L ist die Kanallänge des OFETs, W die Kanalbreite, C_i die spezifische Kapazität des Dielektrikums, μ die ermittelte Beweglichkeit, V_{TH} die ermittelte Schwellspannung, I_{on}/I_{off} das Verhältnis des maximalen An-Stroms zum minimalen Aus-Strom und S der sogenannte "Subthreshold swing" (vgl. Abschnitt 5.1).*

Appendix A

Polycrystalline thin film growth by organic molecular beam deposition

This appendix is a brief description of the active layer deposition via organic molecular beam deposition (OMBD) used for the polycrystalline thin films of organic semiconductors.

Most of the organic semiconducting layers currently used in plastic electronics are in need of increased long-range crystalline order and/or purity. Thus, methods of physical vapour deposition attract increased interest. They are based on the thermal evaporation of the organic material in inert atmosphere or vacuum and in this way allow the formation if crystalline films of controllable order and purity, depending on the choice of organic material, the substrate, and the pre-deposition purification of system and materials. OMBD, as employed for the evaporated organic semiconductors in this work, applies an ultra high vacuum (UHV) below 10^{-8} mbar during deposition of the organic semiconductor films. For processes and especially substrate surfaces for which an epitaxial interface formation is not likely these films usually result in a polycrystalline structure. This may surely be the case if the substrate is amorphous (as in the case of SiO_2, covered or not with silanes) or most likely if the substrate is covered with an adsorbed contaminant layer, or if the mismatch strain of the interfacing crystalline structures is very large. The films' purity is essentially governed by the purity of the material that is to be evaporated and they are constituted of so-called grains with a uniform crystalline structure. The films are described in terms of their grain structure. This means the size of the grains, their shape (grain boundary morphology), and the crystallographic orientations in the film [141].

The OMBD is a low-energy deposition process compared to molecular beam epitaxy (MBE) of inorganic materials, because of the smaller evaporation temperatures needed in the organic materials. The setup is presented in fig. A.2 and has been specifically described in various diploma theses of the group (e.g. [108, 109, 111]). The important factors for controlling the structure of the growing film are the growth rate of the deposited material,

determined by the organic material in combination with the pressure, the temperature of the effusion cell (fig. A.2 (F)), but also adsorbing properties and temperature of the substrate. It is characterised e.g. by the time required to deposit a single monolayer. The second parameter is the material specific probability of encounters of different deposited molecules (ad-molecules) which diffuse randomly on the substrate surface. Additionally, the temperature difference between the melting temperature of the deposited material and the substrate temperature determines the structure of the polycrystalline film. All these factors control the degree for ad-molecules to seek out minimum energy positions and grain boundaries to be able to adopt minimum energy morphologies.

The different growth methods are classified in the following three classes, compare fig. A.1 from [141]:

- the *Vollmer–Weber* (VW) growth mode is when the ad-molecules proceed by the growth of islands until they coalesce. It is most likely for a large growth flux and moderate substrate temperature. Generally the molecules in VW–mode energetically tend to bond together, rather than to the surface. It results in an island growth mode.
- the *Franck–van der Merwe* (FM) growth mode is the opposite of VW, when ad-molecules form stable clusters and new arriving ones tend to attach to the cluster at its periphery, in order to bond with both the substrate and the cluster molecules. This is a layer-by-layer growth mode.
- the *Stranski–Krastanov* (SK) growth mode combines the features of VW and FM. The material starts in a planar growth and then the mode is reversed after a few monolayers. The subsequent ad-molecules tend more to grow in clusters than to continue the layer by layer growth. The behaviour is material and substrate specific and also (layer) thickness dependent.

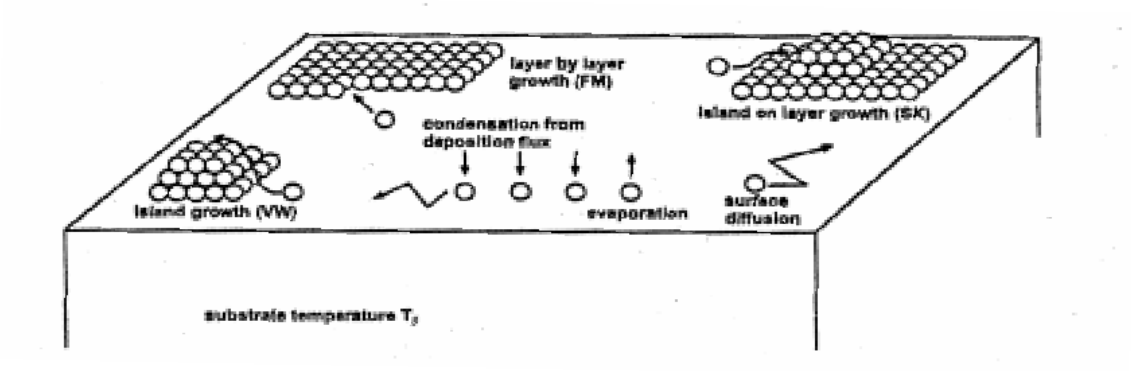


Figure A.1: *Schematic showing the principle modes and influencing factors of film formation on substrates (from [141]). Island growth (VW) is displayed in the bottom left corner, layer-by-layer growth (FM) top left corner, and island on layer growth (SK) in the top right corner.*

In the experimental part DH4T, DB-, and DT-TTF are investigated using OMBD. Here, the oligothiophene DH4T proves a *Franck–van der Merwe* growth and allows the analysis of ultra-thin layers covering the whole substrate at a considerable high crystalline long-range order (cf. chapters 2 and 6). The TTF derivatives both exhibit *Vollmer–Weber* growth. The growth analysis and optimisation of layers with respect to the performance in OFETs for the DB-TTF is presented in detail in appendix D.

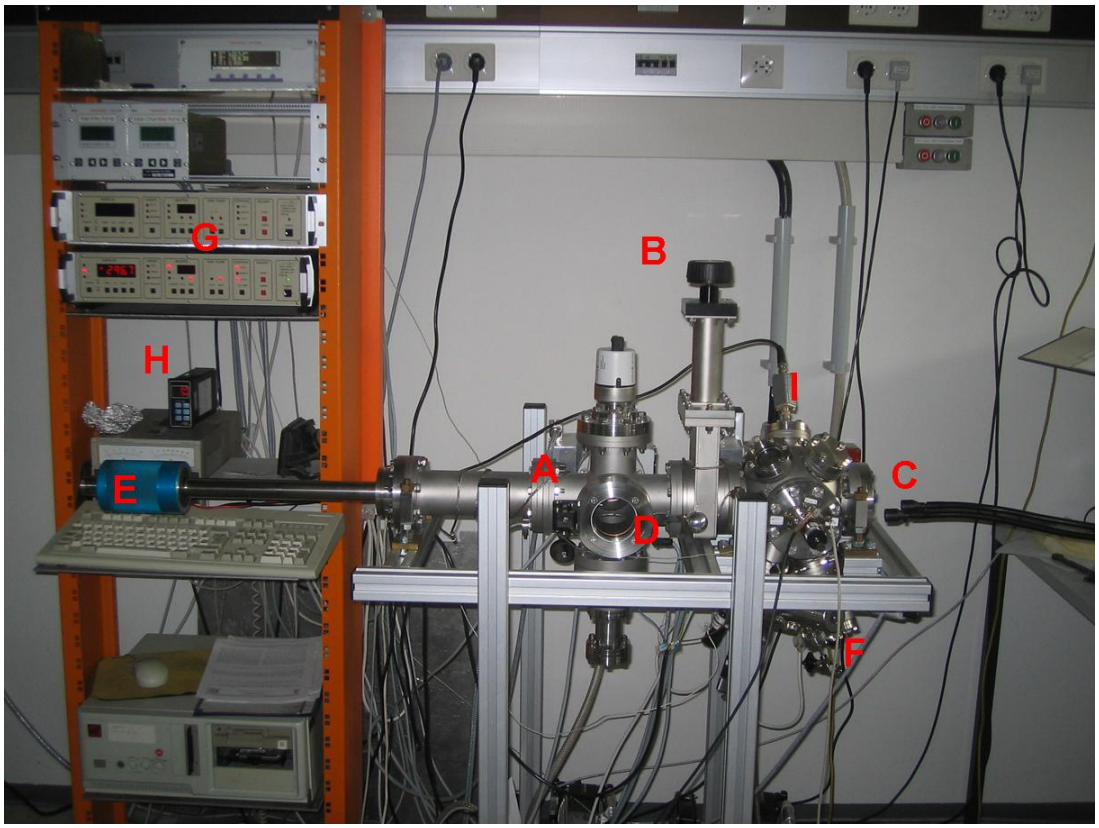


Figure A.2: *Image of the organic molecular beam deposition system. The chamber consist of a load-lock chamber (A) and the main chamber (C) with a maximum of four effusion cells (F) for the evaporation of the organic materials. Each chamber is pumped by a turbomolecular pump (backside, not visible). The load-lock (D) allows a fast entry of samples that can be transferred via the manipulator (E) on the sample holder in the main chamber (C). Here, the valve (B) between the chambers prevents the main chamber from being vented while loading a sample. The deposition is controlled by the temperature control of the effusion cells (H) and the substrate (G). The microbalance (I) measures the mass of the deposited material and has to be calibrated for each material with respect to the resulting layer thickness.*

Appendix B

Soft lithography

Lithography takes an essential part in this work. It is the main tool for device fabrication. In fact each electrode structure and partly the organic semiconductor were structured using a lithography method. The appendix will describe the aspects of lithography, including a short general description and lithography solutions to specific requirements in context with the experimental results presented in chapters 6 - 10. The section on standard lithography will describe the principle and treat the advantages and disadvantages of UV-optical and electron beam lithography (UVL and EBL, respectively). It will also discuss approaches to resist layer concepts and the resulting profiles after development. Then the performed alternative lithography methods with sub-micrometer resolution will be discussed and finally the lithography on organic semiconductors (in this case the PTAA) will be treated.

B.1 Standard lithography

By standard lithography conventional UVL and EBL are meant. Both methods are well established in research and offer a huge amount of possibilities in structuring surfaces. The material systems, device specifications, economics, etc. provide the conditions for the choice of method and/or chemistry. A survey of lithography for semiconductor applications is given by Moreau [142]. In this thesis, beside the usual application of structuring source and drain electrodes of thin-film transistor, lithography on the organic semiconductor is presented as an innovative application.
EBL has an increased resolution compared to UVL. It is therefore applied in the fabrication of sub-micrometer channel electrodes with results achieving channel lengths below 100 nm at a remarkably large total channel width of more than 100 μm. The UVL was optimised to deliver transistor structures in a metallisation and lift-off process with a channel length L down to 500 nm and a channel width of 2 mm. The image of a structure is presented in fig. B.5 (a). The optimisation process is described in [143]. The principle applied for the

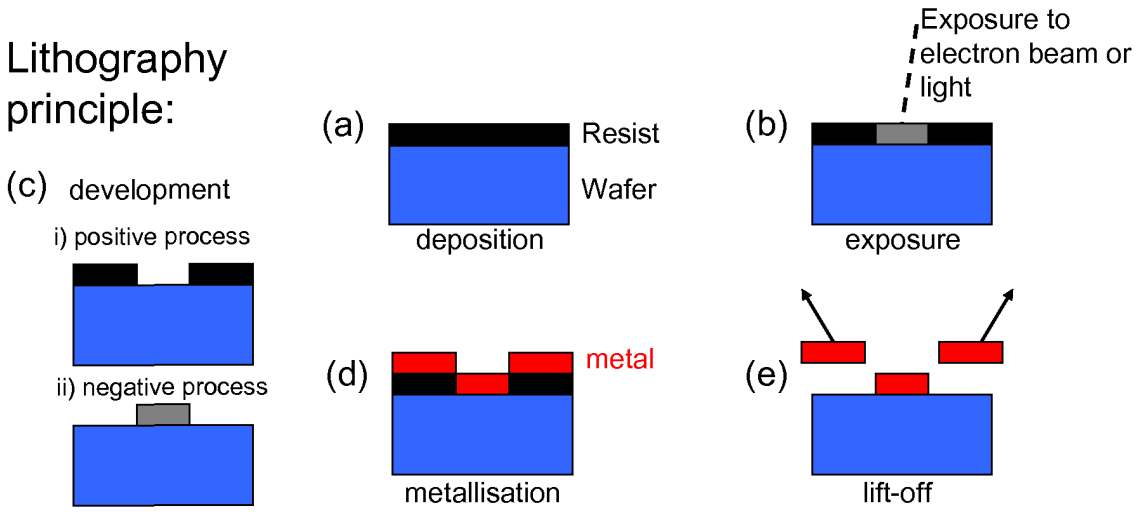


Figure B.1: *Lithography principle in a five step lift-off process ((a) resist deposition, (b) exposure, (c) development, (d) metallisation, (e) lift-off).*

electrode structuring is displayed in fig. B.1.

- (a) The resist layer is a photo- or electron-sensitive layer of an organic compound. It is spin-coated onto the surface.
- (b) The resist is exposed to light illumination (UVL) or an electron beam in a SEM system (EBL). The exposure changes the resist's properties in the illuminated area. Here lies the advantage of UVL, where the illumination is a parallel process through an optical mask, whereas EBL is a slow serial scanning process.
- (c) The resist either becomes soluble in the illuminated areas under application of a specific developer (this is called a positive process) or insoluble (negative process). The developer removes the resist.
- (d) The opened windows to the surface of the resist offer various structuring methods (e.g. controlled etching). In a metallisation process, in which various techniques can be used, a thin metal layer is deposited.
- (e) The final lift-off step transfers the pattern (only positive process displayed) a solvent for the removal of the residual resist with the metal on top being used.

The above listing disguises the challenges to the lithography processes, which are the adjustment of the properties in the material systems: the surface, the resist, the developer, and the metal layer by different parameters: the materials themselves, the deposition and baking methods, exposure and development time factors, stability and ageing aspects, etc.. In the following specific aspects for OFET electrode fabrication are discussed.

B.1.1 Resist profiles

The resist profile is generated by the appropriate dose (amount of electrons/photons per area) during exposure and the developer combination. Especially in the lift-off process the profile in the resist is essential for the image transfer. This is apparent in a more precise consideration of the metallisation and lift-off step (fig. B.1 (d) and (e)). In principle the resist profile before metallisation will result in one of the two outer types (a) and (c) displayed in fig. B.2. The desired profile in the present process is the undercut profile (a) where the shape is dominated by the dose and in the case of EBL by the reflected electrons. Here, ideally (depending on the proportion of resist layer thickness to deposited metal layer thickness) there will be no connection between the metal deposited on the resist and in the opened windows. The lift-off is granted and the edges of the pattern will be smooth and even descending due to diffusion processes in the half shadow of the undercut. In the case of a continuous metal layer the undercut will form small channels for the lift-off solution to wash in and permit the separation of the desired structure. High resolution structures using lift-off technique will only be possible if this kind of profile is used. If the flanks of the profile are open for the deposited metal like in the overcut profile (c) the separation at the structures' edges is more difficult. Here, the shape is dominated by the developer. Then, in metallisation and lift-off the ratio of resist layer thickness to deposited metal layer thickness is the critical parameter, because the metal film has to be thin enough to tear off and the lift-off solution must have the possibility to wash away the resist. Furthermore the process can be accompanied by side effects like standing walls at the edges which may influence the device performance. Additionally the deposition method of the metal layer influences the coverage of the profile flanks. Even though the evaporation source is located at a perpendicular angle to the surface, this is not sufficient to warrant a perpendicular coverage by the metal e.g. for magnetron sputtering deposition where increased scattering processes influence the direction of the metal atom flux. A larger distance between substrate and source reduces these effects, however this is a condition of the evaporation system. The vertical profile (b) is the compromise between the two others.

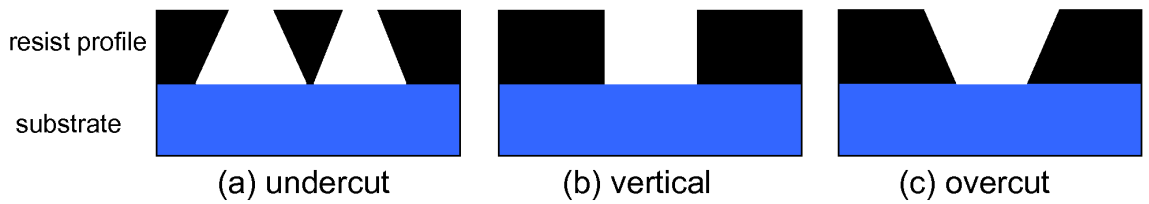


Figure B.2: *Schematic of the possible resist profile types after the development step: (a) the undercut profile, (b) the vertical profile, and (c) the overcut profile.*

B.1.2 Results and different resist systems

B.1.2.1 Electron beam lithography

The EBL is done using a LEO (now Carl Zeiss) SEM with a cold field-emission cathode (W/ZrO_2) using a RAITH stage control system. The cold field-emission guarantees a higher long term stability of the emission current. As a resist polymethyl methacrylate (PMMA) of various molecular weight dissolved in ethyllactate in positive lithography processes was used for all transistors in this thesis. In the presence of electrons, the PMMA changes (for the chemistry cf. [142]) and becomes soluble in isopropanole (IPA), the developer.

The resolution of processes hereby is not controlled by the electron energy or even by the electron beam width but rather by the resist and the path of the electrons in the resist. Three classes of effects occur:

- the *proximity effect* is a backscattering process where electrons from an adjacent feature influence the neighbouring exposed feature by backscattering from the substrate
- *forward scattering of electrons* where arriving electrons scatter in the resist. This effect can be controlled by the electrons' energy and is used for generating the desired profile. A higher energy decreases the number of forward scattered electrons but also the number of electrons affecting the resist, which increases the necessary dose of charge per area.
- and *secondary electron effects* where affecting electrons produce secondary electrons in the resist.

A comfortable way to control the resist profile which results after development is using layered systems of the resist in correlation with electron dose and developing time. The resist systems in the schematic of fig. B.3 show the principle of the approaches employed for EBL in the context of metallisation and lift-off processes with deep sub-micrometer resolution.

A thin (of thickness below 50 nm) one layer resist (a) has the least requirement concerning sample preparation. Another advantage is that the process is accompanied by low energy exposure (< 5 keV), which reduces the exposure time due to more electrons taking effect in the resist. Moreover, the needed undercut profile is achieved due to the low energy exposure: it creates an increased forward scattering in the resist additionally to backscattering effects from the SiO_2 surface. The profile will have drop shape that can be controlled by the dose and development time to reach the shape in the bottom image of (a). The lower energy generally increases the side effect which limits the resolution of the whole process. In the present work transistor structures like in fig. B.4 using a one layer resist could be

fabricated down to a channel length L of 100 nm. The main limiting factor is the extend of the undercut which will result in "underdigging" the remaining resist if it exceeds L/2. The higher the electrons' energy is the more the profile will have a vertical shape like in fig. B.2 (b). However, then the lift-off is limiting the resolution in the thin one layer system and a change in the resist system to multi-layered resist is expedient.

The vertical profile has its advantages in the three-layer resist (c) in fig. B.3. The resolution of this process is only defined by the first layer. It is extremely thin (< 50 nm) and exposed to high energy electrons (30 keV) which results in a vertical profile after development. Then the thin metal layer (e.g. 10 nm Ti) is etched in a chemically assisted ion beam etching (CAIBE) process using the PMMA as a mask. The top layer is then removed in oxygen plasma etching which also etches a certain volume of the bottom PMMA layer through the opening in the metal layer. This guarantees an undercut profile of high resolution. The preparation and processing steps are very elaborate and sensitive to all kinds of influence. Therefore, the method is not used in the electrode fabrication.

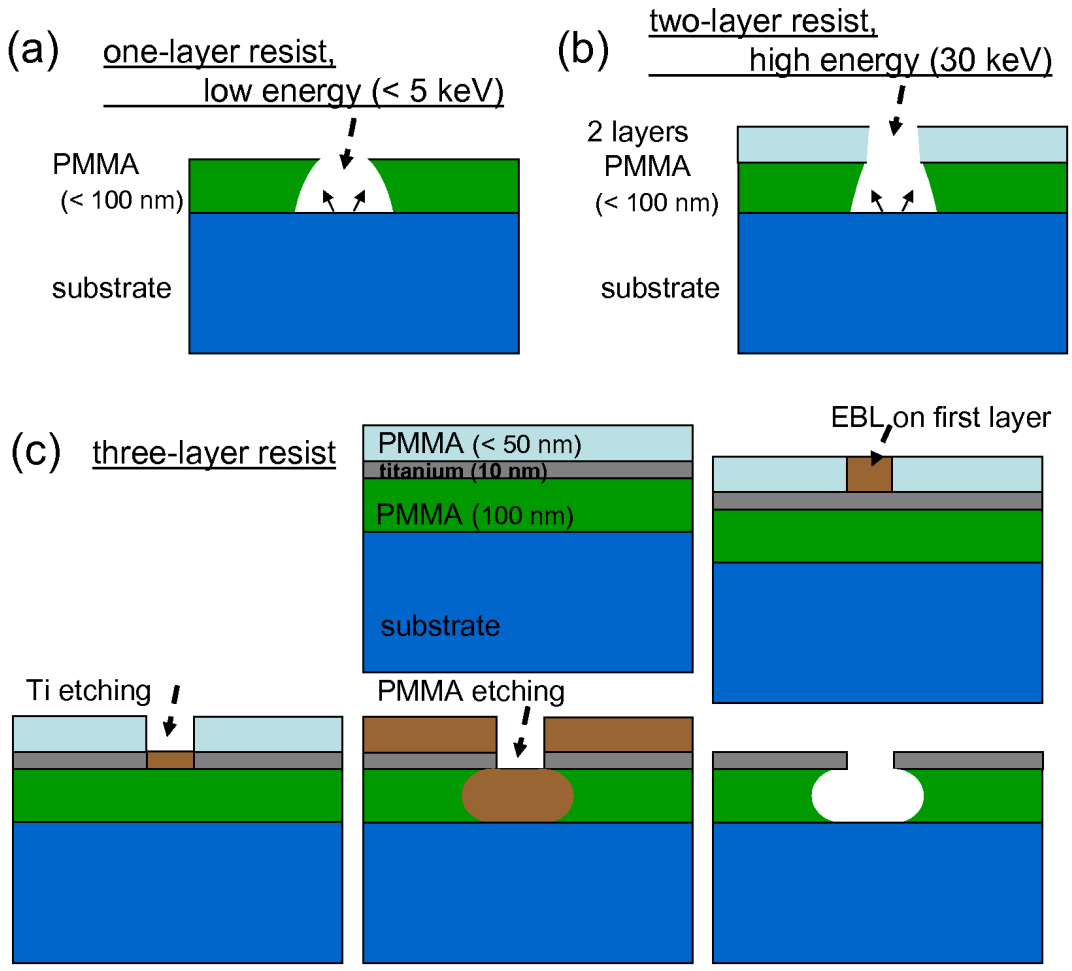


Figure B.3: *Resist systems for EBL: (a) one layer resist system and low energy (< 5 keV) exposure, (b) two-layer resist system and high energy (30 keV) exposure, (c) three-layer resist system.*

The best compromise between preparation effort and resolution is the two layer resist. It consists of a thin top layer of PMMA and a thicker bottom layer of PMMA (of a total thickness of below 100 nm). The bottom layer PMMA is of a higher molecular weight. Therefore in a 30 keV exposure scattering in the bottom layer is larger in comparison with the top layer. This is the origin of the undercut profile in the two-layer resist system.

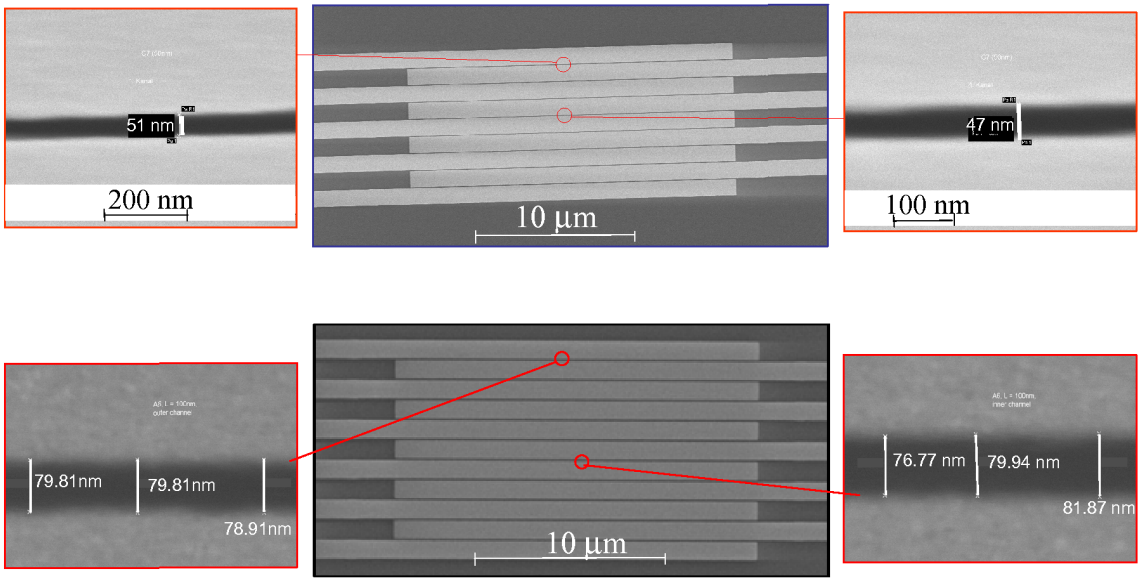


Figure B.4: *SEM images of source/drain electrode structures of homogeneous sub 100 nm channel length with a total channel width of 160 µm and 200 µm in the top and bottom electrode structure, respectively. Top: resulting from a two-layer resist EBL process with electron beam evaporated metal (Ti/Au (1 nm/ 19 nm)) and lift-off in aceton. Bottom: the same process but metallised with 10 nm Pt by magnetron sputtering.*

The challenge in the fabrication of sub-micrometer electrodes lies in the combination of smallest channels (= standing walls in the resist profile) and homogeneity over a large channel width which is constituted by large features close to one another. This means a control of the above denoted scattering effects with respect to the lift-off step. The undercut profile in the two layer resist system has proved high yield in structures with a channel length down to 50 nm depending on the deposited metal layer. Titanium has proved to be of disadvantage regarding the contact resistance to p-type organic semiconductors (cf. section 5.2 and [140]). However, it is necessary to warrant the contact between noble metal like gold or platinum to SiO_2. In order to avoid the titanium layer a magnetron sputtering deposition of e.g. platinum can be used. It enables sufficient adhesion and thus creates pure noble metal contacts. The two structures of fig. B.4 were achieved using the same two-layer resist but different metallisation methods in a lift-off process. The top structure utilises electron beam evaporated gold contacts (19 nm) with a 1 nm thick titanium adhesion layer (*in situ* metallised), the bottom contacts are metallised via

magnetron sputtering deposition with a layer of 10 nm platinum. Both results show a high homogeneity of the channel length. The value of L is constant in both electrode structures for the inner and outer channels which means a very good control of the proximity effects in the presented cases. The electron beam evaporated metals show the higher resolution with a channel length of L = 50 nm compared to the 80 nm achieved with 10 nm magnetron sputtered platinum. The above mentioned disadvantage of a sputtering deposition due to a less perpendicularly directed metal atom flux can explain the resulting larger minimum channel length. A further optimisation of the resist composition in the two-layer resist system using a thinner two-layer resist and electron beam evaporated 1 nm/9 nm Ti/Pt contacts even results in a channel length below 30 nm [139].

B.1.2.2 Optical resist

In the optical resist the profile is controlled by the developer. Thus, the shape is of overcut profile (fig. B.2 (c)). In fig. B.5 (b) the AFM image of a Ti/Au contact on SiO_2 with a layer of the organic semiconductor pentacene shows a standing contact edge that most probably stems from the lift-off in an UVL process. In fact the stability of the *in situ* samples presented in chapter 8 was enhanced by using an EBL process even for OFET with a channel length in the large micrometer scale.

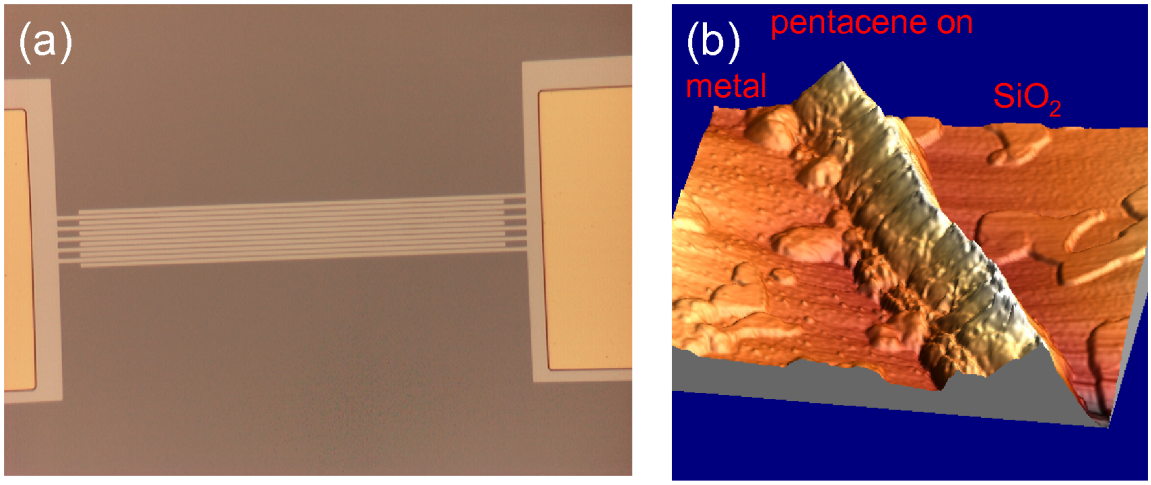


Figure B.5: *(a) Transistor electrode structure fabricated by UVL in a metallisation (Ti/Au, 1 nm/ 19 nm) and lift-off process bearing a channel length L of 500 nm and with W of 2 mm. (b) AFM image of metal contact on SiO_2 covered with pentacene. The edge of the contact is standing up.*

Here, the undercut technique, which is commonly used in EBL, was also implemented to UVL by the adaption of a two-layer resist system to an UVL process. The result is shown

in the SEM image of a cross section in the resulting profile after metallisation (fig. B.6 (left)). The system consists of two layers of the same resist. After the baking out of the first layer, it is completely exposed (flash exposed) to UV light for 2 s. This is about 30 % of the total time necessary for the complete exposure of the single resist layer. Then the second layer is spin-coated and baked out at a lower temperature, to prevent from outgassing in the first layer. After the exposure of the desired structure the first layer develops faster due to the advance in exposure and hence the undercut profile is achieved. The right images show the electrode finger's edges after the lift-off. They prove the working lift-off with resulting smooth contact edges. Here, the difficulty lies in the inhomogeneity caused by the intermixing of the two layers during the deposition of layer two. This is mainly due to the high solubility of the applied *Novolac* resist in the context with the low baking temperatures.

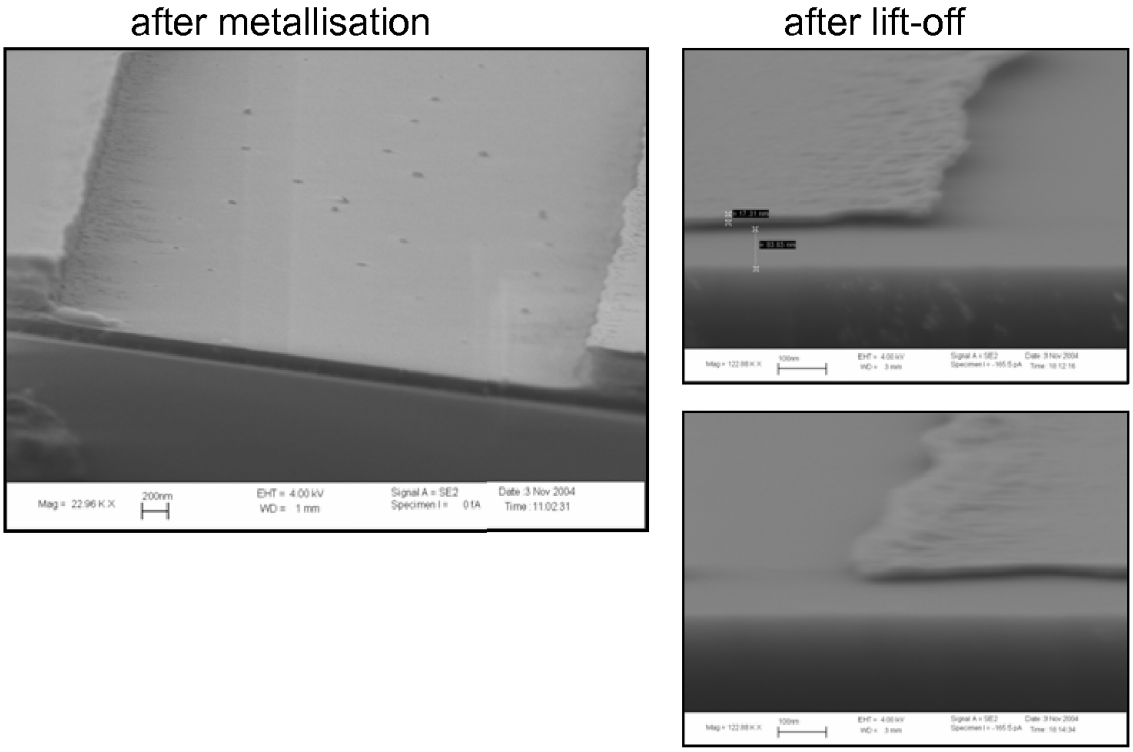


Figure B.6: *SEM images of a two layer optical resist profile after exposure, development and metallisation with 10 nm titanium of one electrode finger (cross section through the structure)(left) and after lift-off (2 images on the right).*

B.2 Alternative methods for sub-micrometer lithography

The conventional EBL presented above for the creation of electrode structures with sub-micrometer resolution is a serial process. It is complex concerning the requirements on

technology, time and use of chemistry in resist deposition, development and depending on the process, e.g. lift-off steps. In this appendix we describe two possible alternative methods applied to fabricate transistor electrodes with 100 nm channel length.

B.2.1 An optimised microcontact printing process for sub-micrometer OFETs

The section follows the publications [6, 144], and [145]. It establishes a soft lithography process used to fabricate structures of resolution below 100 nm. Printing techniques are attractive for the fabrication of OFETs [11, 86] both because of economic reasons and because of the inherent appeal of an all-organic fabrication process for organic semiconductors. Many organic materials are not compatible with conventional lithography. In this context microcontact printing (μCP) is a parallel printing technique capable of structuring large areas with high-resolution chemical patterns [144, 146]. It is an interesting possibility for low-budget printing processing. In contrast with nanoimprint lithography (NIL) [104] it offers the additional advantage of being forgiving as to substrate quality, and can be readily applied to e.g. flexible [147] or structured [144] substrates.
Here, μCP is employed for the fabrication of interdigitated electrode structures for application in OFETs. A rigid carrier μCP technique is used. It is originally developed in reference [144]. It enables high quality mix-and-match performance and avoids macroscopic distortions that limit downscaling in thicker elastomeric stamps. Electrical characteristics prove that the process yields OFETs with similar or better electrical performance than devices fabricated using conventional lithography.

There are several steps involved in μCP fabrication of electrode structures. The process is based on a general μCP concept [148]: a rubber stamp prints a molecular ink onto a gold covered substrate. The stamp pattern is transferred by wet etching of the gold, where the ink serves as a mask [149]. The concrete fabrication of the stamp follows the process described in reference [144]. A master, defined by electron beam lithography (PMMA on silicon, thickness of 300 nm to 500 nm) is used as a mold for a prepolymer of polydimethylsiloxane (PDMS) rubber on flat rigid silicon. An appropriate pretreatment of the master and substrate with dodecyltrichlorosilane and vinyloctodecyltrichlorosilane, respectively, ensures the release of the stamp after hardening of the PDMS and enhances its adhesion to the Si carrier. Curing of the polymer was done at room temperature to prevent thermal shrinkage of the edges of the stamps. The pressure during curing (5 h) was $\sim$8 bar, resulting in thin stamps with approx. 2 μm PDMS thickness and a relief depth of 300 nm to 500 nm. This is defined by the master. The printing on Au/Ti covered SiO_2 substrates was carried out under external load in a pneumatic press, with pressures between 2 and 6 bar. The value is calculated using an approximate pattern area and the mass of the load. As ink, alkanethiols have shown the best results [146, 150]. They form a self-assembled monolayer (SAM) on the gold surface which offers stable effective protection of the metal, while unprotected Au is etched in a ferricyanide etchant solution [151]. In the present case eicosanethiol (ECT) [$CH_3(CH_2)_{19}SH$] diluted in ethanol is used, which

combines limited diffusion in the PDMS during printing and good protection of Au during the etching steps [146, 152]. The ink is loaded by dropping 3 ml of solution onto the stamp; after waiting 30 s the stamp is blown dry in a stream of nitrogen. The parameters printing time (t_{print}), printing pressure (p_{print}), and the concentration of ECT in ethanol were systematically varied and optimised. In order to produce electrode structures with small channel length L_{eff} , the critical resolution is not necessarily that of the stamp, but instead the size of the uncovered part of the substrate, which forms the conducting channel after removing the gold. This implies that the broadening of the 'inked' areas can be beneficial, provided it is well controlled, e.g., by the applied pressure. Experimentally it turned out that a certain minimum p_{print} was always needed to obtain uniform contact between the stamp and template. p_{print} below 2 bar resulted in a partially incomplete contact. Upon an increase of p_{print}, the SAM covered area broadened due to mechanical stretching of the elastomeric stamp. This is shown schematically on the right side of fig. B.7. Above certain p_{print} the patterns are no longer transferred correctly, resulting first in merging of the structures (intermediate region, 6–8 bar, in fig. B.7, bottom diagram) and finally in collapse (>8 bar), where the SAM covers almost the whole area.

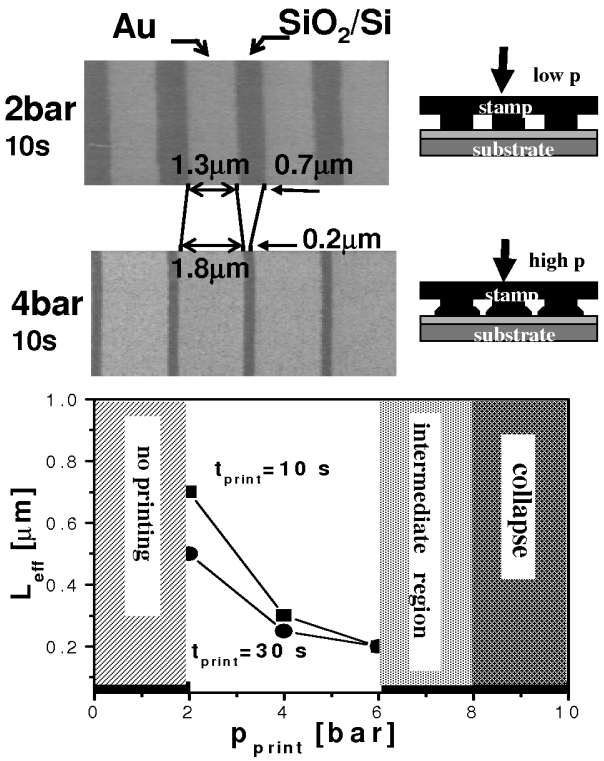


Figure B.7:

Top: SEM images showing the narrowing of L_{eff} due to an increase of p_{print} . This results from the broadening of the stamp structures by applying higher pressures (schematic on the right).

Bottom: Diagram showing the dependence of L_{eff} on p_{print} for two different t_{print} , 10 and 30 s. For p_{print} lower than 2 bar there is no full contact of the stamp so the printing results are bad. p_{print} too high results in partial destruction of the patterns due to merging and sagging effects (6–8 bar). p_{print} even higher results in a collapse and no patterning is achieved.

This principle is used to control L_{eff} of the resulting electrode structures. Fig. B.7 (top) shows SEM images of two Au/Ti patterns on SiO_2 fabricated by the same PDMS stamp, where p_{print} was changed from 2 to 4 bar, while all other parameters were kept constant. In this way a 200 nm channel could be produced using a stamp with an initial master-defined channel length L_i of 700 nm. The diagram at the bottom of fig. B.7 indicates that an in-

crease in time, during the pressure is applied to the stamp, also results in shorter L_{eff}. This was investigated in greater detail in experiments that varied t_{print} at constant p_{print} of 3.8 bar and an ECT concentration in ethanol of 2 mM, shown in fig. B.8 in the top diagram. L_{eff} decreases continually with t_{print} . Thus, L_i can be reduced until sagging effects and merging of close features cause the collapse of the printing results. Varying the concentration of ECT in ethanol has, within the concentration range investigated, only a weak effect on L_{eff} (fig. B.8, bottom), decreasing it from about 12% to 44% for the highest concentration (2 mM) compared to the results of a low concentration of 0.2 mM. During fabrication t_{print} and p_{print} were kept constant at 2 s and 3.8 bar, respectively. In this way OFETs

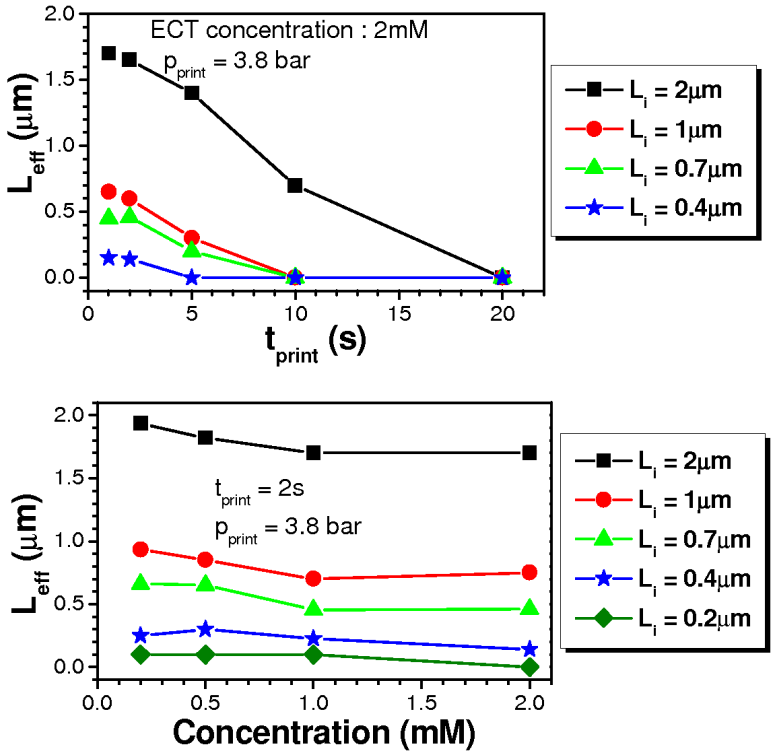


Figure B.8: *Top: Channel length L_{eff} depending on t_{print} at constant p_{print} of 3.8 bar and eicosanethiol concentration of 2 mM for different L_i of the stamp. Bottom: Channel length L_{eff} depending on the eicosanethiol concentration in ethanol at constant t_{print} of 2 s and p_{print} of 3.8 bar for different L_i of the stamp.*

were made from interdigitated gold on titanium electrode structures, fabricated using μCP on a thermally oxidised (100 nm oxide thickness), highly n-doped silicon wafer shown in fig. B.9. The printed area was about 5×5 mm^2 and contained numerous devices with master-defined L_i ranging from 2 μm down to 200 nm and total widths ranging from 160 to 360 μm (9–19 interdigitated fingers with an overlap of 20 μm). By varying the printing parameters in the manner described above, structures with L_{eff} down to 100 nm could be fabricated (fig. B.9). The bottom contact OFET was completed by an HMDS pretreatment (appendix C) and afterwards depositing a thin layer $\sim$ 10 nm of DH4T via vacuum evaporation organic molecular beam deposition (T_{sub} = 90 °C, rate of 2.3 Å/min) (see appendix A). The corresponding output characteristics of a 100 nm and a 1.8 μm channel sized structure, with total widths of 160 and 360 μm, respectively, are presented in fig. B.10. The large channel shows excellent characteristics and behaves according to standard theory (cf. Chapter 4). The 100 nm channel exhibits marked short channel effects (cf. section 5.3): bad off current and nonsquare behaviour for higher channel voltages. Both devices exhibit high levels of current for relatively modest channel and gate biases. From the transfer char-

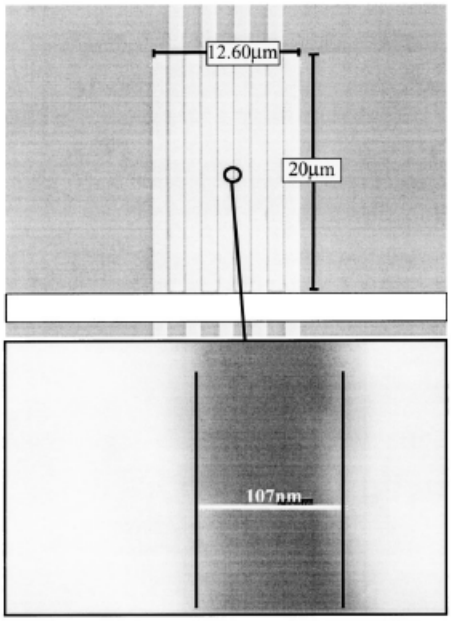


Figure B.9: *SEM image of a transistor structure with L_{eff} down to 100 nm and width of 160 μm fabricated using μCP.*

acteristics of the $L_{eff} = 1.8$ μm device, the analysis yields a mobility value of 1.0×10^{-2} and 1.1×10^{-2} cm^2/Vs for the linear (V_{DS} = -2 V) and saturation region (V_{DS} = -20 V), respectively. The values for the mobility are an order of magnitude higher than those reported for the NIL fabricated structures of Ref. [104], which were made from polymeric P3HT. The demonstration of the working 100 nm structure whose short channel behaviour should be manageable by reducing the oxide thickness is encouraging. The results prove the high potential of the μCP technique for fabricating downscaled OTFTs for low-budget highthroughput fabrication in a mix-and-match process.

B.2.2 Sub-micrometer channel length by angle evaporation of metals

The principle of a shadow evaporation is a common method to create gaps of certain size. The metal is deposited onto the sample under a certain angle. Structures on the surface of the samples are used to create a fine structure by their shadow relative to the evaporation source. In the presented case the process follows the schematic in fig. B.11. Common electrode structures of micrometer channel length are fabricated using standard optical lithography metallisation and lift-off (a). The next step (b) is necessary to prevent the electrodes from short-cutting. In a second optical lithography step a shadow mask of structured resist is created by opening windows over the electrode finger's overlap. Now the last step (c) is the angle evaporation of metal. The angle α and the electrodes' height h resulting in step (a) define the size of the uncovered area and the reduced distance between source and drain contacts. Using trigonometry it follows

$$L_{reduced} = h/tan(\alpha).$$

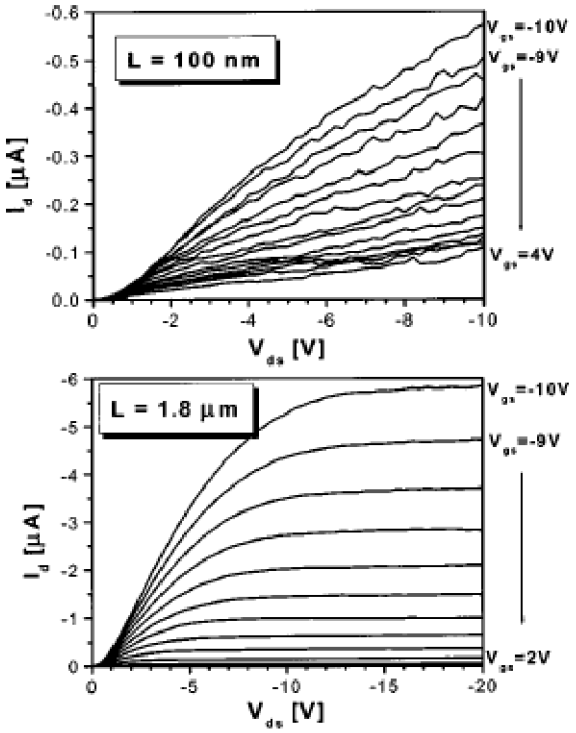


Figure B.10: *Output characteristics $I_D(V_{DS})$ of DH4T thin-film transistors with an electrode structure made by microcontact printing. Top: Characteristics of an OFET with L_{eff} down to 100 nm and width of 160 μm. Gate bias V_{GS} was varied from 4 to -10 V. Bottom: Similar results for L_{eff} = 1.8 μm and W = 360 μm, but V_{GS} was varied from 2 to -10 V.*

In fig. B.12 the results of the process are presented. The pre-structured h is 25 nm and the installed α is 75°–80°. From the above equation follows a $L_{reduced}$ of 100–150 μm. The measured distance between the origin electrode and the added metal is in the range 80 - 100 nm. The wave profile of the edge results from the natural roughness of the lithography step. A more precise profile of the shadow creating structure however would introduce more complex technologies. The effective channel may be further reduced by diffusion processes into the shadowed regime which explains the difference between the calculated and the measured values. The process is probably not of less effort than using EBL. However, it applies easy accessible methods and in this way will deliver a possibility to create nanostructured top contacts, if an optical lithography process on top of the organic semiconductor is available. The following section describes such a lithography method for PTAA (for the transport results cf. Chapter 10).

B.3 Lithography on organic semiconductors

This section describes two lithography processes with the organic semiconductor PTAA. They are developed for the use in OFET fabrication with PTAA as the active layer. The corresponding transport properties and stability results are presented in chapter 10.

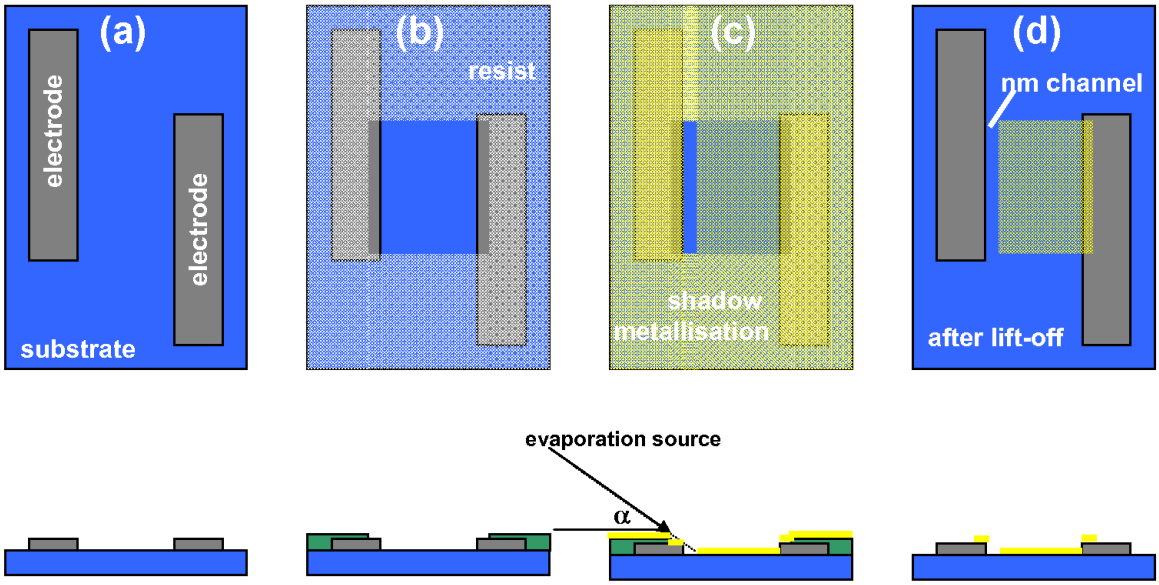


Figure B.11: *Schematic of an angle evaporation process for creation of a reduced channel length.*

B.3.1 Structuring PTAA via oxygen plasma etching

The process allows the structuring of a deposited layer of PTAA using a lithographically defined mask (the developed resist) and an etching process with oxygen plasma. The aim was to leave the PTAA only in the area of the device channel which is the overlap of the finger electrodes on SiO_2 covered wafers (standard bottom contact setup, cf. fig. 4.1). Therefore,due to the given requirements - a small area to be covered compared to the whole sample - a negative lithography process was developed. This is achieved by the method of reversal bake. The substrate before the lithography process is therefore a OFET sample of a SiO_2 covered wafer with a layer of PTAA (by standard pretreatment procedure and deposition as described in section 6.3). The following list describes the steps of the processing:

- the optical resist (*Novolac*) is deposited and baked out as in standard lithography (thickness of the resist is $\sim$ 600 nm $>$ thickness of PTAA layer $\sim$ 100 nm
- the overlap of the finger electrodes is exposed by alignment of a special mask
- a reversal bake (5 min at elevated temperature compared to the bake out temperature before) leaves the beforehand exposed areas insoluble in the developer
- by the exposure of the whole area the positive process is inverted into a negative process
- the development in standard developer leaves resist only on the first exposed areas

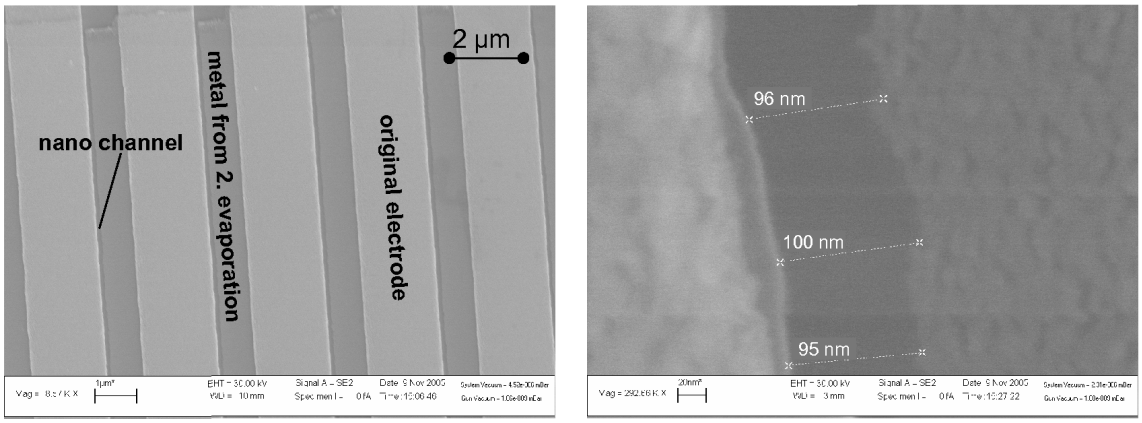


Figure B.12: *SEM images of a fabricated 100 nm channel using angle evaporation processing described in fig. B.11.*

- in an oxygen plasma etching process the thick resist layer protects the PTAA between the electrodes
- the remaining resist is lifted-off in acetone

The last step is not necessary for transport because the resist layer is isolating, however it proves the resistivity of the PTAA against acetone and offers a huge variety of possibilities of using the material. The images of fig. B.13 show the final result after the process of a single transistor.

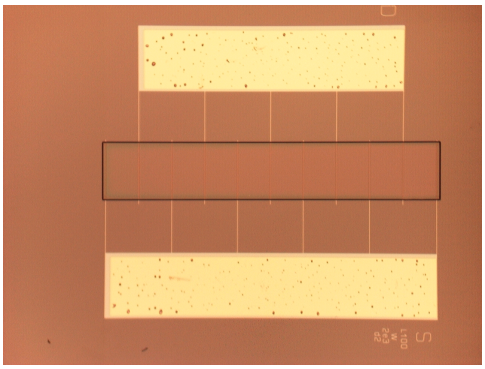


Figure B.13: *Micrograph of an OFET with a structured active layer of PTAA. The PTAA is structured by a standard lithography process and oxygen plasma etching.*

B.3.2 Structuring PTAA via lithography and lift-off

The aim of this process is the same as in the previous subsection: leaving a structured PTAA film isolated from other structures solely on the transistor electrodes. This is achieved by a process comparable to the fabrication of electrodes described in the beginning of this appendix. Based on SiO_2 covered wafers with electrode structures a mask of resist with

lithographically defined windows over the electrodes is fabricated. The PTAA is spin-coated using the standard method and the lift-off of the resist with the PTAA on top is performed in acetone, where the adhesion of the PTAA film on the SiO_2 is sufficient to let it tear off. The resist layer is not forgiving to the standard pretreatment process, therefore any treatment is omitted and a reduced performance in transport is expected (cf. 10). However, in comparison with the previous structuring method the effort is considerably lower. The resulting structures are presented in fig. B.14.

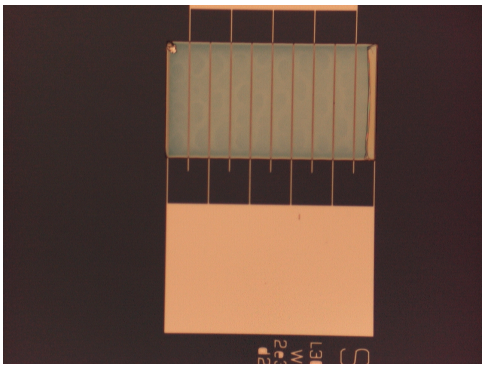


Figure B.14: *Micrograph of an OFET with a structured active layer of PTAA. The PTAA is structured using UVL and lift-off process in acetone.*

Appendix C

Pretreatment of the SiO_2 gate insulator

This appendix describes different pretreatment steps applied to the SiO_2 dielectric in order to increase the performance of the OFETs. Thus, the substrate pretreatment aims at the optimisation of the interface with the organic semiconductor. On the one hand, it is to prevent interfacial states. On the other hand, the surface manipulation is supposed to lead to an optimised growth during the different deposition methods (appendix A). In several previous sections, the relevance of the ordering in the organic semiconductor for its carrier mobility was pointed out. As the high mobility in the OFET device is always marking a high performance the aim in the pretreatment steps lies in a resulting higher order and additionally in a cleaning of the interface. Moreover, the SiO_2 attracts water and tends to generate a hydroxyl terminated top layer. The result is a hydrophilic surface which is characterised by a low contact angle (between 20° and 80°). For the definition of the contact angle see fig. C.4. This causes an inhomogeneous growth of the materials, grown by organic molecular beam deposition or by solution processing from a polar solvent (as practised in the presented results). Additionally, the untreated surface provokes an increased number of surface states which act as charge carrier traps and reduce the device performance. Here the concept of self-assembled monolayer (SAM) formation that changes the surface properties, on the one hand, delivers the desired surface properties, i.e. a homogeneous hydrophobic surface, and on the other hand, prevents an increased number of surface states. In the case of SiO_2, silane molecules are suitable for a monolayer chemisorption (formation of a chemical bond between molecule and surface). The next section describes the procedure for the formation of a SAM of hexamethyldisilazane (HMDS) and octadecyltrichlorosilane (OTS) on SiO_2 (cf. fig. C.1 for the chemical structures).

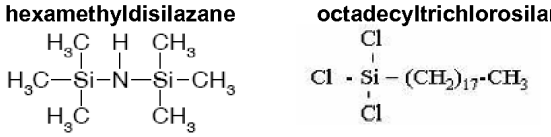


Figure C.1: *Chemical structure of HMDS (top) and OTS (bottom).*

C.1 Silane self–assembled monolayers on SiO_2

The formation of a SAM of one of the two molecular species in fig. C.1 follows chemical reactions described in literature [153]. The final step for the chemisorption obeys the reactions in fig. C.2. A chemical bond with the hydroxyl terminated SiO_2 surface is formed. The reaction takes place on the whole surface and leaves the molecules standing homogeneously distributed on and perpendicular to the surface, which is illustrated in fig. C.3. The surface is now terminated with the hydrophobic ending of the SAM. The reaction

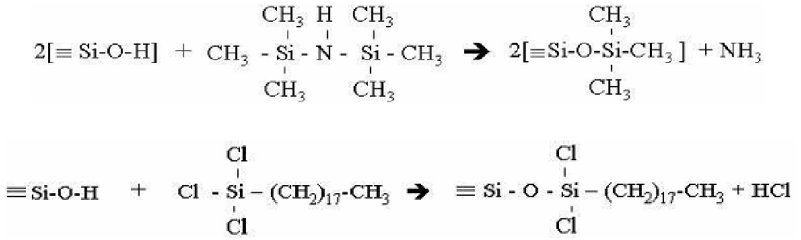


Figure C.2: *Chemical reaction of HMDS (top) and OTS (bottom) with the hydroxyl terminated SiO_2 surface.*

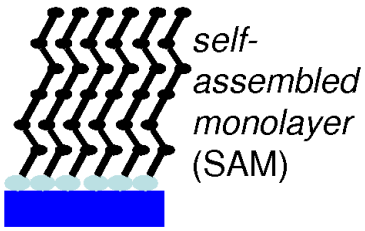


Figure C.3: *Schematic of the self assembled monolayer of molecules on a surface.*

requires the hydroxyl terminated SiO_2. In this context the natural formation by humidity absorption is not enough regarding the comparability of different samples that undergo the pretreatment. The following list gives a detailed description of the pretreatment.

Surface cleaning and hydroxyl termination of the SiO_2

- the samples are cleaned in a solution of H_2O_2/H_2SO_4 (1:4) (piranha solution).
  The solution is an aggressive etchant which, on the one hand, cleans the surface from any organic residua and, on the other hand, leaves a completely hydroxyl terminated surface. The contact material can be very sensitive to this step, therefore the reaction time is limited to 30 s.
- the samples are rinsed in water for at least 5 min.
  This step prevents from ionic residua on the surface.

Application of OTS (liquid phase)

- the samples are stored in a 0.5 vol% solution of OTS (as bought in the purest form) in chloroform.

This step is carried out in a dry nitrogen glove box, because OTS polymerises in contact with water. The OTS reacts on the surface for at least 4 hours, until the process reaches a saturated status.

Application of HMDS (gas phase)

- the samples are stored in a container with an HMDS saturated atmosphere for at least 3 hours.
  This step is achieved at reduced pressure so that the HMDS (as bought, liquid) vaporises.

Final steps

- the samples are cleaned in acetone (5 min, ultrasonic bath).
- the samples are cleaned in isopropanol (5 min, ultrasonic bath).
  These cleaning steps remove the deposited and not chemically bonded molecules from the surface.
- the samples are dried.

C.2 Contact angles

A proof of the hydrophilic surface is given by the high value of the contact angle of a drop of water on the surface. In the case of OTS-treated SiO_2 the value of α is measured $> 100°$. In investigations on contact angles depending on the time of the OTS-treatment and

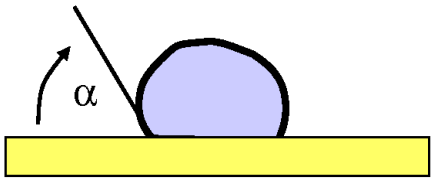


Figure C.4: *The schematic definition of the contact angle α of a water drop on SiO_2.*

the temperature of the solution, an angle of over 100° is achieved by a time of more than 3 hours or at an elevated temperature of 50°C for a reduced time. The HMDS-treatment results in a reduced contact angle.

C.3 Impact on device performance

In this section the impact of the pretreatment with a special regard on the materials investigated in the experimental part will be discussed. It will give experimental evidence that leads to the choice of the optimised pretreatment necessary for best performing devices with respect to the active layer material and its deposition method. The increase in performance of OFETs due to the silanisation of the surface has been confirmed for vacuum deposited pentacene [154] and the polymer poly-hexylthiophene (P3HT) [155]. For the pentacene results the application of an OTS-treatment increased the mobility by a factor of six. Results in the group confirm this for the DH4T [40, 108]. Therein, the OTS-treatment increased the mobility by a factor of three compared to HMDS.

Apart from better homogeneity during growth by vacuum evaporation, the silane/silazane treatment also gives rise to advancements of TTF-based OFETs for the solution processed single crystals. The only piranha-cleaned surface results in the formation of small and thin crystals [111]. The general device performance in drop-cast deposited samples, especially the mobility, is reduced compared to OTS or HMDS treated ones. However, the difference between pretreatments with the two silane turned out to be small. Therefore, often the less elaborate HMDS treatment is applied. For the vacuum evaporated material, no HMDS treatment was tested due to the experience with DH4T and reported advantages of the OTS treatment in combination with a vacuum evaporation deposition [154, 155]. The OTS-treatment again turns out to increase the performance compared to a cleaned hydrophilic surface. The behaviour of PTAA was vastly analysed in a standard characterisation analysis [143], which pointed out the benefit for device performance of a hydrophobic surface. However, the dewetting of the surface during the spin-cast deposition of the solution was an issue.

Appendix D

Atomic force microscopy on films of evaporated DB-TTF

In this appendix the growth mechanism of evaporated DB-TTF will be investigated on OTS pretreated (cf. the previous appendix) SiO_2 wafers. The material is deposited via organic molecular beam deposition as described in appendix A in ultra-high vacuum ($< 10^{-8}$ mbar). Here, the study is focused on the growth parameters:

- *the material flux* f_m, controlled by the temperature of the Knudsen evaporation cell and monitored using a microbalance
- the substrate temperature T_{sub}
- the layer coverage

The investigation of the growth mechanism is interesting with respect to the application in thin-film devices as the OFET due to the scaling of performance with long-range crystalline order in the film. The deposited layers are analysed *ex situ* by atomic force microscopy (AFM) in contacting mode at a constant force of 2 nN and different field sizes. The resulting height profiles are then statistically evaluated.

The direct and decisive conclusion is a three dimensional growth mode (Vollmer-Weber, cf. appendix A). In the following the influence of the growth parameters will be presented in detail. The calibration of the microbalance output is performed with respect to the average layer thickness $< d >$ measured by AFM, which will be described in the following.

The reader is encouraged to read a more detailed version of this study including more background on the statistical methods in the diploma thesis [111]. Here, the most relevant aspects, which are required for the appreciation of the DB-TTF OFET results presented in the previous chapters, are summarised.

D.1 Influence of the material flux f_m

The strong influence of the material flux on the number of crystallisation centres on the surface becomes clear when analysing the result of the deposition of a small amount of material. The two optical micrographs in fig. D.1 show the behaviour on an OTS-treated SiO_2 surface at room temperature. At a deposition rate of 0.18 nm/min there are less crystallisation centres formed compared to a nine times higher flux, where molecules stick with a higher rate.

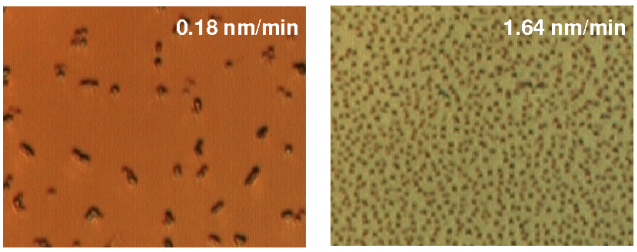


Figure D.1: *Optical micrographs of 9.2 nm (nominal height) DB-TTF grown on SiO_2 at different material flux f_m, OTS-treated, and $T_{sub} = 24°C$).*

When the layer thickness is increased the formed crystallites grow together. In the case of a higher rate this means the formation of more but smaller domains due to the increased number of crystallisation centres. The series of AFM images in fig. D.2 show DB-TTF layers of approx. (92 ± 5) nm height with a clear dependence on the deposition rate. Additionally to the different grain size, which is directly connected to the flux controlled number of crystallisation centres, the 0.18 nm/min sample shows a different type of crystal growth also rudimentally visible in the 1.1 nm/min sample. The height distribution is displayed in

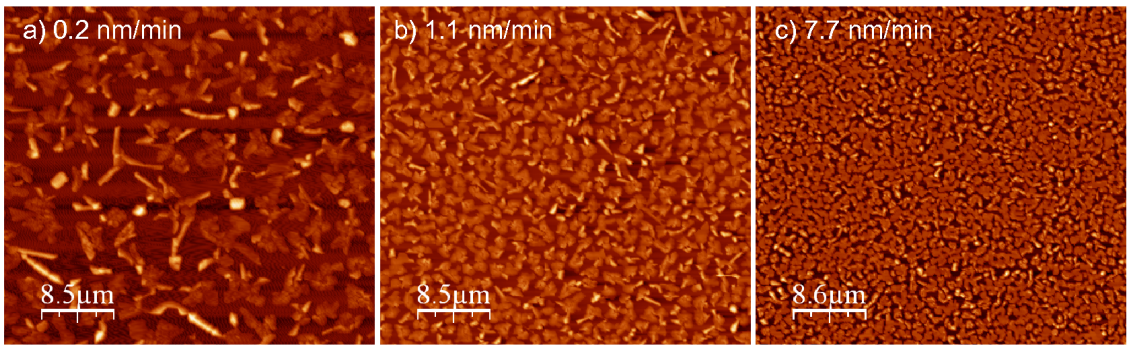


Figure D.2: *AFM images of (92 ± 5) nm DB-TTF grown on SiO_2 at different material flux f_m, OTS-treated, and $T_{sub} = 24°C$.*

the next figure. The diagram in fig. D.3 results from the AFM results (resolution of images 512×512 pixels) with respect to the attributed height. The widest distribution is attributed to the lowest f_m. Also the peak's location value d_p is the higher one (127 nm) compared to the other rates. In the high rate sample the distribution is the smallest with d_p of 86 nm. The conclusion is that an increased f_m favours the formation of an increased number

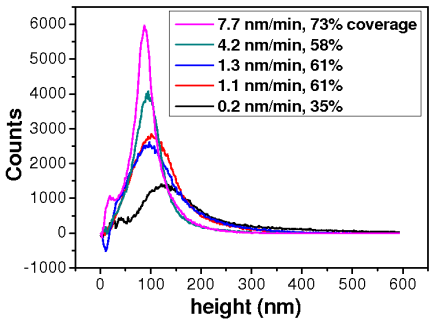


Figure D.3: *Distribution of the height of deposited material in the evaporated DB-TTF layers from fig. D.2.*

of grains resulting in a more equalised height distribution. The smaller f_m is, the more the growth mechanism is three dimensional in larger crystallites. The electrical transport characterisation has shown that the positive effect of a more homogeneous layer predominates the effect of the larger crystallites. This may also stem from the increased number of gaps between the crystallites in the larger island growth which causes a reduction of current paths between the electrodes of an OFET. Too fast a growth, however, causes a negative effect of the increased density of created grain boundaries. The best performance of DB-TTF OFETs was achieved at $f_m \approx 1$ nm/min.

D.2 Influence of the substrate temperature T_{sub}

The substrate temperature influences the growth mainly by the mobility of molecules arriving at the surface. The smaller T_{sub} is the more molecules stick directly at the surface after arrival. In the other case, molecules are mobile and the probability to stick to other molecules is increased. This behaviour is also very material specific. The situation in the vacuum deposited DB-TTF is illustrated in the AFM images of fig. D.4 using a small material deposition of nominally 9.2 nm average height. The four images show the result of the same amount of material deposited at OTS-treated SiO_2 at T_{sub} of 100 °C, 80 °C, 60 °C, and 40 °C. Although the resolution of the 100 °C image is nearly twice as high as the others the behaviour of increasing grain formation for decreasing T_{sub} is obvious. An estimation of the grain heigth results in a reduced height for the lower temperatures. The average grain height decreases from 100 nm down to 45 nm when T_{sub} is decreased from 100 °C to 40 °C.

The conclusion is comparable to the f_m influence, but antiproportional: a lower substrate temperature favours the formation of grains with a higher density resulting in a narrower height distribution. The higher T_{sub} is, the more the growth mechanism is three dimensional in larger crystallites. Concerning the electrical transport properties no advantages of a T_{sub} above room temperature, like e.g. in DH4T, were found.

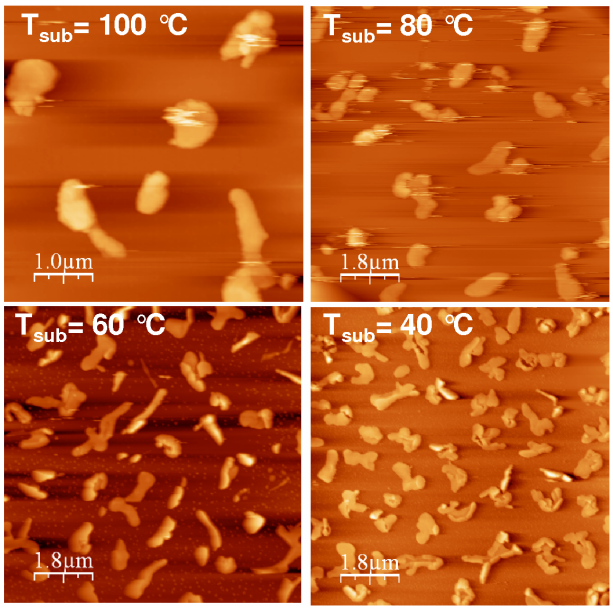


Figure D.4: *AFM images of small material coverage (<d> = 9.2 nm) of DB-TTF on OTS-treated SiO_2 under variation of the substrate temperature and the corresponding height profile.*

D.3 Analysis of the material coverage

The three dimensional growth of the material only allows to denote an average height using statistical estimation of the deposited material in combination with the grade of surface coverage. The details of AFM images in fig. D.5 show six samples with different amounts of material deposited. All SiO_2 surfaces are OTS-treated and T_{sub} is room temperature. Due to this the formation of crystallisation centres is comparable for all samples. The deposition rate varies slightly between 2 and 4 nm/min. This, however, does not influence the observation of the average layer thickness <d>, because it results in the averaging of all material with respect to the surface.

The analysis concerning coverage and microbalance output translated into average height is done in the diagrams of fig. D.6. In diagram 1 the image pixels are attributed to the analysed height. The fluctuations near 0 nm height result from the statistical subtraction of the underground. In the next diagram, the area under the curves of diagram 1 is calculated, which gives the volume of the material deposited. The average height results after normalisation with respect to the number of pixels. In diagram 3 it is plotted versus the micro balance output in order to prove the linearity of the output and the calibration factor which is calculated to

$$< d[nm] >= (1.83 \pm 0.10)[\frac{nm}{MBU}] \cdot d_{MB}[MBU] \qquad \text{(D.1)}$$

where d_{MB} denotes the output of the micro balance in *micro balance units (MBU)*.

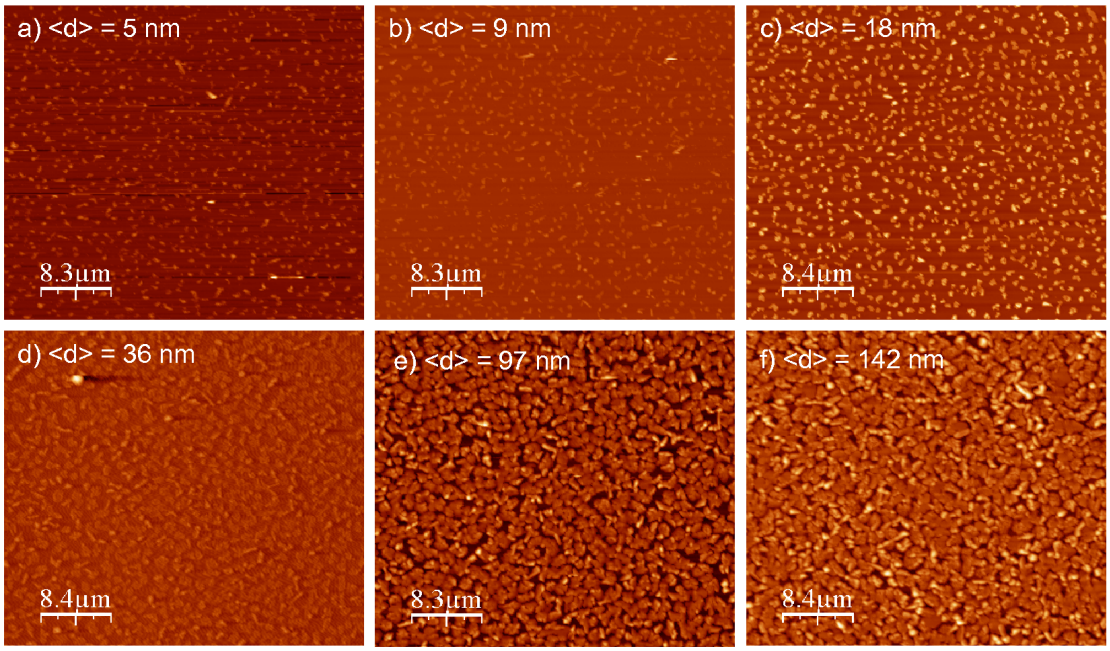


Figure D.5: *AFM images of 8.3 µm × 8.3 µm OTS-treated SiO_2 surface covered with different amount of DB-TTF material, $T_{sub} = 24°C$.*

The last diagram estimates the amount of material for a full coverage of the surface, in other words, when the material has completely grown together. Following an empirical model [156], the connection between coverage Φ and layer thickness <d> is given by $\Phi = a \cdot < d >^b$ with the fitting parameter a and b. Under the condition of 0% coverage for no material deposited the best fit results in a complete coverage at 154 nm deposited material.

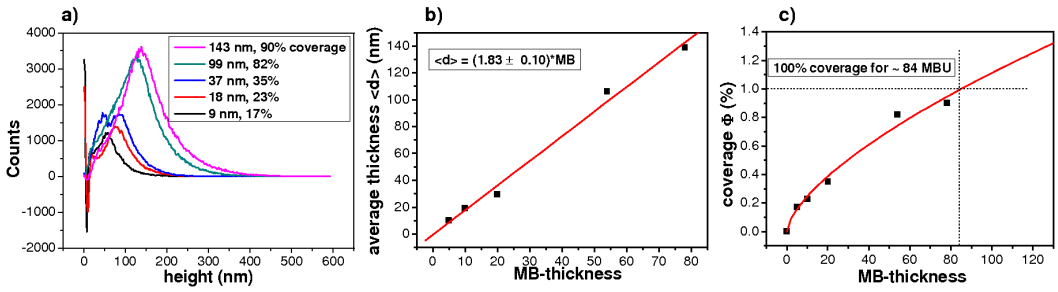


Figure D.6: *Analysis of the average material height and the coverage of DB-TTF on OTS-treated SiO_2 surface based on the AFM data from fig. D.5.*
Diagram (a) monitors the distribution of height in the investigated images. Diagram (b) shows the average height <d>. Diagram (c) uses an empirical model [156] for the estimation of the complete surface coverage.

The resulting effect in OFETs is a strong dependence of performance on layer thickness. Where in DH4T the sole contribution of the first monolayers of material could be proved, the TTFs do not saturate with respect to the layer thickness.

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5. ***High-mobility tetrathiafulvalene organic field-effect transistors from solution processing***
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Contributions to conferences (1^{st} author only)

1. ***Temperature dependence of the field-effect mobility of $\alpha\alpha$'-dihexylquaterthiophene (DH4T)***
   Spring Meeting of the German Physical Society 2003 in Dresden, Talk

2. ***Downscaling of thiophene based OFETs to the nanometer regime***
   Spring Meeting of the German Physical Society 2004 in Regensburg, Poster presentation

3. ***Optimized sub–μm organic thin-film transistors: the influence of contacts and oxide thickness***
   Spring Meeting of the European Materials Research Society 2004 in Strasbourg, France, Talk

4. ***Optimisation of contacts for downscaling of organic thin-film transistors***
   Spring Meeting of the German Physical Society 2005 in Berlin, Talk

5. ***Suppression of short-channel behaviour in deep sub-micron polymer thin-film transistors***
   International Conference on Organic Electronics (ICOE) 2005 in Eindhoven, The Netherlands, Talk

6. ***Fabrication and characterisation of polymer thin film transistors in the sub-micrometer channel regime***
   1^{st} Naimo Summerschool 2005 in Erice, Italy, Poster presentation

7. ***A process for screening of organic semiconductor properties based on sub micron thin film transistors***
   Spring Meeting of the German Physical Society 2006 in Dresden, Poster presentation

8. ***Solution processed single crystal organic field-effect transistors based on tetrathiafulvalene derivates***
   Spring Meeting of the German Physical Society 2006 in Dresden, Poster presentation

9. ***High performance organic field-effect transistors based on solution processed tetrathiafulvalene derivatives***
   International Conference on Organic Electronics (ICOE) 2006 in Eindhoven, The Netherlands, Talk

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Curriculum Vitae

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Buchholz i.d.N., Oktober 2009

(Michael Leufgen)

Ehrenwörtliche Erklärung

gemäß § 5 Abs. 2 Ziff. 2, 3 und 5
der Promotionsordnung vom 22. September 2003 der Fakultät für Physik und Astronomie
der Universität Würzburg

Hiermit erkläre ich ehrenwörtlich, dass ich die Dissertation selbständig und ohne Hilfe eines kommerziellen Promotionsberaters angefertigt und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Die Dissertation wurde bisher weder in gleicher noch in anderer Form in einem anderen Prüfungsfach vorgelegt.

Am 8. Mai 2003 wurde mir von der Universität Würzburg der akademische Grad
Diplom–Physiker (Univ.) verliehen.
Weitere akademische Grade habe ich weder erworben noch versucht zu erwerben.

Buchholz i.d.N., Oktober 2009

(Michael Leufgen)