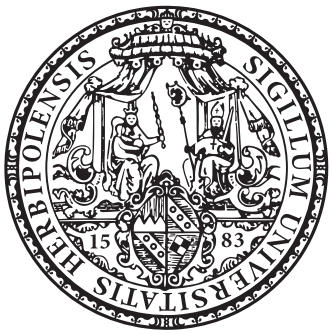

Fabrication of magnetic artificial atoms

Dissertation

zur Erlangung des
naturwissenschaftlichen Doktorgrades
der Julius-Maximilians-Universität Würzburg

vorgelegt von
Radu-Gabriel Dengel
aus Slatina

Würzburg 2013

Eingeeicht bei der Fakultät für Physik und Astronomie

Gutachter der Dissertation:

1. Gutachter: Prof. Dr. Laurens W. Molenkamp

2. Gutachter: Prof. Dr. Bert Hecht

Prüfer im Promotionskolloquium:

1. Prüfer: Prof. Dr. Laurens W. Molenkamp

2. Prüfer: Prof. Dr. Bert Hecht

3. Prüfer: Prof. Dr. Reinhold Oppermann

Parts of this thesis have been published elsewhere

- R.-G. Dengel, A. Frey, K. Brunner, C. Gould, L. W. Molenkamp, *Fabrication of magnetic artificial atoms*, Nanotechnology **23**, 395301 (2012)
- A. Frey, M. Ruth, R.-G. Dengel, C. Schumacher, C. Gould, G. Schmidt, K. Brunner, L. W. Molenkamp, *Semimagnetic II-VI semiconductor resonant tunneling diodes characterized by high-resolution X-ray diffraction*, Journal of Crystal Growth **312**, 1036 (2010)

Contents

Zusammenfassung

Die Fabrikation und Erforschung künstlicher Atome ist hinsichtlich ihres physikalischen Verständnisses und ihrer Herstellungstechnologie weit fortgeschritten. Diese werden vorwiegend in lateralen oder vertikalen Quantenpunkten (QDots) aus dem III-V Materialsystem erzeugt. Allerdings ist es derzeit nicht möglich, künstliche Atome mit ausgeprägten magnetischen Eigenschaften herzustellen, um diese zu untersuchen. Diese Arbeit präsentiert die Punkt-für-Punkt-Entwicklung der Herstellungstechnologie sowie erste experimentelle Beobachtungen von künstlichen magnetischen Atomen aus dem II-VI verdünnt magnetischen Halbleitermaterialsystem (Zn,Cd,Be,Mn)Se. Das der Entwicklung zugrunde liegende elektronische Bauelement ist eine resonante Tunneldiode (RTD) aus dem II-VI Halbleitermaterialsystem, die früher bereits entwickelt wurde.

Auf der Basis des konstanten Wechselwirkungsmodells, das zur Beschreibung von künstlichen Atomen herangezogen wird, sowie der Giant-Zeeman Energieaufspaltung im paramagnetischen Quantentrog (QW) (Zn,Cd,Mn)Se der Doppelbarrierenstruktur wird die Entstehung künstlicher Atome mit starken und interessanten magnetischen Eigenschaften erwartet. Aus Experimenten an künstlichen Atomen ist bekannt, dass es am besten ist, die RTDs, aus denen die Quantenpunkte hergestellt werden, im linearen Transportbereich um $U_{SD} \approx 0$ V zu betreiben. Die Ausgangs-II-VI RTD, mit einer QW-Breite von 7 nm, hat ihre erste Resonanz, aufgrund der großen Energieabstände in der k_z Quantisierung erst bei 160 mV. Da diese Energiegrößenordnung nicht mit einer Steuerungselektrode (Gate) manipuliert werden kann, ist es notwendig, die Resonanz von vornherein physikalisch in die Nähe der Fermienergie der Kontakte zu bringen. Als erstes wird die QW-Breite erhöht, die jedoch die Resonanz deutlich verbreitert aber ihre Position auf der Spanungsskala nicht weit genug erniedrigt. Die Erniedrigung der Position bis auf 0 V wird stattdessen über die Verkleinerung der Bandlücke im 7 nm breiten QW durch das Hinzufügen von $\sim 7.6\%$ Cd erreicht.

Die II-VI RTD wird pseudomorph auf einem GaAs Substrat gewachsen. Elektrische Felder und die Aufladung der III-V/II-VI Grenzfläche verhindern die Verwendung der Substratrückseite als einen Rückseitenkontakt des Bauelements. Diese Eigenschaft stellt neue Anforderungen an die Kontaktanordnung des RTD-Bauelements. Aufgrund der durchgehenden, hochdotierten Rückseitenschicht müssen die Topkontakt-, Rückseiten- und Gatekontaktbondelektrode voneinander physikalisch getrennt werden, um einen eindeutigen Strompfad durch die Struktur festzulegen. Es wird deshalb ein zuverlässiger und Oberflächen nichtkontaminierender Herstellungsprozess für $\geq$ 1,3 μm tiefe Trenngräben entwickelt. Er basiert auf dem Aufbringen von 100 nm Ti als Maske während des

Trockenätzprozesses, die sich anschließend problemfrei entfernen lässt. Darüber hinaus müssen Methoden zur Topkontaktierung des submikrometer breiten Türmchens ausgelotet werden, da eine direkte Kontaktierung mit dem Drahtbonder nicht möglich ist. Das Linienmesaprinzip, das von Austing *et al.* [Aust 96] entwickelt wurde und nun standardmäßig in III-V (QDots) verwendet wird, wird auf seine Anwendbarkeit in der II-VI RTD getestet. Da 200 nm breite Linien immer noch elektrisch leitfähig sind, kann diese Methode nicht verwendet werden. Die Brückentechnologie ist deshalb weiterhin die Methode der Wahl, muss allerdings hinsichtlich der PMMA-Lackdicke angepasst werden, um ein Überbrücken der tiefen Trenngräben zu gewährleisten.

Aus den gewonnenen Erkenntnissen während der Entwicklung des Herstellungsverfahrens für die Linien, ist der Prozess zur Verkleinerung der Türmchendurchmesser hin zu submikrometer Abmessungen erfolgreich entwickelt und angewendet worden. In diesem Zusammenhang wird wieder eine Ti-Trockenätzmaske mit einer Dicke von 60 nm zum Trockenätzen von 250 nm hohen Türmchen verwendet. Dem Ar-Ionenstrahl wird BCl_3 als chemische Komponente hinzugefügt. Weiterhin verhindert ein geringerer Einfallwinkel die Ausbildung von Ätzgräben und erzeugt steilere Seitenwände an den Türmchen. Dieses Grundherstellungsverfahren für künstliche Atome beinhaltet das Entfernen des überschüssigen Ti mittels Flusssäure. Abweichungen in den physikalischen Eigenschaften unterschiedlicher Substrate haben zu einer Weiterentwicklung dieses Prozessschrittes geführt. Dabei wird das überschüssige Ti der Trockenätzmaske ausschließlich trockenchemisch entfernt. Die so hergestellten Strukturen werden elektrisch bei 4,2 K getestet und weisen einen zunehmenden Einfluss der Quantisierung durch die laterale Abnahme der Abmessungen auf.

Nachdem ein zuverlässiges Herstellungsverfahren für Submikrometertürmchen mit Abmessungen bis herunter zu 200 nm Durchmesser entwickelt wurde, wird das wichtigste Element, das Gate, das die Untersuchung der elektrischen Eigenschaften der QDots erlaubt, hinzugefügt. Die Unterschiede zwischen dem III-V und II-VI Materialsystem hinsichtlich der Bauteilhöhe, Schichtabfolge, des Einflusses von Ätzchemikalien und des Nichtvorhandenseins eines idealen Schottky-Kontakts erfordern die Entwicklung eines geeigneten Designs sowie Herstellungsprozesses des Gates. Außerdem zeigt die Untersuchung der elektrischen Eigenschaften der mittels PECVD konform aufgebrachten Dielektrika, dass mit Si_3N_4 eine größere Ladungsträgermanipulation möglich ist, aber die auftretende Hysterese ebenfalls nicht zu vernachlässigen ist. Da das Gate nicht mittels selbstlimitierenden Schattenaufdampfens aufgebracht werden kann, wird das Gate mit dem Elektronenstrahl definiert. Hierzu ist eine hohe Präzision unter Berücksichtigung systematischer Abweichungen bei der Ausrichtung erforderlich. Eine Weiterentwicklung zu einem flächigen Gate erhöht zwar die Komplexität des Herstellungsverfahrens, aber durch das Verwenden einer schützende Lackmaske kann das überschüssige Metall auf der Türmchenspitze entfernt werden. Allerdings löst die neue Methode die Schwierigkeiten mit der Ausrichtung. Die vertikale Ausrichtung des Gates wird erreicht, indem die Ätzraten und -tiefen des Halbleiters sowie Aufbringraten und -dicken des Dielektrikums sorgfälltig überprüft werden. Die elektrischen Messungen an den so hergestellten Bauteilen zeigen, dass das Verfahren funktioniert. Allerdings werden im Falle einer Falschpositionierung auch die

daraus resultierenden Einflüsse sichtbar.

Abschließend wird der komplette Herstellungsprozess von Anfang bis Ende, wie in [Deng 12] vorgestellt, präsentiert. Das Grundherstellungsverfahren wird mit dem verbesserten und universelleren Herstellungsprozess ergänzt. Der Letztere enthält Veränderungen, die die Herstellung flexibler auf Abweichungen reagieren lassen. Der verbesserte Herstellungsprozess entkoppelt das Verfahren vom II-VI Materialsystem, so dass er auf andere Materialsysteme ebenfalls angewendet werden kann. Tieftemperaturmessungen, an einem 250 nm breiten Türmchen aufgezeichnet, zeigen die Ausbildung von QDots. Die hohen Widerstände des Bauteils haben allerdings Ströme zur Folge, die vergleichbar zu den Leckströmen durch den Isolator sind. Aus diesem Grund müssen die DC-Messungen durch Lock-in Messungen ersetzt werden. Hierbei wird eine kleine AC-Anregungsspannung bei niedrigen Frequenzen hinzugefügt. Die niedrigen Frequenzen verhindern ein kapazitives Leck. Darüberhinaus weisen die Messungen von Coulomb-Oszillationen bei unterschiedlichen Anregungsspannungen sowie das Stabilitätsdiagramm das Vorhandensein einer Blockade in Serie mit dem QDot auf. Außerdem deuten die aufgezeichneten Fock-Darwin-Spektra auf die Enstehung von mehreren QDots hin, da Spektra überlagert sind. Trotzdem kann man eine ausgeprägte paramagnetische Komponente beobachten. Beim Anlegen eines Magnetfeldes ändert sich die Position der Energieniveaus entsprechend einer Brillouin-Funktion. Dies belegt die ausgeprägten magnetischen Eigenschaften im QDot. Durch die zusätzlich beobachtete k_x-k_y Quantisierung wird die Entstehung von künstlichen magnetischen Atomen belegt. Aufgrund der Bauteilunzulänglichkeiten können keine quantitativen Schlüsse gezogen werden. Das Verhalten des Bauteils entspricht jedoch dem berechneten Spektrum, zusammengesetzt aus dem konstanten Wechselwirkungsmodell und der Giant-Zeeman Energieaufspaltung im II-VI Halbleiter. Insgesamt führt die Aufspaltung dazu, dass eine Spinausrichtung mit zunehmendem Magnetfeld dominiert. Dies unterstreicht nochmals den paramagnetischen Charakter der künstlichen Atome.

Summary

The study and fabrication of artificial atoms, consisting of lateral or vertical quantum dots (vQDots), primarily from the III-V material system, are well advanced in understanding and technology. However, to date the field lacks the capability to create and investigate artificial atoms with pronounced magnetic properties. This thesis presents a detailed technology development of the fabrication process and first experimental observations of artificial magnetic atoms based on a previously established resonant tunneling diode (RTD) heterostructure from the II-VI diluted magnetic semiconductor (DMS) alloy (Zn,Cd,Be,Mn)Se.

From the constant interaction model describing artificial atoms, and the Giant-Zeeman energy splitting in the paramagnetic (Zn,Mn)Se quantum well (QW) of the double barrier heterostructure (DBH), the formation of artificial atoms with a strong and exciting magnetic response is expected. As is known, the best regime to operate the RTD devices forming the vQDot is in linear transport at source-drain bias voltages of $U_{SD} \approx 0$ V. However standard II-VI RTD heterostructure with a QW of 7 nm exhibits the first resonance at bias voltages of about 160 mV, due to the large energetic spacings in the k_z quantization. Since this energy scale cannot be reasonably addressed by gate, it is necessary to physically lower the energy levels down to the vicinity of the Fermi energy of the leads. The first attempt is done by increasing the QW width, which adds significant broadening but does not lower the resonance enough. Instead the reduction of the 7 nm QW's energy bandgap by the incorporation of $\sim 7.6\%$ Cd is shown to be the correct approach to line up the QW's energy level with the contacts Fermi level.

The II-VI RTD heterostructure has to be grown pseudomorphic on a GaAs wafer. Electrical fields as well as the charging at the III-V/II-VI interface prevent the use of the wafer backside as a real backside contact and therefore impose new challenges to the contacting scheme of the RTD devices. Because of the continuous highly doped backside layer, the top contact, backside and gate bonding pads requires physical separation of the different contact areas to ensure a well defined current path through the device. Therefore a reliable, easily removable and surface non-contaminating fabrication process for ≥ 1.3 μm deep separating trenches is developed based on a 100 nm thick Ti metal mask and dry etching. Also, since submicron pillar dimensions eliminate the possibility of wire bonding the top contact, alternative techniques have to be exploited. The state of the art line mesa method presented by Austing *et al.* [Aust 96] is tested for the II-VI RTD heterostructure. However 200 nm lines are still fully conductive and prove this method to be not applicable to the II-VI devices. An air-bridge technique therefore is

the appropriate top contact method, but it requires some adjustments in the resist layer composition in order to facilitate bridging across the deep and narrow trenches.

From the insights gained on developing a reliable manufacturing method of the submicron line mesas, the RTD pillar width is successfully reduced to submicron dimensions. Once again a ~ 60 nm thick Ti metal dry etching mask is used to fabricate the 250 nm high pillars by using BCl_3 in chemical assisted ion beam etching with argon. Decreasing the incident etching angle steepens the pillar's sidewalls and prevents the formation of etching trenches around it. The developed process, which is part of the basic fabrication process for artificial atoms, involves hydrofluoric acid to remove the excess Ti mask. Variations in the physical properties of different RTD wafers have led to a further development of this step, which now only involves dry etching and a protective resist mask for the excess Ti removal in the end. Electrical characterization, at liquid helium temperature, of the fabricated devices show increasing influence from the lateral confinement through lateral miniaturization of the pillar dimensions.

With a reliable manufacturing process of nano-pillars for working diameters as small as 200 nm, the most important element in the investigation of the electronic properties of the vQDots is now addressed: the application of a gate electrode. The differences between the III-V devices and the II-VI material system in vertical dimensions, the layer sequence, impact of wet etchants and especially the non-availability of ideal Schottky contacts require the development of a suitable design and fabrication process for the gate electrode. Investigating the electric properties of conformal deposited SiO_2 and Si_3N_4 by plasma enhanced chemical vapor deposition reveals that Si_3N_4 provides the higher gating effect, but also exhibits a non-negligible hysteresis. The absence of a shadow masking technique for self aligning the gate requires defining the gate electrode by electron beam lithography. This requires high precision horizontal alignment of the gate by carefully accounting for systematic shifts in the electron beam lithography step. Further development leading to a plane gate method adds extra steps to the complex fabrication process, by once again using a protective resist mask to remove metal on the pillars insulator-covered top contact. Nevertheless this method helps in overcoming issues from unavoidable misalignments. The vertical alignment to the very narrow positioning window is achieved by carefully monitoring of semiconductor etching rates and depths as well as dielectric deposition rates and thicknesses. Electrical characterization measurements prove, on the one hand, the suitability of the method, and on the other hand, reveal influences from vertical misalignment of the gate electrode.

Finally the entire fabrication process from beginning to end, as presented in [Deng 12], is described in detail. This basic fabrication process is supplemented with the improved and more universally applicable manufacturing process that contains the modifications necessary for enhanced versatility in fabrication. Generally speaking the improved process decouples the fabrication from the specific II-V semiconductor alloy used in the work, and makes it easily portable to other material systems. Low temperature characterization measurements recorded in a dilution refrigerator on a 250 nm diameter pillar show the formation of vQDots. The high resistance of these devices leads to currents at $U_{SD} \approx 0$ V of similar order as the leakage current through the dielectric. Thus pure DC mea-

surements have to be replaced by Lock-in experiments, where a smaller AC excitation is added at low frequencies. The later helps to avoid capacitive leakage from the leads. Additionally Coulomb oscillation measurements at different bias voltages and the stability diagram indicated the presence of an extra blockade in series with the formed QDot. The recorded Fock-Darwin spectrum suggest the formation of more than one QDot leading to the observation of superimposed spectra. Nevertheless, a clear and strong paramagnetic component is observable. The Brillouin characteristic of the evolution of the quantized levels in a magnetic field proves the strong magnetic response present in the quantum dot. Together with the clear observation of the k_x-k_y quantization this documents the observation of artificial magnetic atoms. Quantitative findings can however not be extracted from the measurements, due to device imperfections. The behavior qualitatively corresponds to the calculated spectrum of a constant interaction model supplemented with the Giant-Zeeman energy splitting in the II-VI semiconductor. Altogether this leads to a quick domination of the spin-down energy levels as the magnetic field increases, underlining the paramagnetic nature of the artificial magnetic atom.

Chapter 1

Introduction

Beginning with Democritus, who first expressed and developed the idea of atoms as the smallest unbreakable parts of matter, mankind's interest in the elements of our physical world and the laws of their interaction has always remained undiminished. For centuries more and more secrets have been revealed and a comprehensive picture of these building blocks of matter has been gained. Nevertheless some properties of real atoms still can't be studied with the methods on hand due to their physical limitations. To give an example, the electronic 'singlet-triplet' transition of a helium atom as a function of the magnetic field requires several 10^5 Tesla [Thur 82], which are not accessible in any man-made system. Therefore the availability of structures with qualitatively similar physical properties, which however are much more easily accessible, would enable the study of novel physical properties.

In 1986 Watanabe and Inoshita [Wata 86] proposed the novel concept of artificial atoms from a modulation doped III-V semiconductor heterostructures, which they called 'superatoms' at first. Their semi-classical calculations together with Inoshita's *et al.* work [Inos 86, Inos 88] show the formation of well-defined atomic orbitals within the proposed system. However, the formation of artificial atoms proved to be most feasible by the fabrication of quantum dots. These are comparable to small boxes, whose dimensions are of the order of the de Broglie wavelength of the electrons. The 3D confinement of the electron wave gives rise to the emergence of discrete energy levels which resemble atomic orbitals in real atoms.

In order to investigate the electronic transport properties of such QDots one must attach leads to these 0D objects. Thus two possibilities for device configurations are the lateral design, where the leads are attached laterally, or the vertical design, where the QDot is sandwiched between the source and drain contacts. The work of Meirav *et al.* [Meir 90] on narrow interrupted channels into a GaAs/AlGaAs 2DEG facilitated for the first time to the observation of Coulomb blockade in an artificial system. Further improvement of the design led then to the realization of fully tunable lateral QDots [Goul 98, Cior 00]. In contrast, the pioneering work of Esaki, Tsu and Chang [Esak 58, Chan 74] and the progress in molecular beam epitaxy (MBE) resulted in a novel type of devices: the resonant tunneling diodes (RTD). With their double barrier heterostructure (DBH) they

already provide a quantization of the energy in the growth direction. Advances in micro and nano lithography enabled the lateral downscaling of RTDs with properly tunned bandstructure to the region of lateral quantum confinement [Reed 88, Su 91, Tewo 92]. Moreover the addition of a gating electrode [Kina 90, Dell 92a] allows for further manipulation of the bandstructure [Guer 92a, Bent 92, Wang 94b]. A direct control over the lateral quantum confinement in these submicron RTD devices thus leads to a direct influence on the energy levels and the formation of vertical quantum dot (vQDot).

In 1995 Tarucha *et al.* [Taru 95] reported on the fabrication of a single electron transistor from a side-gated GaAs/AlGaAs RTD, which allowed the observation of irregular Coulomb blockade oscillations. This design was then used for devices with an optimized AlGaAs/InGaAs DBH in 1996 [Taru 96]. Inside these 0.5 μm wide circular pillars a 2D disk shaped dot is formed from the lateral confinement of the few-nm thick quantum well. The confinement potential of this disk is best approximated by a two-dimensional harmonic potential which gives rise to degenerate sets of single-particle states. The analysis of the Coulomb oscillations' spacings in the absence of a magnetic field confirms the energetic degeneracies in the QDot and each set of levels can be regarded as a shell. Furthermore a close investigation of the peak spacings for half-filled shells reveals that electrons are added to the QDot following Hund's first rule. These findings reveal that the electronic spectrum in these vQDots represents an analogy to the one of real atoms and that the QDots can be regarded as artificial atoms. Over the last decade, these artificial atoms and the tunability of their electronic properties offered thus a suitable lab environment to test electronic, magnetic or spin related phenomena [Kouw 01, Reim 02, Hans 07] in single or multiple QDots.

Nevertheless all experiments so far have been performed on lateral and vertical devices from the III-V semiconductor material system. Here the addition of magnetic dopants also alters the electronic properties of the system and impedes the fabrication of artificial atoms with a strong magnetic response. Whereas in the II-VI semiconductor material system the incorporation of magnetic ions is isoelectric and thus leaves the electronic properties of the material unaffected. Furthermore it is well known from the intense study and characterization of these diluted magnetic semiconductors, that they exhibit a strong magnetic response, the Giant-Zeeman splitting [Gaj 79, Twar 84, Furd 88]. Based on the work of Slobodskyy *et al.* [Slob 03], Gould *et al.* [Goul 06] and Rüth *et al.* [Ruth 11b] it has been shown that this material can be implemented in electronic devices such as RTDs. On the one hand the strong magnetic response of the material is preserved, on the other hand novel physical properties can be observed, i.e. zero-field splitting of the QW's energetic levels. Therefore the use of the II-VI DMS material system for the fabrication of artificial atoms opens a way to a new field of exciting opportunities for electric and magnetic tunability at once. The first attempt to fabricate gated II-VI submicron RTD devices [Borz 07], however proved to be more challenging than in the III-V semiconductor material system.

In this work the development, the final process for the fabrication and the observation of artificial magnetic atoms from the DMS (Zn,Cd,Be,Mn)Se are presented. The thesis is

organized as follows. The first part of chapter 2 presents the basic physics and electronic transport properties of quantum dot devices of circular symmetry, which form the artificial atoms. In the second part the II-VI heterostructure from (Zn,Cd,Be,Mn)Se is introduced and the magnetic properties of the magnetically doped (Zn,Mn)Se QW are reviewed. It also includes a general look on the implications arising from combining the single-particle energy spectrum with the Giant-Zeeman energy splitting. The last section describes the tunning of the QW in order to bring its lowest energy level as close as possible to the Fermi energy in the leads. This is necessary for performing experiments in the linear transport regime.

Chapter 3 addresses the development of a proper contacting scheme in the submicron devices. Due to the pseudomorphic growth of the II-VI heterostructure on a GaAs wafer, a contact on the wafer backside cannot be used. Instead a continuous highly doped layer below the DBH is used to contact the backside of the device. But in order to avoid parasitic currents a clear current path through the device has to be ensured. Therefore the backside layer and the II-VI superlattice buffer, screening the RTD heterostructure from the III-V/II-VI interface electric fields, have to be cut through. Here the development of a reliable fabrication process for ≥ 1.3 μm separating trenches is presented.

The second part of the chapter presents methods for contacting the top of the submicron pillars. Therefore the idea of metal capped, insulating semiconductor line mesas [Aust 96] is tested for the II-VI heterostructure. However the method proves to be not applicable to our material system and thus the air-bridge technique [Borz 04] is adjusted to the profile of the device.

In the following the miniaturization of the RTD pillars to submicron dimensions and is presented in chapter 4. Here the challenges in the fabrication process are discussed and the necessary solutions are outlined. The different development steps are accompanied by electronic and magnetic transport measurements. These ensures that the electronic and magnetic properties of the RTD heterostructure are unimpaired.

Having established a fabrication process for vQDots from submicron pillars in the II-VI RTD, the addition of the gate electrode is outlined in chapter 5. The requirement of a dielectric material is discussed and subsequently the characterization of the available dielectrics: SiO_2 and Si_3N_4 is presented. Therefore the challenges arising from the current RTD heterostructure are considered in the design as well as the fabrication of the gate electrode in order to ensure maximum functionality. The suitability of the fabrication and its impact on the device functionality is monitored by electrical measurements.

With all fabrication steps established, chapter 6 summarizes the entire process to fabricate artificial magnetic atoms from the II-VI DMS. The basic fabrication method is complemented with a further developed process, which is more universally valid and does not take advantage of any special properties of the used wafer or dielectric material. The second part of this chapter then presents the observation on vQDots from the (Zn,Cd,Be,Mn)Se RTD heterostructure. It discusses the first observations of the formation of an artificial magnetic atom considering the electronic and magnetic device properties.

Chapter 2

State of the art quantum dots and diluted magnetic semiconductors

At the time this thesis has been started, a demonstration of artificial magnetic atoms has not yet been done. The study of non-magnetic artificial atoms however was a rather mature field. Indeed already in the 1990's the formation of semiconductor quantum dots in lateral and vertical configuration has been extensively investigated and a parallel to observations made in real atoms has been pointed out [Asho 96, Kouw 97]. The relevant physical characteristics of these artificial atoms from quantum dots are examined in the first section of this chapter. Since the fabrication of artificial atoms from a magnetic semiconductor is the scope of this work, the used II-VI material system from (Zn,Cd,Be,Mn)Se is presented subsequently. It is also shown, how the magnetic properties resulting from adding Mn into the II-VI semiconductor are expected to modify the quantum dot's magnetic response. In the last part of the chapter the enhancements to the state of the art double barrier heterostructure developed by Slobodskyy *et al.* [Slob 03] are presented together with the results from electronic transport measurements. These results lead to a II-VI RTD heterostructure suitable to perform the necessary electronic transport on quantum dots in the linear regime.

2.1 Artificial atoms from quantum dots

This section presents a brief overview on the physics and electronic transport through semiconductor quantum dots, as artificial atoms, relevant to this work. The reviews on artificial atoms and few-electron quantum dots of Ashoori [Asho 96], Kouwenhoven *et al.* [Kouw 97, Kouw 01], Reimann *et al.* [Reim 02] and Hanson *et al.* [Hans 07] as well as the PhD thesis of T. H. Oosterkamp [Oost 99] serve as a basis.

Quantum dots from semiconductors, forming 0D objects, are structures of a few 100 nm in size holding a number 1 to 1000 free electrons. For electronic transport these small boxes are coupled via tunnel barriers to the reservoirs in the leads. The electrostatic potential of a quantum dot can be altered relative to the reservoirs by adding one or more gate electrodes to the system. With that said changing the gate voltage allows to

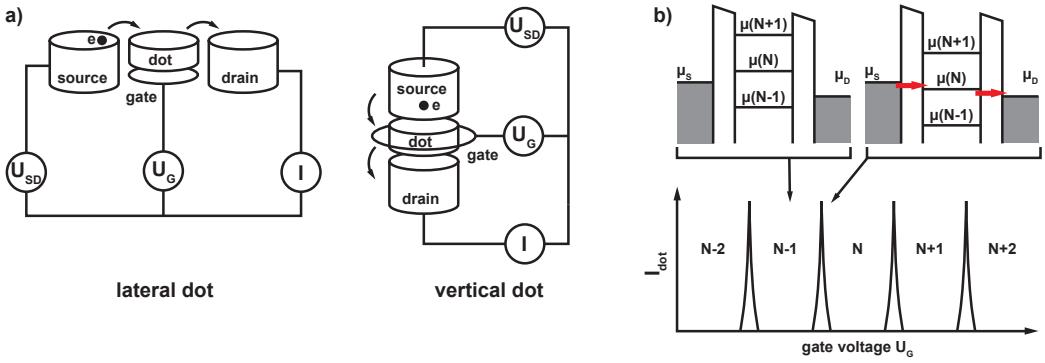

Fig. 2.1: a) Schematic quantum dot design of lateral and vertical configuration. The quantum dot is depicted by a circular disc with gapped connections (representing the tunnel barriers) to source and drain reservoirs. Creating a closed-circuit the current I through the device is measured with respect to a bias voltage U_{SD} and a gate voltage U_G. b) Schematic illustration of the Coulomb blockade in the case of low bias regime. (Left) No electrochemical potential of the dot is located within the bias window, thus no current flows through the device. (Right) The $\mu(N)$ level is situated inside the bias window, allowing electrons to pass from the source to the drain and enabling a current flow. (Bottom) The resulting current I_{dot} versus U_G. [Kouw 97, Hans 07]

precisely vary the number of electrons within this box. Attaching voltage and current probes to this three terminal device, the electronic properties are investigated (fig.2.1a.)

The observed electronic properties of these quantum dots are similar to the discrete energy spectrum in real atoms but dominated by mainly two effects: the Coulomb repulsion of the electrons on the dot and the discrete energy spectrum arising from the confinement in all three directions. These electronic properties are described to first approximation by the constant interaction model, which is based on two assumptions. First, the interaction of the electrons inside the dot with the electrons of the environment is parametrized by a constant capacitance C,

$$C = C_S + C_D + C_G \tag{2.1}$$

where C_S, C_D and C_G stand for the capacitance of the dot to the source, drain and gate, respectively. Second, the single-particle energy-level spectrum of the 0D object is assumed to be independent of these Coulomb interactions and not affected by the number of electrons in the dot. The total energy of an N electron dot is thus approximated by

$$U(N) = \frac{(-e(N - N_0) + C_G V_G)^2}{2C} + \sum_{n=1}^{N} E_{n,l}(B) \tag{2.2}$$

where e is the electron charge, N_0 stands for the number of electrons on the dot at $V_G = 0$ V, the continuously alterable charge $C_G V_G$ denotes the charge that is induced on the dot by V_G and the last term is a sum over the occupied single-particle energy levels $E_{n,l}(B)$. Only the later are dependent on the applied magnetic field and are given by the confining potential of the quantum dot.

The electrochemical potential $\mu(N)$, representing the transition between the N-electron ground state and the $(N-1)$-electron ground state, is defined as

$$\begin{aligned}\mu(N) &\equiv U(N) - U(N-1) \\ &= \left(N - N_0 - \frac{1}{2}\right) E_C - e\frac{C_G}{C} V_G + E(N)\end{aligned} \tag{2.3}$$

with $E_C = e^2/C$ the charging energy and E_N the topmost filled single-particle energy level of the N-electron dot. The spacing of adjacent electrochemical potentials is then given by the addition energy

$$\begin{aligned}E_{add}(N) &\equiv \Delta\mu(N) = \mu(N+1) - \mu(N) \\ &= E_C + E_{N+1} - E_N = E_C + \Delta E\end{aligned} \tag{2.4}$$

consisting solely of the charging energy E_C and the spacing ΔE among two consecutive discrete energy levels E_{N+1} and E_N.

As previously reported, the energy levels $E_{n,l}$ form the single-particle energy spectrum which arises from the confinement potential of the dot. By fabricating devices of different shapes, i.e. triangle, square, etc., one can only introduce asymmetries in the lateral confinement deforming a rotationally symmetric harmonic potential [Taru 97]. These induced asymmetries mainly lift degeneracies originating from a highly symmetric confinement potential. Thus the circular shape, having however the highest degree of symmetry and having been extensively investigated in the past, is also selected for the pillars in this work. Within a pillar of a circular design the vertical quantum dot has then the shape of a 2D disc formed from the circular quantum well between the barriers. The resulting confinement potential of the disc can be approximated by a 2D harmonic potential $V(r) = \frac{1}{2} m^* \omega_0^2 r^2$, where ω_0 is the oscillator frequency. The Schrödinger equation for this 2D harmonic potential in the presence of a magnetic field B can be solved analytically and leads to the Fock-Darwin spectrum [Fock 28, Darw 30]

$$E_{n,l} = (2n + |l| + 1)\hbar\sqrt{\frac{1}{4}\omega_c^2 + \omega_0^2} - \frac{1}{2} l\hbar\omega_c \tag{2.5}$$

where $\hbar\omega_0$ denotes the electrostatic confinement potential, $\hbar\omega_c = \hbar eB/m^*$ is the cyclotron energy, m^* stands for the effective electron mass and the radial and angular quantum numbers are n and l. For $B = 0$ T the high degree of symmetry in the circular design leads to sets of energetically degenerate single-particle levels. The emerging shell structure with the 'magic' numbers 2, 6, 12,... [Kouw 01], see figure 2.2, resembles the one of real atoms with completely filled shells at the atomic numbers 2, 10, 18,... These physical characteristics of a quantum dot, which are akin to the ones in real atoms, has lead to the term 'artificial atom'.

It should further be mentioned that each energy level $E_{n,l}$ is two-fold spin-degenerate. The alignment of the spins with the external field can however be accounted for by the

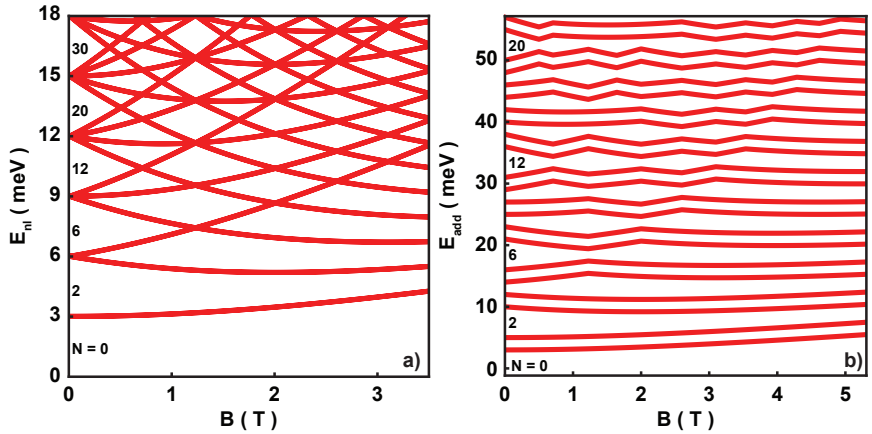

Fig. 2.2: a) Calculated Fock-Darwin spectrum of a parabolic potential with $\hbar\omega_0 = 3$ meV in a GaAs quantum dot, describing the evolution of single-particle states $E_{n,l}$ in a magnetic field. Each state is two-fold spin-degenerate, due to Zeeman energy neglection. b) The addition energy E_{add} of this system is given by equation 2.4 and using a fixed charging energy $E_C = 2$ meV.

Zeeman spin-splitting $\Delta E_Z = g\mu_B B$, where g is the Landé-factor and μ_B the Bohr magneton. In the III-V material system the g-factor is small (g_{GaAs} = -0.44), so E_Z ($E_Z(GaAs)$ = 25 μeV) is much smaller than the other energy splittings in a quantum dot and thus usually neglected, leaving each single-particle energy level two-fold degenerate.

More thorough investigations of the evolution of the energy levels in an increasing magnetic field revealed a spin-polarized filling of the shells at $B = 0$ T [Taru 96]. In other words degenerate states are, as much as possible, first filled by electrons with parallel spins up to the point where the shell is half filled, which corresponds in fact Hund's first rule in atomic physics. In the energy spectrum of a quantum dot this becomes apparent by enhancements for i.e. $N = 9$, corresponding to a spin-polarized, half-filled third shell. This fact once more emphasizes the analogy between the physical properties of the 0D object formed in a quantum dot and real atoms.

When performing measurements on a quantum dot there are three temperature regimes to be distinguished:

(1) $e^2/C \ll k_B T$, the high temperature limit, where the discrete charging cannot be discerned,

(2) $\Delta E \ll k_B T \ll e^2/C$, the classic Coulomb blockade regime, where discrete charging is observable, but many single-particle energy levels are excited by thermal fluctuations,

(3) $k_B T \ll \Delta E \wedge k_B T \ll e^2/C$, the quantum Coulomb blockade regime, where discrete charging and single-particle energy levels are examinable.

For performing transport spectroscopy on a quantum dot's energy spectrum the third regime is required. In order to observe effects due to discrete charging a second criterion has to be met by any device. Based on the typical time to charge and discharge the quantum dot $\Delta t = R_t C$ and the Heisenberg uncertainty $\Delta E \Delta t > h$ the tunnel resistance R_t has a lower limit of

$$R_t \gg e^2/h \tag{2.6}$$

which is called the weak coupling regime. For the vertical quantum dots used in this thesis this criterion is met.

Transport in gated transport spectroscopy occurs when the electrochemical potential of the dot $\mu(N)$ aligns with those of the source μ_S and drain μ_D. A source drain voltage $V_{SD} = (\mu_S - \mu_D)/(-e)$ opens a bias window, allowing electrons to tunnel from one reservoir to the other when $\mu(N)$ is located in it, meaning $\mu_S \geq \mu(N) \geq \mu_D$ for at least one value of N. If this condition is not satisfied, then no current flows through the dot and the number of electrons therein remains unchanged. This is known as Coulomb blockade. Varying V_G, $\mu(N)$ can be realigned with the bias window lifting the Coulomb blockade and enabling electron tunneling from source to drain. In the low-bias regime only one dot level is within the bias window and sweeping V_G generates a current trace I_{Dot} as schematically depicted in figure 2.1b. In contrast when the bias window is chosen such that multiple dot levels are situated therein the measurement takes place in the high-bias regime.

2.2 The II-VI material system

2.2.1 (Zn,Be,Cd,Mn)Se semiconductor alloy

The development, fabrication and investigation of vertical quantum dots performed during this thesis are done on multilayer heterostructures from the II-VI semiconductor material system (Zn,Be,Cd,Mn)Se. The sequence of layers in the heterostructure, which is depicted in figure 2.3 and described in detail later in this section, results in the formation of a II-VI resonant tunneling diode (RTD) [Chan 74]. The thin and abrupt tunnel barriers in such a heterostructure, which are weakly affected by a gating potential, provide already a well defined confinement along the growth direction (usually referred to as the z-direction). Furthermore the wide-gap II-VI semiconductor ZnSe ($E_g(4.2\text{ K}) = 2.82$ eV [Land 99]) acts as the base semiconductor for the entire heterostructure. In contrast to the III-V material system, used previously to fabricate vertical quantum dots, the incorporation of Mn atoms for inducing magnetic properties does not alter the doping of the material. In fact the detached electric and magnetic properties in the II-VI material system, which will be discussed later, allow tunability of doping and band structure useful for device optimization as well as investigation of spin related phenomena.

The ZnSe based multilayer heterostructures are typically grown on GaAs substrates, because there is only a small lattice mismatch of 0.27 % [Land 99] and they are readily available. Adding Be to ZnSe layers and creating the ternary alloy $Zn_xBe_{1-x}Se$ two effects can be achieved. First, its incorporation decreases the lattice constant of the layer, due to the smaller lattice constant of BeSe [Land 99]. This fact allows to reduce the elastic strain enabling a pseudomorphic growth of the device's heterostructure. Second, the tunability of the band gap [Asta 02, Chau 00], which comes from Be incorporation,

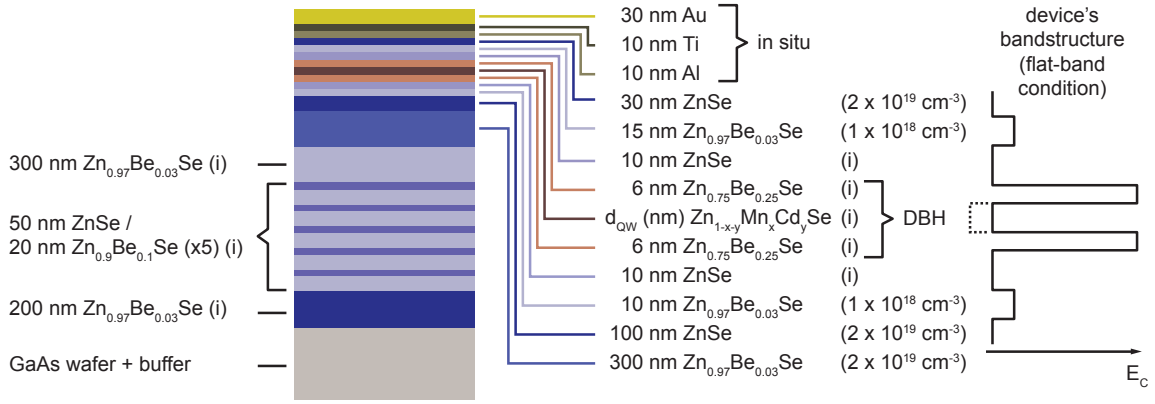

Fig. 2.3: The entire II-VI heterostructure layout built up from: the GaAs wafer, the superlattice, the RTD device and *in situ* metalization. (Right) Schematic, the RTD device bandstructure (in flat-band condition) indicating the band gap reduction when Cd is incorporated.

makes it a perfect fit for creating the tunnel barriers necessary for the resonant tunneling diode. This aspect also benefits from the fact that the increase in band gap energy at the type I heterointerface ZnSe/$Zn_xBe_{1-x}Se$ occurs predominantly in the conduction band [Kim 00, Koen 99]. The quantum well of the resonant tunneling device is formed from the diluted magnetic semiconductor $Zn_xMn_{1-x}Se$. Based on the results of Slobodskyy *et al.* [Slob 03] the Mn concentration is 8 % in all devices of this thesis. Quantum well II-VI RTD heterostructures grown by Slobodskyy *et al.* [Slob 03] and Frey *et al.* [Frey 10b] exhibit resonances above $U_{SD} = 100$ mV. In order to align the resonance with the Fermi energy in the leads, small amounts (up to 8 %) of Cd are alloyed into the QW. Since pure CdSe has a band gap of $E_g = 1.74$ eV [Lunz 96], which is smaller than E_g(ZnSe), Cd is an adequate candidate for fine tunning the band gap of the quantum well. Finally the electric conductivity through the device is achieved by appropriately n-doping the contact layers and the semiconductor leads to the DBH with iodine [Shib 88].

Figure 2.3 presents the entire II-VI heterostructure which was grown by Frey [Frey 12] using molecular beam epitaxy (MBE). This heterostructure, which consists of two main blocks, is grown on a standard epi-ready GaAs wafer, followed by a 180 nm undoped GaAs buffer layer. The first block of the heterostructure consists of a 200 nm thick highly doped ZnSe screening layer, followed by 7 periods of an undoped ZnSe / $Zn_{0.9}Be_{0.1}Se$ (50 nm / 20 nm) superlattice and a 300 nm thick undoped $Zn_{0.97}Be_{0.03}Se$ layer. This way the influence of electrical fields and charging from the polar III-V/II-VI interface[Frey 09, Farr 91, Frey 10a] is eliminated (see also chapter 3.1).

The second block represents the RTD heterostructure itself, which is based on the research done by Slobodskyy *et al.* [Slob 03]. Except for small variations in barrier width and height as well as QW composition and width, which required to be adjusted due to variation in growth conditions, the layer properties remained unchanged. Following the MBE growth, the first two layers of this block form the backside contact. The first one consists of a 300 nm thick $Zn_{0.97}Be_{0.03}Se$ (2×10^{19} cm^{-3}) doped layer and is matched to GaAs, preventing the addition of strain to the structure. The second layer of the two is a

100 nm thick ZnSe (2×10^{19} cm^{-3}) doped layer to minimize contact resistance [Miya 92]. 10 nm $Zn_{0.97}Be_{0.03}Se$ (1×10^{18} cm^{-3}) and 10 nm undoped ZnSe act as the source to the following DBH. The later is formed from 6 nm thick barriers of $Zn_{0.75}Be_{0.25}Se$ and a QW from $Zn_{1-x-y}Cd_yMn_xSe$ of different widths d_{QW}. Drain and top contact are then provided by 10 nm undoped ZnSe followed by 15 nm $Zn_{0.97}Be_{0.03}Se$ (1×10^{18} cm^{-3}) and 30 nm ZnSe (2×10^{19} cm^{-3}). The heterostructure is completed by in situ metal evaporation of Al / Ti / Au (10 nm / 10 nm / 30 nm), again to minimize contact resistance[Maxi 04].

2.2.2 Diluted magnetic semiconductor (Zn,Mn)Se

Diluted magnetic semiconductor stands for a semiconducting alloy formed from randomly substituting some of the host crystal's cations by magnetic ions, in this case Mn^{2+}. Unlike in (Ga,Mn)As, where Mn^{2+} is p-doping the III-V semiconductor through adding acceptor states, in II-VI semiconductors the isoelectric incorporation of the Mn^{2+}-ion does not change the crystal's electric properties. When Mn is built into the II-VI semiconductor crystal, i.e. the zincblende crystal of ZnSe, its two $4s$ electrons participate in the formation of the crystal bonds. The five d electrons of the half filled $3d$ orbitals are however localized and their spins are aligned in parallel, according to Hunds rules. The total spin S_{Mn} of the manganese atom is thus 5/2. These randomly distributed magnetic ions in the semiconductor crystal induce strong Zeeman splittings of electronic levels in an external magnetic field. This originates in an exchange interaction between the s/p band electrons, referring to the conduction/valence band respectively, and the d electrons from the Mn^{2+}-ions [Furd 87, Furd 88].

The magnetization M of the paramagnetic phase of a $A^{II}_{1-x}Mn_xB^{VI}$ DMS in the very dilute limit ($x < 0.01$) can approximately be expressed by the formula

$$M = xN_0 g\mu_B S B_S(g\mu_B SH/(k_B T)) \tag{2.7}$$

where x is the magnetic ion mole fraction, N_0 is the number of cations per unite volume, H represents the applied field, B_S is the standard Brillouin function, g stands for the electron g-factor, T denotes the temperature and S is the manganese spin. For arbitrary values of x and T however the analytical expression from above is no longer valid. Gaj *et al.* [Gaj 79] observed a similar qualitative correlation of the magnetisation M vs. H and the Brillouin funtion. This purely empirical finding replaces x and T by effective values x_{eff} and $T_{eff} = T - T_0$ in the magnetisation M

$$M = x_{eff} N_0 g\mu_B S B_S \left(\frac{g\mu_B SH}{(k_B(T - T_0))} \right) \tag{2.8}$$

where x_{eff} and T_0 are fitting parameters and can be tabulated for each family of DMS. The reduced mole fraction of active Mn^{2+}-ions, accounted for by x_{eff}, is based on the Mn^{2+}-Mn^{2+} antiferromagnetic interaction of a small fraction of ions which form clusters with a zero net magnetic moment [Shap 84]. Hence, the energy of up or down electron spin levels in the conduction band, based on the s-d-interaction, is given by [Gaj 79, Twar 83, Twar 84]

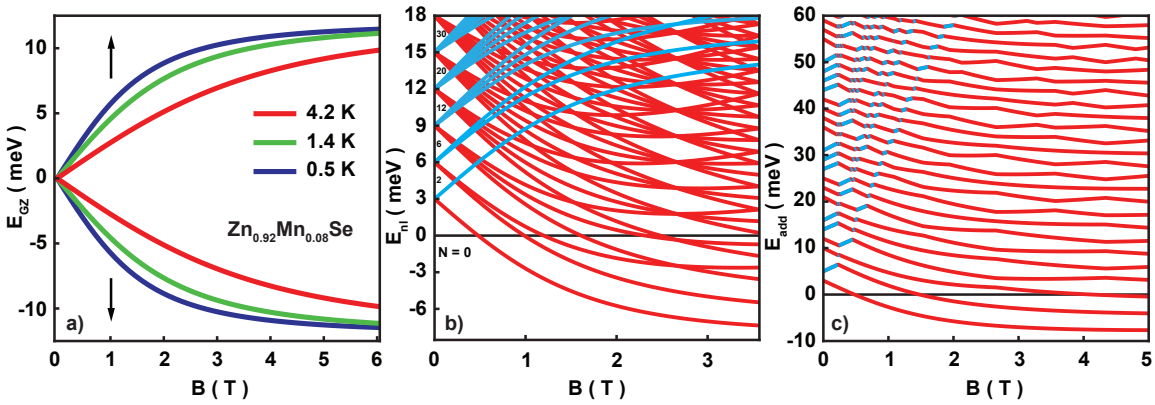

Fig. 2.4: a) Giant Zeeman energy of the electronic spin-up and spin-down levels in a $Zn_{0.92}Mn_{0.08}Se$ layer at different temperatures. b) Calculated Fock-Darwin spectrum from figure 2.2 for a $Zn_{0.92}Mn_{0.08}Se$ quantum dot supplemented with the Giant Zeeman splitting between spin-up (blue) and spin-down (red) electrons. c) The addition energy E_{add} of this system, given by equation 2.4, using a fixed charging energy $E_C = 2$ meV.

$$E_{GZ\uparrow,\downarrow} = \pm\frac{1}{2}N_0\alpha x S_{eff} B_S \left(\frac{g\mu_B SH}{(k_B(T-T_0))}\right) \tag{2.9}$$

and the total energy splitting reads

$$\Delta E_{GZ} = N_0\alpha x S_{eff} B_S \left(\frac{g\mu_B SH}{(k_B(T-T_0))}\right) \tag{2.10}$$

where $N_0\alpha$ is the material dependent exchange integral for the *s*-*d*-interaction and S_{eff} (with $S_{eff} < S_{Mn}$) stands for an effective spin at a given manganese concentration x alloyed with the semiconductor. For (Zn,Mn)Se Twardowski *et al.* [Twar 83, Twar 84] determined $N_0\alpha = 0.26$ eV. Keller [Kell 04] measured $S_{eff} = 1.13$ and $T_0 = 2.35$ K for a manganese concentration of 8%, similar to the concentration used in the QWs of the samples processed in this thesis. Figure 2.4a displays a calculated spin-splitting of the conduction band edge at different temperatures for $Zn_{0.92}Mn_{0.08}Se$ from the formula and values for $N_0\alpha$, S_{eff} and T_0 mentioned above.

As mentioned in section 2.1, for the QDots made out of a III-V semiconductor the consideration of Zeeman spin-splitting within the Fock-Darwin spectrum is neglected. This however is no longer valid for the Giant Zeeman splitting in a II-VI DMS, where the energetic splitting is equal or higher than the energy spacing from a 3D confinement. The Fock-Darwin single-particle energy spectrum of a DMS QDot is then given by

$$E_{n,l,\uparrow,\downarrow} = (2n+|l|+1)\hbar\sqrt{\frac{1}{4}\omega_c^2+\omega_0^2} - \frac{1}{2}l\hbar\omega_c \pm \frac{1}{2}N_0\alpha x S_{eff} B_S \left(\frac{g\mu_B SH}{(k_B(T-T_0))}\right) \tag{2.11}$$

where the first and second term are the spin independent single-particle energy spectrum and the third term introduces the Giant-Zeeman spin splitting. Figure 2.4b displays how

the spin-independent Fock-Darwin spectrum, previously shown in figure 2.2, is affected by the spin splitting in a magnetic artificial atom, when a magnetic field is applied. The measureable addition energy of the magnetic QDot is depicted in figure 2.4c, when a charging energy of $E_c = 2$ meV is added to each level of $E_{n,l}$.

2.3 Quantum well energy adjustment

The investigation of electronic and magnetic properties of vQDots is best performed in the linear transport regime. This means the current through the sample is determined while a small source-drain voltage U_{SD} is applied. In order to do so it is necessary that the QDot's energy levels are as close as possible to the Fermi energy of the leads. This way by applying a gate voltage these levels, which are typically separated by a few meV, can easily be located inside a small bias window.

These QDot energy levels originate from confining the electron wave in the x, y and z spacial direction. The z-confinement is given by the QW's thickness of a few nm and results in energetic spacings ΔE_z from many tens of meV to over hundred. However, the 2D confinement in x-y-direction arises from the lateral miniaturization when etching the pillar to form the vQDot. Thereby the E_{xy}-degeneracy of each QW's E_z energy state is lifted. Due to the pillar's lateral dimensions of a few-hundred nm the energetic spacings ΔE_{xy} result in gaps of some meV. Since only a small fraction of the QW's total energy spectrum is accessible by the gate voltage, the electronic investigations are concentrating on the E_{xy} quantization for a fixed E_z. Therefore, the mentioned requirement for linear transport is achieved when a E_z energy level of the two dimensional QW, preferably the QW's ground state, is already situated near the Fermi level of the contacts. This requirement however is not met at the starting point of the development of vQDots from the II-VI semiconductor RTD-structure.

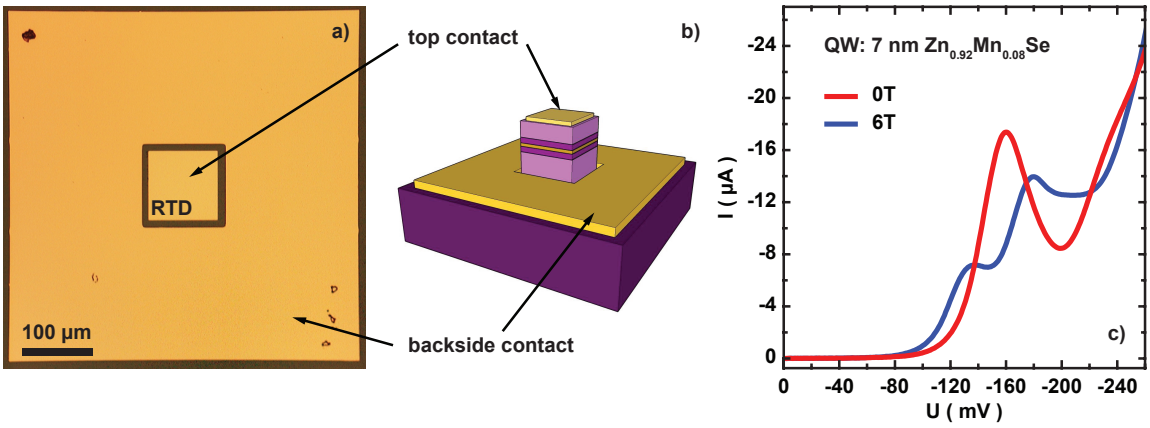

Fig. 2.5: a) Optical image of a 100^2 μm^2 QW RTD device used for characterization. b) Schematic side view of the QW RTD device. c) I-U curves at $B = 0$ T and 6 T from a 100^2 μm^2 RTD device with a 7 nm $Zn_{0.92}Mn_{0.08}Se$ quantum well showing the Giant-Zeeman splitting of the resonance.

As mentioned earlier the entire RTD-device is based on the heterostructure developed by Slobodskyy *et al.* [Slob 03] combined with the insulating superlattice described by Frey *et al.* [Frey 09]. However, the MBE growth necessary for all the samples presented in this work is performed by A. Frey and described in detail in his PhD thesis [Frey 12]. Also a detailed model of the electronic transport in the RTDs QW from the II-VI DMS is presented in the PhD thesis of Rüth [Ruth 11a]. At the starting point [Frey 10b], the RTD's DBH is typically formed from 6 nm $Zn_{0.75}Be_{0.25}Se$ / 7 nm $Zn_{0.92}Mn_{0.08}Se$ / 6 nm $Zn_{0.75}Be_{0.25}Se$. The grown heterostructures are electrically characterized by first fabricating 100^2 μm^2, 120^2 μm^2, 150^2 μm^2 square pillars through optical lithography, Ti/Au/Ti metal mask evaporation and chemical assisted ion beam etching (CAIBE) down to the backside layer. Each pillar is surrounded by a 500^2 μm^2 square shaped backside contact-ring, fabricated by optical lithography, electron beam evaporation of Ti/Au and lift-off. Figure 2.5a shows a top view of a 100^2 μm^2 characterization RTD-device and a sketched side view is displayed by figure 2.5b. Figure 2.5c shows characteristic 2-terminal I-U-curves of a 100^2 μm^2 device at B = 0 T and 6 T. The voltage U_{res} = (-161 ± 1) mV indicates at which source drain voltage the first QW-level is in resonance with the Fermi energy in the top contact. This value lies within the range of -155 mV to -165 mV, given by the growth to growth variations. A similar observation is true for the peak-to-valley-ratio (PVR) of 1.92, which is in this case at the top end of the 1 to 2.2 range in the II-VI RTDs. From the position of the LO-phonon resonance [Gold 87] at U_{LO} = (-232 ± 1) mV and the known LO-phonon energy in ZnSe E_{LO} = 31.7 meV [Land 99] the lever factor, which connects the difference in voltage to the energetic spacing, is found to be λ = (2.24 ± 0.06) mV/meV. The spacing of the two resonances at $U_{res,1}$ = (-137 ± 1) mV and $U_{res,2}$ = (-180 ± 1) mV in the 6 T curve gives a Giant-Zeeman energetic spacing of the spin-up and spin-down level in the QW of ΔE_{GZ} = (19 ± 2) meV, taking into account the aforementioned lever factor λ. This corresponds well with the expected energetic splitting of ΔE_{GZ} = 19.6 meV, given by the empirical equation 2.10. The described behavior is typical for the grown RTDs with a $Zn_{0.92}Mn_{0.08}Se$ and confirms that the expected QW's magnetic properties are preserved.

However the first resonance, denoted by the voltage position of the resonance peak, of these QW RTDs is well above the Fermi energy in the leads. It is broader than expected from tunneling theory, because of QW width fluctuation as described by the model of Rüth [Ruth 11a]. Furthermore, the read-out U_{res}-values from the I-U-curves agree well with the determined positions of the maxima of the second derivative dI^2/dU^2, as proposed by Smith *et al.* [Smit 96] and Yoh *et al.* [Yoh 98]. The later is helpful, when extremely broad resonant peaks, i.e. the LO-phonon peak, are investigated. Finally is has to be pointed out that there is an observable asymmetry between the voltages at which the resonances are observed in positive and negative source drain bias (not explicitly shown here). The reason for the difference may well be in growth related issues as there are the segregation of alloys at interfaces of different layers and small variations in the layers surrounding the DBH [Frey 12]. With these facts established this QW DBH has to be modified such, that the Fermi level of the QW aligns with the Fermi energy in the leads, allowing to perform measurements in the linear response regime. For this purpose two

possibilities for lowering the energy level present: increasing of the QW width or forming a QW from an alloy with a smaller band gap. The investigation of this options, which led to the optimal QW for the magnetic QDots, is presented in the following.

2.3.1 Width variation

In order to investigate how changes in the DBH's conduction band profile, presented in figure 2.6a, affect its electronic properties, one has to look into how these changes are connected to the physical properties. Neglecting any contributions from the contacts and just considering a DBH plus its adjacent leads the passing current is given by the formula

$$J \propto \int T(E) D_S(E) D_D(E+eU)(f_S(E) - f_D(E+eU))dE \tag{2.12}$$

where $D_S(E)$ and $D_D(E+eU)$ are the density of states and $f_S(E)$ and $f_D(E+eU)$ denote the Fermi distributions in the source and drain, accounting for an applied bias voltage U. $T(E)$ is the transmission probability through the DBH and is given by the physical characteristics of the DBH. Using the transfer matrix method as described in [Mizu 95, Leps 97] the transmission probability $T(E)$ can be expressed

$$T(E) = \frac{m_D^* k_D}{m_S^* k_S} \frac{1}{|M_{11}^{tot}|^2} \tag{2.13}$$

where m_D^* and m_S^* are the effective masses and k_D and k_S are the electron wavenumbers in the source and drain. M_{11}^{tot} is the (11)-element of the total transfer matrix formed from the transfer matrices at each DBH's interface. Figure 2.6b presents qualitatively the $T(E)$ for a flat band DBH with a barrier height of 400 eV from $Zn_{0.75}Be_{0.25}Se$ and

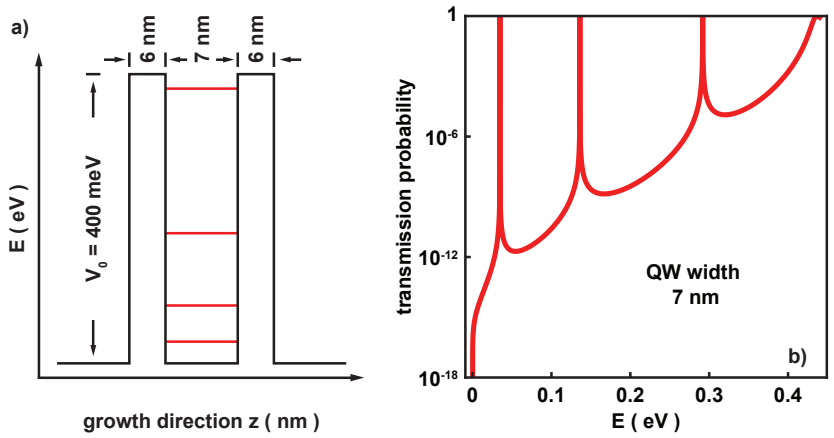

Fig. 2.6: a) Schematic of the conduction band profile in growth direction under flat-band condition. Two 6 nm thick $Zn_{0.75}Be_{0.25}Se$ layers forming the tunnel barriers confine a 7 nm thick $Zn_{0.92}Mn_{0.08}Se$ quantum well. b) The arising discrete energy states inside the quantum well result in peaks of unity in the calculated transmission probability as a function of the incident electron energy.

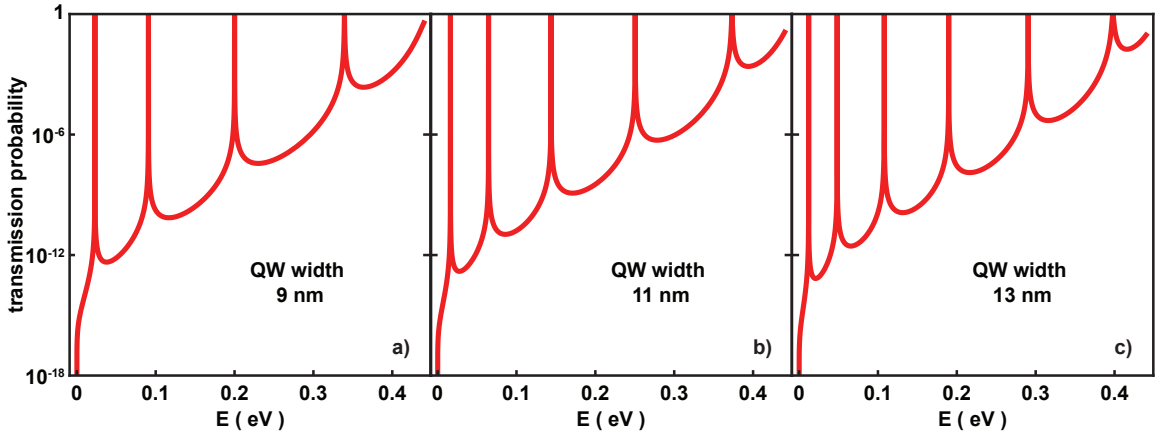

Fig. 2.7: Calculated transmission probability for the double barrier heterostructure in figure 2.6 with varying quantum well thicknesses of a) 9 nm, b) 11 nm and c) 13 nm showing the decrease of the energetic position of the first resonance towards lower energies as the quantum well thickness is increased.

6 nm thickness as well as a 7 nm wide ZnSe QW. Moreover, for all segments of the energy potential a constant effective mass $m^* = 0.145\ m_e$ is assumed. The difference between the aforementioned resonance U_{res} and the one of the simulation is based on the simplicity of the model which lacks further device parameters. A detailed treatment on this problem is presented by [Ruth 11a] and is beyond the scope of this thesis.

A first strategy to approach the resonance to the Fermi energy of the contacts, meaning to move U_{res} towards 0 V, consists in varying the width of the QW. As it is observable from the transmission probability $T(E)$ for QWs of 9 nm, 11 nm and 13 nm, depicted in figure 2.7, the first resonance is shifting towards lower energies. This means the QW's ground energy is lowered towards the conduction band edge and with all other parameters remaining unchanged its distance to the Fermi level is reduced. This simple picture suggests a valid possibility to achieve the intended linear transport regime in the RTD device.

Figure 2.8 presents I-U measurements from standard $100^2\ \mu m^2$ RTD devices where the QW are 9 nm, 11 nm and 13 nm. As expected the resonance moves to lower bias voltages as a function of the QW width and goes down as far as $U_{res} = 100$ mV for a 13 nm QW. This shift is accompanied by a broadening of the resonance as well as a drop of the PVR down to 1, reducing the observation of a clear resonance peak. Additionally, since the decrease in U_{res} by doubling the QW width does not shift the resonance significantly near zero bias voltage, this path proves to be not suitable for the intended objective and is not further pursued.

2.3.2 Bandgap variation

The second possible approach is based on reducing the energy gap of the semiconductor alloy in the QW. By this means, the conduction band bottom is lowered and therefore all

energy levels of the QW are also shifted to lower energies. With that said this method offers the possibility to align the ground state of the QW with the contacts' Fermi energy. However, the energetic spacings of the levels within the QW, which are given by the QW width, remain unaffected by this modification.

Similar to the creation of the barriers in the conduction band, this modification is easily achieved by incorporating Cd into the QW. Since the CdSe bandgap is 1.74 eV at 4.2K, alloying Cd into the (Zn,Mn)Se offers a possibility to lower the QW conduction band edge. Because the bandgap of $Zn_{1-x}Mn_xSe$ following Astakhov *et al.* [Asta 02] findings is given by

$$E_g(x) = 2.82 - 0.145x + 4.073x^2 \tag{2.14}$$

for 8% of manganese the resulting energy gap of 2.83 eV is similar to the one of pure ZnSe. Hence the bandgap variation when Cd is incorporated into the QW can be expressed in terms of a $Zn_xCd_{1-x}Se$ alloy. According to Lunz *et al.* [Lunz 96] the change of the energy gap is given by

$$E_g(x,T) = E_g(0,T)(1-x) + E_g(1,T)x - ax(1-x) \tag{2.15}$$

where $E_g(0,T)$ and $E_g(1,T)$ denote the bandgaps of CdSe and ZnSe at a given temperature T and a includes the deviation from linearity.

Figure 2.9 displays I-U curves of standard 100^2 μm^2 RTD devices with varying Cd concentrations in the 7 nm wide QW of 2.9%, 5.9% and 7.6%. The measurements clearly show that the resonance is shifting towards zero bias and reaches the linear transport regime at a Cd concentration of 7.6%. This behavior indicates that the ground energy state in the QW is finally situated near the contacts' Fermi energy, facilitating electronic transport when a small source drain bias voltage is applied. The observation of a single resonance moving to higher energies when a magnetic field is applied, as shown by figure

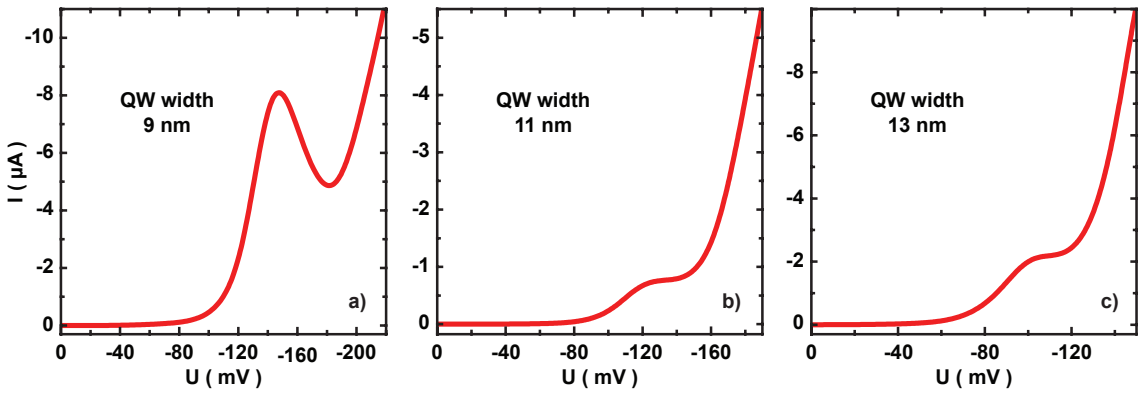

Fig. 2.8: I-U curves of 100^2 μm^2 RTD devices with varying $Zn_{0.92}Mn_{0.08}Se$ quantum well thicknesses of a) 9 nm, b) 11 nm and c) 13 nm showing the decrease of the energetic position of the first resonance towards lower energies as the quantum well thickness is increased, as expected from figure 2.7. The alignment of the first resonance with the Fermi energy in the contacts is not achieved this way.

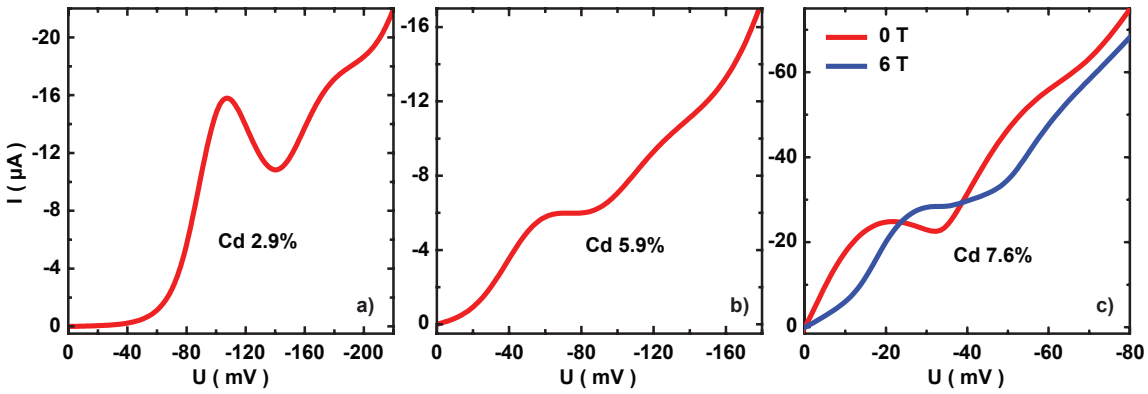

Fig. 2.9: I-U curves of 100^2 μm^2 RTD devices with a 7 nm thick $Zn_{0.92-x}Mn_{0.08}Cd_xSe$ quantum well and a varying Cd incorporation of a) 2.9%, b) 5.9% and c) 7.6% showing the decrease of the energetic position of the first resonance towards lower energies as the Cd incorporation is increased. This way the alignment of the first resonance with the Fermi energy in the contacts is achieved.

2.9c, supports this interpretation. Since the downwards moving resonance remains below the Fermi energy, it can't be accessed in transport measurements. Furthermore the still existent PVR > 1 enables the reliable observation of the resonance peak, indicating a good confinement of the electron wave in the QW. A similar approach is also found in the final DBH from the III-V material system. Here the best results have been achieved by lowering the conduction band bottom using a $In_{0.05}Ga_{0.95}As$ alloy through incorporation of In [Taru 96].

Having established an appropriate II-VI RTD heterostructure for the linear transport regime, as presented in figure 2.3, a fabrication method of gated vQDots from this semiconductor material is developed in this thesis.

Chapter 3

Contacting

The miniaturization of the RTD structure towards sub micrometer pillars is faced with new challenges in contacting the future three terminal device. In the following two issues and their solutions towards proper contacting are described. First, for all devices to be fabricated from the II-VI material system a simple and reliable contact separation has to be provided ensuring a current path solely through the device. In order to achieve this and given the starting material a suitable and reliable process step needs to be developed. Second, the few hundred nanometer wide pillar mesas, forming the vQDots, require proper contacting of their top. In this context the idea of metal capped insulating semiconductor line mesas [Aust 97] as an alternative top contacting method for sub micrometer pillars is investigated for our material system in terms of fabrication and conductivity, while being miniaturized. In addition to this the established air bridge technique [Borz 04], proving to be essential later in the vQDot fabrication process, is adjusted such that the device's non-planar surface can be accurately spanned.

3.1 Contact separation

The state of the art vQDots based on a RTD heterostructure are fabricated from the III-V material system [Kouw 01, Kita 07b]. Here high quality III-V wafers for MBE growth allow the utilization of the wafer backside as an electrical contact of the device. Unlike in the III-V material system there is no adequate II-VI wafer for MBE growth of the RTD structure used in this thesis. Due to the 0.27% lattice mismatch of ZnSe compared to GaAs [Oleg 87], the (Zn,Cd,Be,Mn)Se heterostructure is grown on a epi-ready GaAs wafer. Thereby a polar II-VI/III-V interface, caused by the different electron affinities of ZnSe and GaAs, is developed leading to the formation of electric fields and charging in the II-VI heterostructure [Farr 91, Frey 09]. The investigation of the n-ZnSe/GaAs heterointerface by Frey *et al.* revealed a depletion zone of 60 – 110 nm in the highly doped ZnSe-layer attributed mainly to the interdiffusion of atoms across the II-VI/III-V interface. As a result of this study a pseudomorphic II-VI buffer consisting of 200 nm of highly doped $(Zn_{0.97}Be_{0.03})Se$ ($10^{19}cm^{-3}$), followed by five undoped periods of 50 nm ZnSe/20 nm $(Zn_{0.9}Be_{0.1})Se$ and terminated by 300 nm of undoped $(Zn_{0.97}Be_{0.03})Se$ has

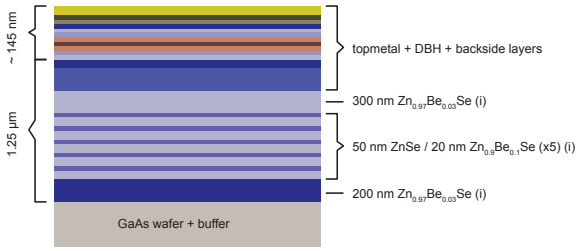

Fig. 3.1: The II-VI layer structure shows the composition of the superlattice and the dimensions of the different heterostructure segments.

been developed to eliminate the influence of electrical fields as well as charging from the pollar III-V/II-VI interface and screen away the interface effects from the relevant layers of the device. Figure 3.1 shows the II-VI heterostructure used in this thesis to fabricate vQDots which is built from the GaAs wafer, the detailed multilayer buffer and the DBH presented in chapter 2.2.

Given the layer configuration of the heterostructure two characteristics for future devices are included. First, as mentioned, compared with state of the art III-V vQDots the wafer backside is not usable for contacting, e.g. forming the source of the device [Taru 95]. Thus the corresponding contact has to be placed laterally on the highly doped ZnSe ($2 \times 10^{19}\mathrm{cm}^{-3}$) backside layer on top of the multilayer buffer. Second, the areas, comprising the bonding pads for the top contact and gate, have to be properly isolated against this highly doped ZnSe backside layer. Any electrical contact to this layer outside the pillar creates an additional path for electrons in parallel influencing any effect to be investigated. The isolation can be done either by deposition of insulator or by separating the different bonding regions by trenches. Due to the low height of the RTD heterostructure ($\sim$ 145 nm from the top of the backside layer) and the thin injector regions (20nm at the bottom and 25 nm at the top) only thin insulator layers can be deposited which can be easily damaged during the bonding process and thus causing unwanted shorts. The separation of the bonding areas by interrupting the backside layer however promises to be a better approach to avoid parallel conducting paths.

Considering the results of Frey *et. al* for the vertical transport through the multilayer buffer, also confirmed by own tests, separating the bonding pad areas down to the insulating GaAs buffer proves to yield a resistance $\gg$ 1 GΩ at 4.2 K in the + 200 mV to - 200 mV voltage range. Since in some test wafers it has been observed that the II-VI superlattice exhibited resistances in the range of some MΩ instead of several hundred MΩ, an etch stop in the multilayer buffer is insufficient. Under the consideration that sub micrometer pillars are expected to exhibit resistances $>$ 100 MΩ an eventually non insulating superlattice causes electrical shorting. Therefore the separation of the bonding areas has to be etched down to the III-V buffer layer in order to guaranty full electrical insulation.

Given the II-VI heterostructure (fig.3.1) the depth of these disconnecting trenches needs to be $>$ 1.3 μm, measured from the *in situ* deposited top contact metal. However, the width of the notches depends on their position within the device structure. In the

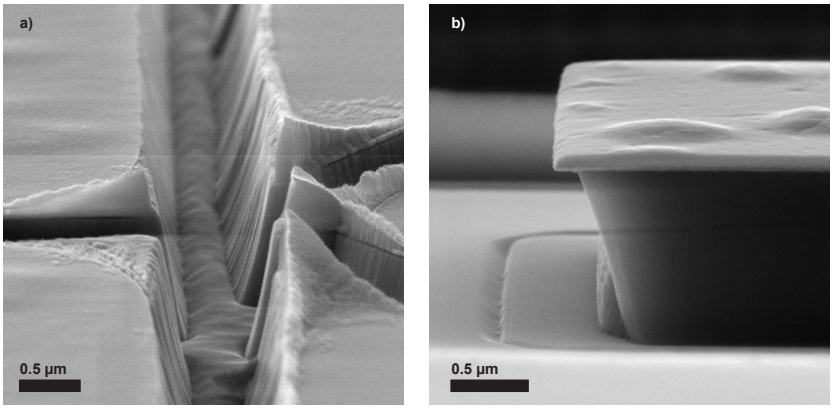

Fig. 3.2: SEM micrographs display different deep features being fabricated by a) dry etching and b) wet etching after a first dry etching step.

area near the pillar the width has to be about 1 μm, whereas at the bonding pads 5 μm wide ditches can be used. To carve these notches into the heterostructure either a dry etching method or wet etching is applicable. Due to its anisotropic character dry etching facilitates optimal pattern transfer with minimal lateral influence in pattern dimension (fig.3.2a). By contrast, the isotropy of wet etching in the II-VI heterostructure is unsuitable for the trenches near the pillar, where the width and depth have similar dimensions (fig.3.2b). In order to fabricate trenches the corresponding pattern has to be defined in a masking material, which has to satisfy the following requirements. First, the erosion of the mask should be minimal vertically and laterally entailing the use of masking materials with etching rates much smaller than the material to be removed. Second after finishing the etching process the mask has to be removable without leaving behind any residue influencing later processing steps or device functionality. Finally, the methods of removing the mask should not affect adversely the original material by etching or chemically alterating. Thus commonly used masking materials for dry etching of deep features are resists, dielectrics and metals.

Based on the process for micrometer size RTDs presented by Borzenko *et al.* [Borz 05], requiring EBL, the trenches are fabricated by apply a PMMA positive resist mask. A sketch in figure 3.3a illustrates briefly the main process steps. The etching rate of the PMMA resist 950K (5%) for the CAIBE dry etching process of the ZnSe heterostructure is 11 nm/min over 70 nm/min for the semiconductor. Its thickness of about 480 nm when spun at 5000 rpm ensures the protection of the covered surface during the total etching time of about 18 min. Figure 3.3b and c show the PMMA masks for the two steps in etching trenches for micrometer sized RTDs following the recipe of T. Borzenko [Borz 05]. The quick and easy manufacturing of the necessary deep notches makes the fabrication step interesting for later testing structures as shown by figure 3.3d.

However, the disadvantages of this fabrication step evolve during the work on different testing and characterization devices which results in abandoning the resist mask for deep feature etching and developing a processing step for trenches utilizing Ti metal as a

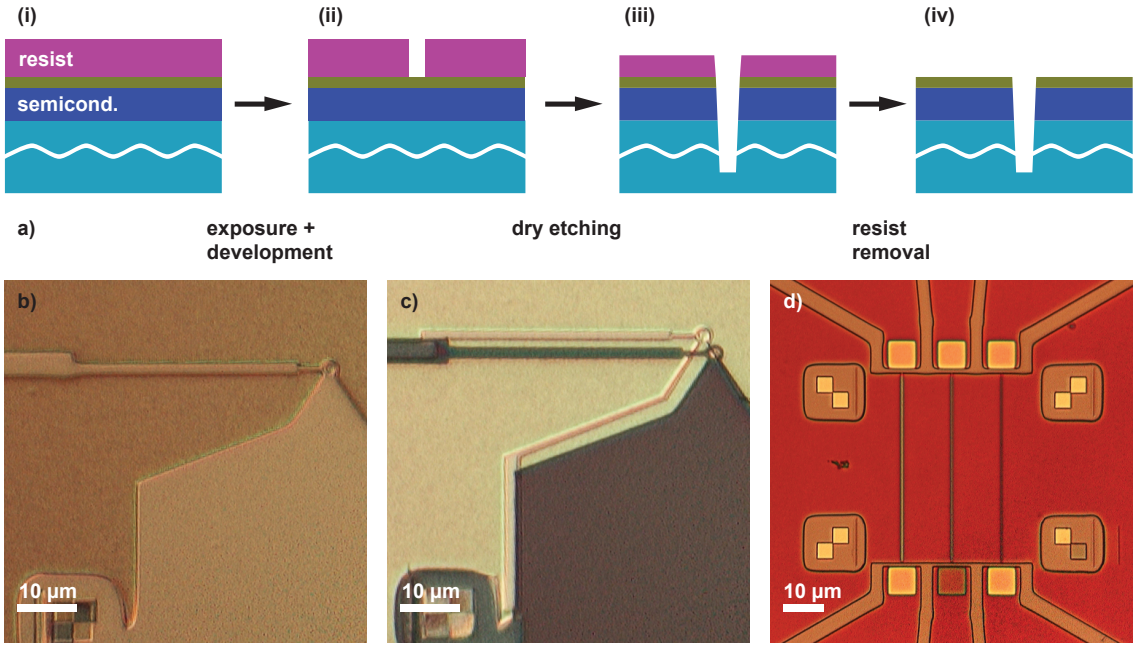

Fig. 3.3: a) A brief sketch showing a dry etching process using a positive resist mask. Optical images displaying the PMMA resist masks used in the b) 1st and c) 2nd fabrication step (mask shifted due to misalignment) following Ref. [Borz 05]. d) The red colored area is the resist mask used for dry etching the trenches in line mesa testing structures.

masking material. One downside of the PMMA mask arises from the difference in the heterostructure to be etched in comparison to the layer stack used in the first place by Borzenko *et al.* [Borz 05], which lacks the II-VI superlattice but has instead just a 300 nm thick high doped ZnSe (10^{19}cm^{-3}) layer. The increasing distance between the backside layer and the insulating III-V buffer necessitates a longer total etching time leading to an extended exposure of the resist mask to Ar ion bombardment and BCl_3 radicals. The sustained ion bombardment hardens the resist surface impeding an easy removal by stripping chemicals and thus requiring heating and usage of continuous ultra sonic agitation. Figure3.4a depicts the junction between a bridge post and its corresponding metal pad in a test sample for line mesas, being described later in this chapter. The residue from the deep feature etching step is still well observable on the metal surface at the end of the fabrication process. This fact is also confirmed by figures 3.4b – 3.4d recorded after a bridge, connecting a line mesa to its contact pad for bonding, has been accidentally riped off. For clarification, the actual bonding pad at the left most end, displayed in figure 3.4d, has been evaporated after the dry etching steps. The SEM images recorded with the secondary electron detector indicate the existence of an additional layer on the etched structures. In lens detector images of the same area show that these uncovered areas of gold have the same contrast as the bonding pads and bridges evaporated from gold added after the dry etching step. Thus the darkening of the bridge contact pad and the line mesa is attributed to the contamination by the previous deep feature etching step. Considering the fact that many of the samples containing a PMMA etching mask

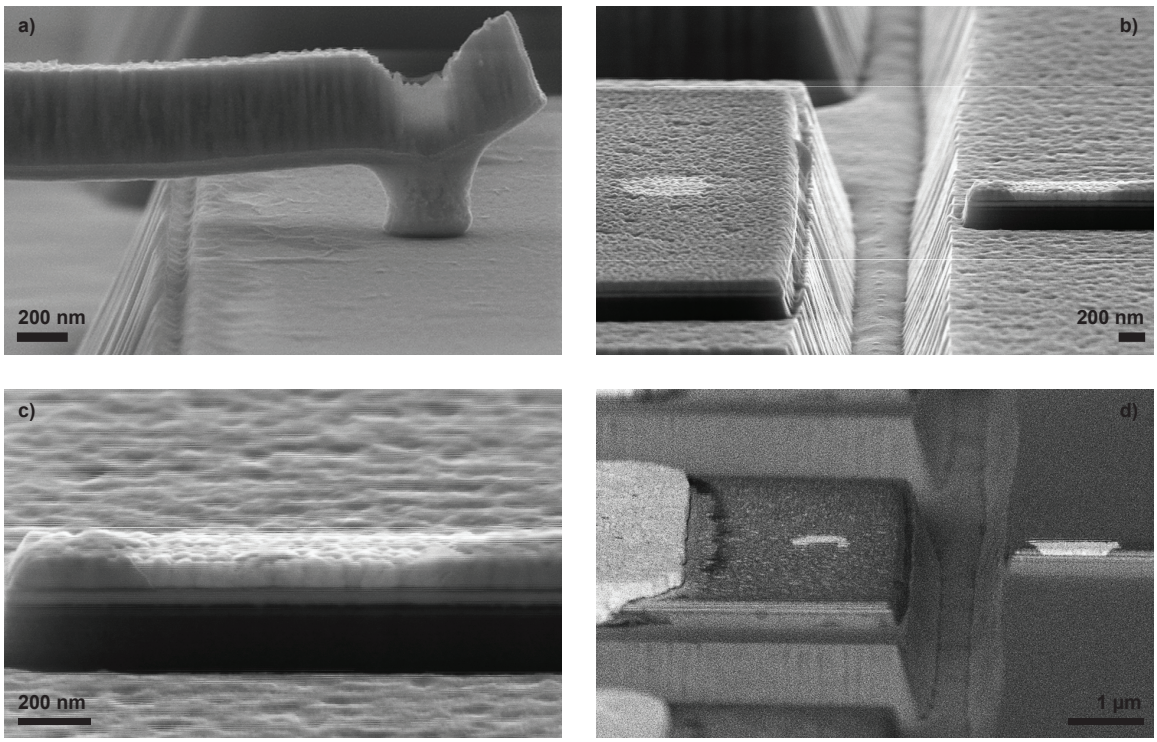

Fig. 3.4: a) SEM micrograph displaying resist residue at the junction of the pillar post and the bonding contact. Images of a lines mesa and the bonding contact after air-bridge removal recorded in b) and c) secondary electron as well as d) in-lens detection mode display the pollution of the top metal surface.

for deep trenches have exhibited diodic I-U characteristics or haven't worked at all when measuring only along the line's top contact metal, emphasizes the unreliability of this fabrication technique for deep notches.

Additionally the resist mask can accumulate BCl_3 radicals during the extended etching time also affecting especially the Al in the *in situ* metal contact of structures. The BCl_3 radicals interact with water molecules from the humidity in the cleanroom environment by forming a highly concentrated hydrochloric acid oxidizing the non-noble metal aluminum and generating gaseous hydrogen. The optical image in figure 3.5a recorded from some testing micrometer sized RTD devices after dry etching in CAIBE exhibit the described reaction. In course of the fabrication process the observed 'bubbles' collapse reinforcing the undercutting assumption by confirming that they are not a change in the PMMA resist but modification in the structure's material.(fig.3.5b) The SEM side view image of an undercut edge displayed in figure 3.5c shows clearly the *in situ* metal detaching from the semiconductor. However the described interaction has been observed very irregularly through the identically fabricated test samples and thus is expected to be related to the *in situ* metal evaporation after MBE growth, but to this point a clear reason could not be identified.

A third disadvantage in using PMMA as an etching mask for deep features arises from the redeposition taking place at the sidewalls of the resist. These redeposition sidewalls,

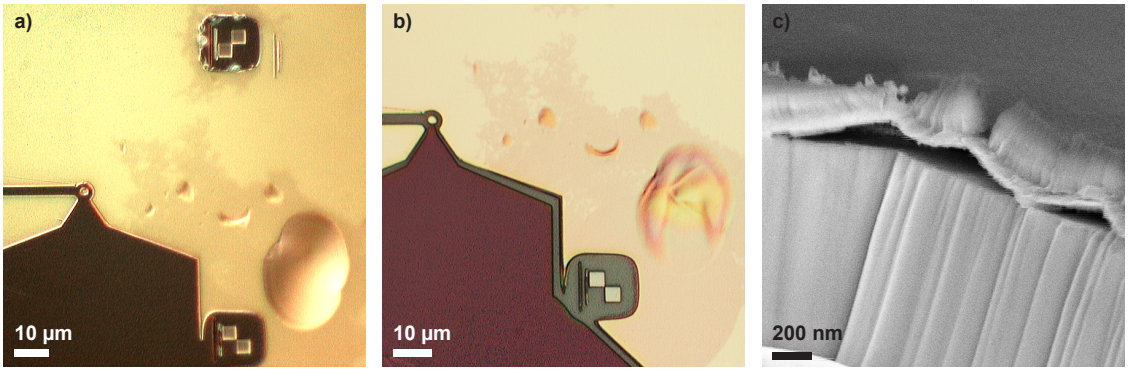

Fig. 3.5: a) Emerging 'bubbles' from under etching and b) collapsed ones after the sample has been dry etched in CAIBE using BCl_3. c) SEM mircrograph displays the detachment of the under etched *in situ* metal.

which appeared after the deep feature dry etching, are displayed in figure 3.6 for different samples. Their adhesion to the sample surface and disorder after resist removal involves the risk of connecting adjacent contacts, causing shorting and thus critically influencing the device functionality.

In order to avoid the described downsides of the PMMA resist mask the application of a metal mask for the fabrication of the 1.3 μm trenches is considered. For the III-V material system Lothian *et al.* [Loth 92] conclude from their experiments on the erosion of different masking materials during dry etching of deep features that metal based dry etching masks are more robust in terms of erosion in comparison to resist or dielectric layers. From their findings they also infer that masking metal layers are thus more favorable for dry etching deep features than resist or dielectric masks. One easily accessible metal suitable for masking proves to be titanium. In the 1970s research reports on dry etching by Krumme *et al.* [Krum 73] and Somekh [Some 76] showed that titanium has a low etching rate for ion beam milling and is almost independent on the angle of incidence. Additionally Krumme *et al.* reported on the suitability of Ti for fabricating 5 μm deep grooves in garnet.

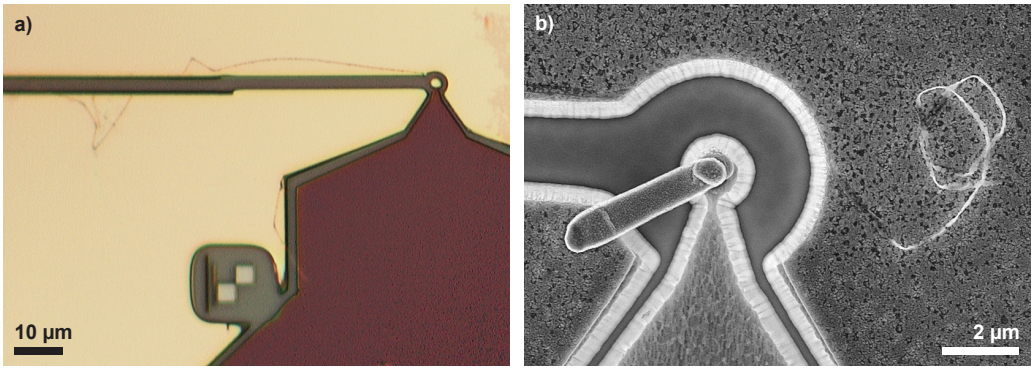

Fig. 3.6: Residue sidewalls from deep feature etching with a PMMA resist mask emerge a) along trenches and b) in the proximity of pillars.

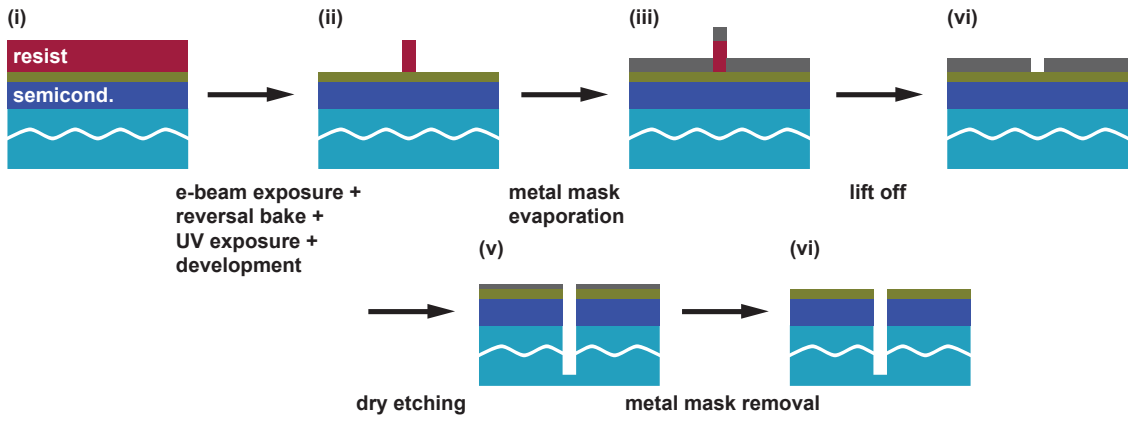

Fig. 3.7: A brief sketch of the process using a negative resist mask from ARU4060 to define the subsequent metal mask required for the dry etching step of deep features.

The quite low Ti etching rate of 5 nm/min with respect to a high rate of 70 nm/min for removing the II-VI ZnSe based semiconductor using the BCl_3 based CAIBE process makes this metal also interesting for deep feature etching in the given heterostructure.

Applying the Ti metal mask overcomes the previously for the PMMA resist mask listed disadvantages. Despite the long etching time of 18 min the removal of excess Ti mask after this process step by diluted HF is not influenced. At the same time the sample surface left behind after mask removal does not suffer from any residue. Further any accumulation of BCl_3 radicals is hindered suppressing any etching reaction of the Al in the top contact metal. In contrast to a resist mask where its height is given by the speed and time of rotation at spinning, the thickness of the evaporated metal layer can be precisely tailored and thus much thinner. Furthermore the use of a thin metal mask and its erosion to a layer of few nanometers at the end of the etching process inhibits the creation of redeposition sidewalls entailing the risk of shortening adjacent contacts.

The dry etching metal mask consists of a metal layer of a definite thickness with gaps where the trenches are to be. In order to achieve this design a negative process is used, by exposing the future trenches applying electron beam lithography to a image reversal resist. By the following reversal bake the exposed areas are crosslinked and hence insoluble by the developer whereas the unexposed regions remain unaffected. The later are then made soluble by a flood exposure with UV-light and removed by the subsequent developing step leaving behind the crosslinked pattern on the sample surface. This resist pattern is then used as a mask during the metal evaporation and removed by a lift off process in acetone and low power ultrasonic agitation converting the exposed negative resist pattern of the trenches into a positive metal mask with openings at the same spots. The described process is sketched in figure 3.7. Figure 3.8a also shows the steep profile of the resist after image reversal and prior to metal evaporation emphasizing the adequacy of this process step for establishing the desired gaps in the metal mask. The resist pattern after development and the final dry etching mask during devices fabrication are shown in figures 3.8b and 3.8c.

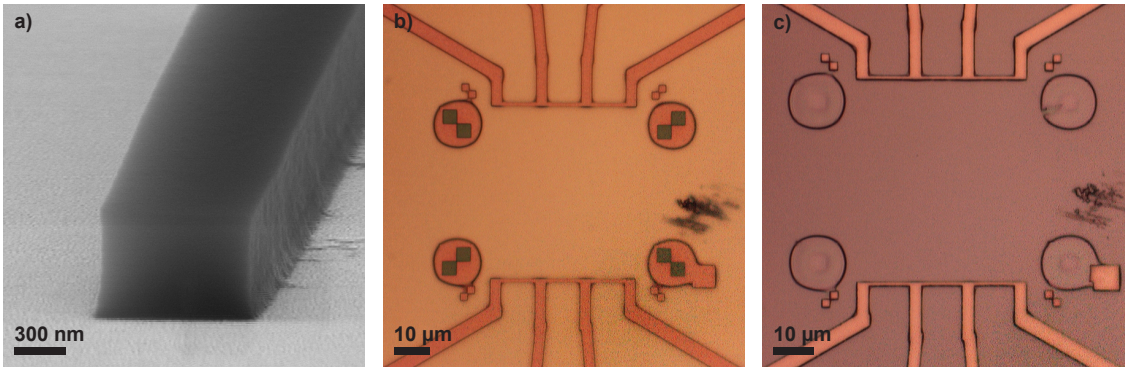

Fig. 3.8: a) SEM micrograph showing the profile of the ARU4060 resist used as a negative resist mask for the subsequent metal mask fabrication. b) Optical images of the negative resist mask within the sample fabrication process and c) the metal mask at the end of the process step.

Nevertheless some issues have been noticed during the development of this processing step and several device fabrications. A first and important point in this context is the age of the resist used for the negative mask. It has been observed as shown by the SEM image in figure 3.9a that resist kept at room temperature longer than four weeks is unusable for exposure. The reasons lie on the one hand in the decomposition of the photo initiator changing its concentration and subsequently causing a lower developing rate an a higher dark erosion. On the other hand the evaporation of the solvent causes an increase in viscosity leading to a change in the layer thickness of the spun resist necessitating a different dose for exposure. As can be seen from figure 3.9a the resist pattern obtained from an aged resist strongly differs in its surface, dimensions and contrast from a perfect exposure presented in figure 3.8a. Lifting metal layers required for the metal mask process described above proves to be impossible as displayed in figure 3.9b. For some samples where aged resist has been applied again the lateral etching of the metal by formation of 'bubbles' has been observed which has been attributed to the accumulation of BCl_3 radicals in the sidewalls of the deposited metal (fig.3.9c).

A second issue is the adhesion of the masking metal layer after the exposure and development of the negative resist pattern. Despite extensively rinsing in deionized water for several minutes traces of resist can still be existent inhibiting the evaporated metal to stick to the sample surface. As a result parts of the metal are ripped off during the thorough lift-off process leading to undesirable gaps in the etching mask to be. The missing cover shown in figure 3.10a affects any part of the structure making this processing step unreliable. To overcome this fact a few seconds long, low power oxygen plasma cleaning step in a RIE chamber is implemented to remove any traces of resist and is not influencing critically the negative resist pattern at the same time.

Finally an effect on the process step reliability caused by various metal mask compositions has been noticed. Due to the necessity for top metal strengthening additional Au metal has to be evaporated onto the sample. One possible way to add on this extra layer

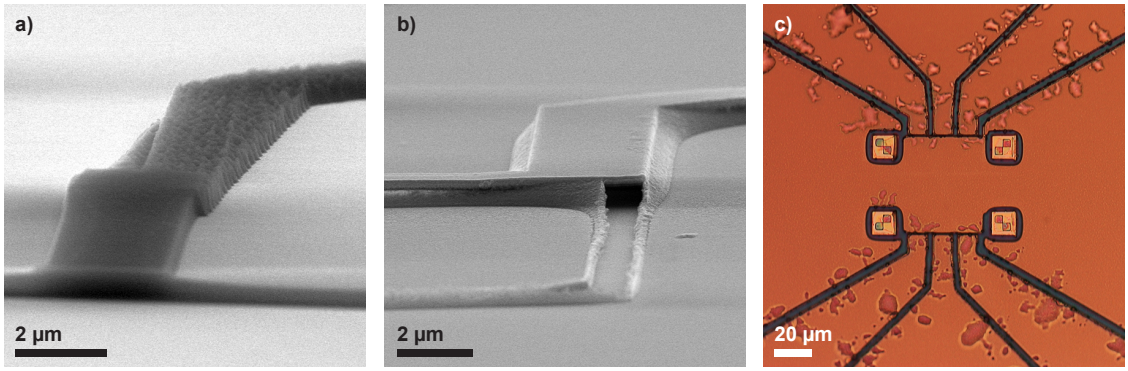

Fig. 3.9: a) SEM micrograph showing the deteriorated resist profile of aged AR4060 used during sample fabrication. b) Optical images displaying a failed lift off process for metal mask fabrication using aged resist and c) 'bubbles' caused by under etching of the top metal due to BCl_3 accumulation at the sidewall of poor-quality metal mask.

is within the metal etching mask formed from a thin 10 nm Ti sticking layer, followed by 100 nm Au and capped with 110 nm Ti for masking. During the thorough lift-off process consisting of acetone and continuous low power ultrasonic agitation the strain imposed by this layer stack is released by ripping off the top contact metal from the semiconductor top surface as depicted in figures 3.10b and 3.10c. Whereas the accumulation of strain is avoided by shifting of the strengthening Au layer to a different processing step, discussed later in this work, resulting in the use of a single layer Ti mask.

This single metal layer together with fresh resist and lift-off, consisting from warm acetone and a couple of low power ultrasonic pulses from time to time, yields a reliable fabrication step for the dry etching metal mask. The later is then transfered to the semiconductor by CAIBE and easily removed by diluted HF leaving behind the required separating gaps.

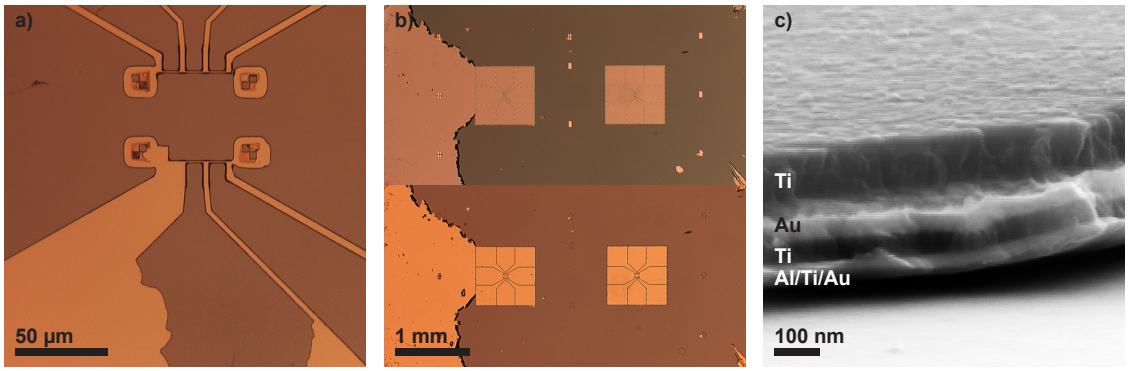

Fig. 3.10: a) The Ti metal mask is partially removed from a structure after the lift-off process. b) A sample featuring a ripped off Ti/Au/Ti mask and top contact metal after lift-off (upper image) before and (lower image) after diluted HF dip for Ti removal. c) SEM micrograph of the metal edge showing the different metal layers.

3.2 Top contacting

Fabricating vQdots from semiconductor heterostructures requires the miniaturization of devices' lateral dimensions towards a few hundred nanometers. The sub micrometer physical dimensions do not allow the application of state of the art bonding techniques or bonding agents directly at the structure's top contact, but require a suited connection to bondable contact pads. Possible connection schemes are on the one hand the coverage by an insulating material followed either by etching contacting holes [Ford 88, Tayl 93, Simp 94] or its planarization [Kina 90, Nguy 04, Latu 08] and hence contacting of the protruding structure's top allowing in both cases the connection to the pads by metal evaporation. On the other hand air-bridges have been developed in the 90's [Sher 93, Sher 94, Yaco 95, Feng 99] for sub micrometer structures as well as an alternative technique by exploiting a metal capped insulating semiconductor line mesa providing the electric contact via its top metal [Aust 97].

In the II-VI material system Maximov *et al.* [Maxi 04] first reported the fabrication of sub micrometer RTD devices where the structure has been covered by polyimide and the pillar top is contacted through a hole in the insulating layer. This method is in danger of affecting the functionality of a vQDot when the gate electrode is added based on the arising of leakage currents and parasitic capacitances between the crossing leads especially in terms of increasing device resistance with decreasing dimensions. Simultaneously it has to be ensured that the insulator etching does not impair the device's total resistance by etching residue. Whereas the air bridge fabrication method developed by Borzenko *et al.* [Borz 04] has been successfully applied to pillar of 0.8 - 1.4 μm diameter [Borz 05] as well as double RTD structures [Borz 07, Ruth 11b] from paramagnetic II-VI heterostructures, proving its reliability and potential application for contacting sub micrometer devices.

Furthermore Austing *et al.* [Aust 96] present a new design for sub micrometer RTD transistors, manufacturing single electron transistors [Taru 95] and artificial atoms [Taru 96] by making use of the symmetric depletion arising from the self aligned Schottky gate deposited around the DBH. Nevertheless the fabrication of these devices required a complex process of planarization of insulating material to enable contacting the vQDot's top. Further investigations of the new design [Aust 97] reveal that with decreasing lateral dimensions of semiconductor line mesas etched from the III-V heterostructure the pinch-off gate voltage for vertical transport through the semiconductor drops to 0 V for widths smaller 0.35 μm. This effect not only facilitates a multi-gate design for more flexibility when exploring single electron phenomena, but more important in this context is the fact that the fabrication process is simplified. Since the line mesas, whose top metal connects the device's top to its bonding pad, have been simultaneously defined with the vQDot, further processing steps related to its top contact become unnecessary.

3.2.1 Fabrication of line mesas

Based on the reported results and the promising facilitation for top contacting vQDots the applicability of the line mesa technique to the II-VI heterostructure is thus investigated.

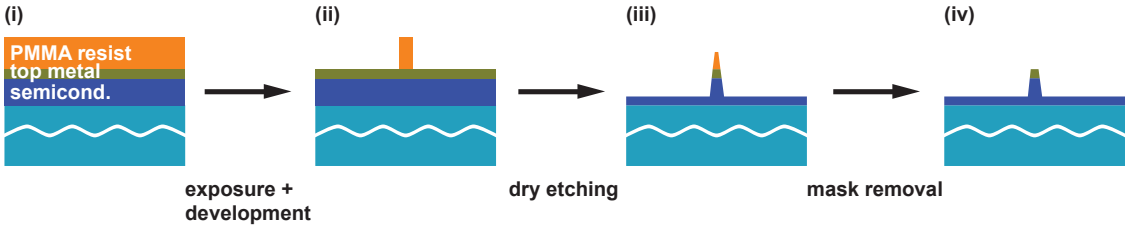

Fig. 3.11: Schematical process description for dry etching line mesas by applying a positive resist mask.

For fabricating the line mesas dry etching over wet etching is the method of choice in order to ensure appropriate control of vertical as well as lateral etching which takes place simultaneously. As done in the case of manufacturing the separating trenches, once again different masking schemes and their impact on the line mesas shape and dimensions are primarily tested.

At first the suitability of a PMMA mask fabricated by a positive process as depicted in figure 3.11 is studied. Here the area surrounding the future lines is exposed and after developing a resist mask of different widths is left behind (fig.3.12a). This pattern is then transfered to the II-VI heterostructure by CAIBE dry etching using the Ar and BCl_3 combination for about 6 min as required to reach the conducting backside layer and is followed by resist stripping. The resulting mesas for lines of different widths are displayed in top view in figures 3.12b and 3.12c, showing an increased mesa width at the backside layer level with respect to the lines top, in particular highlighted by the smaller in situ top metal width. Additionally the lines smaller 400 nm do not feature any in situ top metal at all in this case. This effect is caused by the simultaneous lateral decrease of the resist mask during etching [Gloe 75] entailing a non uniform sputtering of the semiconductor and creating sloped mesa walls (fig.3.12d). To overcome the lateral decrease of the positive PMMA resist mask the use of a negative mask from crosslinked PMMA is only suitable to a limited extent, since it can be only removed by oxygen plasma. Are further processing steps required which would be affected by a remaining PMMA mask any oxygen treatment to remove it leads simultaneously to the oxidation of the semiconductor surfaces and thus crucially influence the device properties. As a result neither a positive nor a negative PMMA resist mask are suitable to fabricate line mesas in the II-VI heterostructure.

In contrast to a negative mask from crosslinked PMMA a negative resist pattern from e-beam exposure of image reversal optical resist as used for defining trenches in the previous section is removable by resist stripping agents not affecting the II-VI semiconductor. Such a 650 nm thick and ca. 400 nm wide resist mask is depicted in figure 3.13a revealing a nice line pattern prior to dry etching by CAIBE. The two major disadvantages of this processing step become apparent from the SEM image in figure 3.13b taken after dry etching and resist removal in stripping agent. First, the sloped and rough semiconductor mesa's lateral walls originate from the shadowing of the relatively thick resist mask while etching at an angle of 70° to avoid trenching around the mesa [Some 76]. Redeposition of sputtered material onto the lateral resist walls during ion beam milling [Gloe 75], generat-

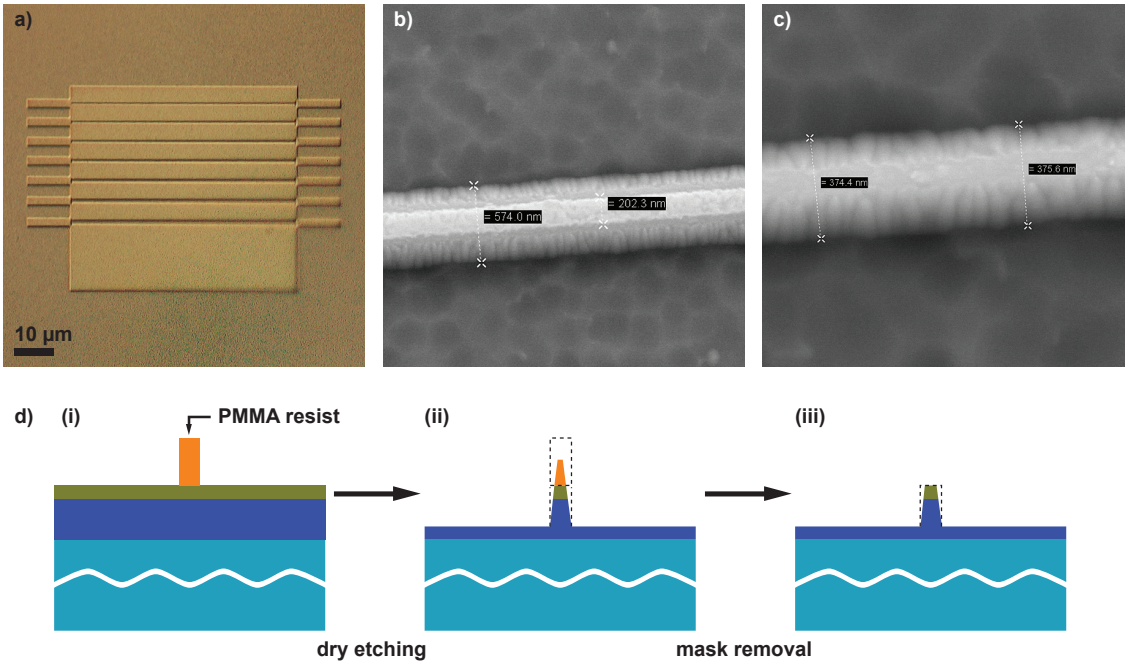

Fig. 3.12: a) PMMA resist mask (darker brown) used to dry etch line mesas. b) 600 nm and c) 400 nm line mesas after dry etching and mask removal exhibit sloped sidewalls and reduction as well as absence of the *in situ* top metal due to lateral mask decrease during dry etching. d) Schematical description of the vertical and lateral resist mask reduction during dry etching.

ing sidewalls after resist stripping, is the second negative issue. Besides, the uncontrollable presence of these high walls has a critical impact on possible contacting schemes for testing the electrical properties of the line mesas. From the undefined shape of these test line mesa and the arising of parasitic redeposition sidewalls the choice of a negative mask from e-beam patterned image reversal optical resist has to be abandoned.

A further option for fabricating line mesas is again the implementation of low rate

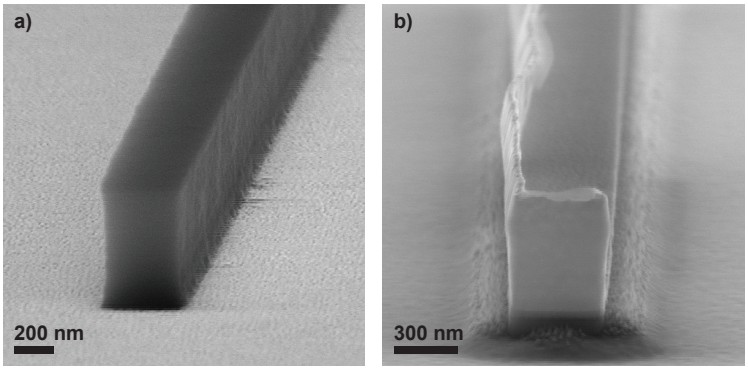

Fig. 3.13: SEM micrographs display the negative resist mask from ARU4060 a) before, exhibiting steep sidewalls, and b) after dry etching and resist removal, leaving behind redeposition sidewalls as well as an undefined shape.

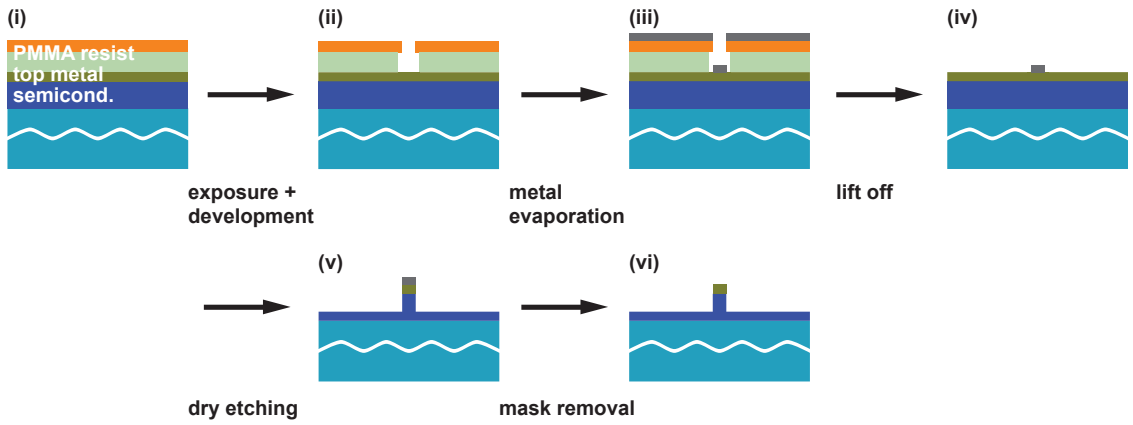

Fig. 3.14: Schematical process description for dry etching line mesas by applying a metal mask, fabricated using a PMMA bilayer resist.

etching metal for masking. Compared with the process for manufacturing deep trenches as described in the previous section, this time a positive PMMA resist pattern is converted to a metal mask. As shown by figure 3.14, a EBL step exposes the lines of different widths in a 300 nm thick PMMA double layer built up from 600K (4%) as bottom and 950K (3%) as top layer. Based on the higher sensitivity of the bottom layer an undercut is created during the developing process allowing the evaporation of maximum 130 nm of metal without generating any troubling metal side walls after the lift-off step. The dimensions of the evaporated metal mask is thus given by the upper less sensitive layer. Following the aforementioned requirements for the masking material and the presented advantages, Ti is once again the metal of choice to fabricate the dry etching metal mask.

At first the mask for line mesa fabrication is built up from a multilayer stack consisting of a thin 5 nm Ti adhesion layer, followed by 90 nm Au and capped with 25 nm Ti. In consequence of the II-VI heterostructure the maximum and minimum height of a line mesa is determined by the lower and upper edge of the high doped 400 nm thick backside layer. In terms of a possible deposition of a thin insulator and the necessary surface refreshing dip in chromosulfuric acid [Maxi 04] is it albeit favorable to stop in the backside's layer upper 100 nm consisting of 2×10^{19} cm^{-3} highly doped ZnSe. Thus the line mesa's height range of 145 to 245 nm, including the *in situ* top metal, predefines the duration of the dry etching sequence. Given the known etching rates of 40 nm/min for Au and 5 nm/min for Ti, it is possible to stop in the Au layer avoiding the necessity of an additional wet etching step for removing any remaining Ti mask, displayed schematically in figure 3.15a. Hence the additional *ex situ* evaporation of sacrificial Au enables here a more reliable fabrication than the available 30 nm of *in situ* Au in case of eventual required variations in etching time. The convenience of this method is limited by the most likely formation of gold-chlorine compounds when etched in a chlorine based plasma as pointed out by Franz *et al.* [Fran 02]. This aspect is enhanced by their low vapor pressures [Land 70]

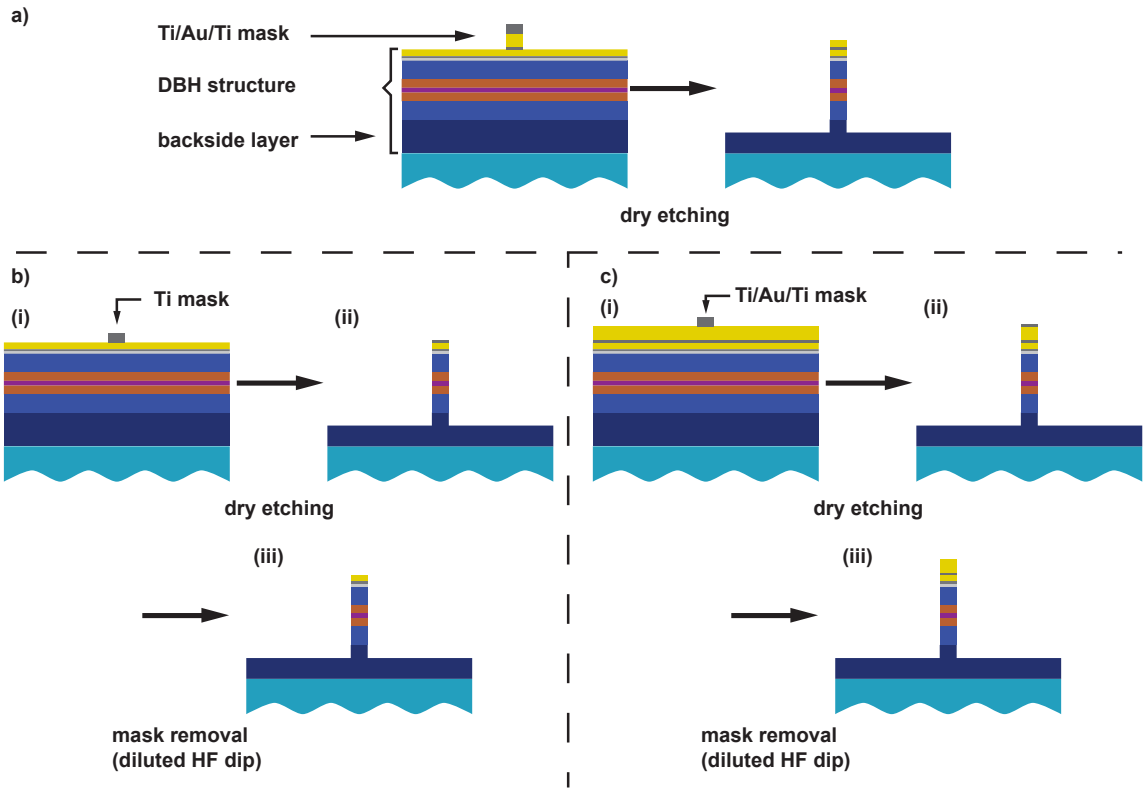

Fig. 3.15: Schematical process description for dry etching line mesas by applying: a) a Ti/Au/Ti mask and stopping the dry etch in Au, b) a Ti mask onto *in situ* top contact and the removal of the excess Ti metal after dry etching by a wet etch dip, c) a Ti/Au/Ti mask and the removal of the excess Ti metal after dry etching by a wet etch dip.

when performing the dry etching sequence by default at 20 °C. Taking into account the diameter of the bridge's posts used to contact the line mesas being $\leq$ 500 nm, any additional resistive layer on the sample surface adds at least area scaled to the total device resistance. Therefore line mesas fabricated by this recipe exhibited mostly diodic characteristics with resistances ranging from several 100 kΩ to MΩ when a current is passed just along the top contact metal. As a consequence this fabrication technique of using a sacrificial Au layer is abandoned and a process similar to the aforementioned trenches fabrication from a metal mask is pursued.

In the second approach ca. 55 nm Ti metal replaces the previous multilayer stack and is directly deposited onto the *in situ* top metal finalized with Au. Taking account of the etching rates the thickness of the Ti layer is chosen such that 10 to 20 nm metal remain on the structure's surface after the CAIBE dry etching process step. Subsequently the excess Ti metal still covering the line mesa is then removed by a short dip in diluted hydrofluoric acid leaving behind just the *in situ* Au layer (fig.3.15b). Surprisingly samples fabricated following this approach exhibited diodic I-U characteristic when the connection to the mesa's top metal has been tested.

In order to test the contact between the bridge post of $\leq$ 500 nm diameter and the

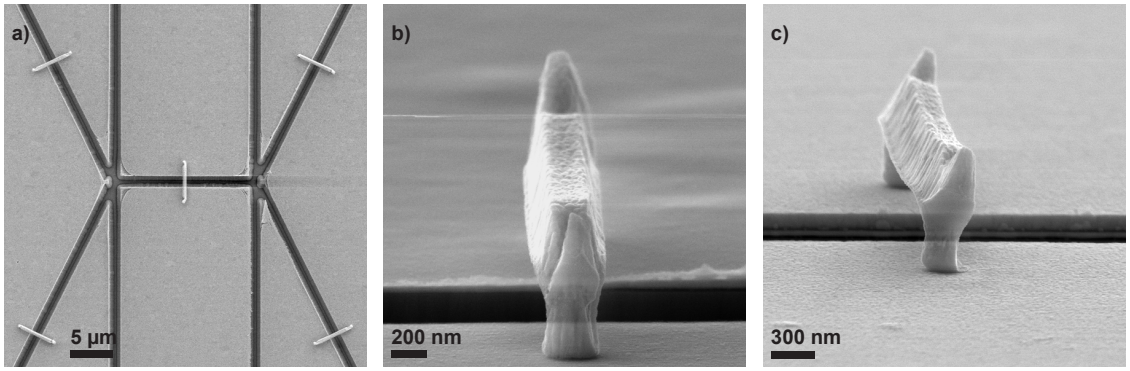

Fig. 3.16: SEM micrographs show a) the layout used to test the electrical contact between air-bridges on b) the *in situ* top metal and c) the additional *ex situ* Ti/Au layer.

in situ Au a simple test structure is fabricated. The *in situ* top metal remains on the surface of the sample, but the different contacts divided by deep trenches are connected only by bridges (fig.3.16). In parallel to this sample a second one is identically fabricated after *ex situ* 10 nm Ti / 100 nm Au have been evaporated prior to fabrication start. The difference between the two samples is thus the topmost layer to which the bridges connect. Electrical tests then revealed that the sample with bridges onto the *ex situ* Au exhibits resistances of about 10 Ohm which add nicely when two bridges are measured in series. Whereas the sample with bridges onto *in situ* Au always exhibits for all measurement configurations the same high resistance obtained when measurements between adjacent structures divided by trenches are performed. Based on these results it is preferable to additionally evaporate *ex situ* Ti/Au and connect the bridges to this layer.

Therefore the second approach for fabricating line mesas is modified such that a multilayer metal mask from 10 nm Ti / 100 nm Au / 110 nm Ti is evaporated during trenches fabrication as described in the previous section. For defining the line mesa 65 nm Ti are evaporated and the aforementioned fabrication method consisting from dry etching in CAIBE and wet etching the excess Ti metal mask by diluted hydrofluoric acid is applied (fig.3.15c). It should be pointed out that since the *in situ* top contact metal is built up from Al/Ti/Au, the diluted hydrofluoric acid dip also attacks the Al/Ti adhesion layer by lateral etching. For some lines mesas of widths $\leq$ 200 nm this lateral etching resulted in a detachment of the Au metal leaving behind the bare semiconductor surface and inhibiting ohmic contacts to the bridge posts. This difference in the varying manifestation of lateral etching has been observed to depend on the processed wafer. These various wafers have nominally identical semiconductor - metal top contacts formed from 30 nm 2×10^{19} cm^{-3} highly doped ZnSe followed by 10 nm Al/ 10 nm Ti/ 30 nm Au, hence one possible explanation could ensue from variations of the semiconductor - Al interface. But nevertheless no specific reason can be unquestionable related to this behavior to date and this effect has to be taken into consideration for fabrication processes implementing this method.

Again the implementation of a metal mask for dry etching appears to be adequate

in order to fabricate line mesas down to 200 nm for investigation of a possible electrical pinch off as a function of the lateral dimensions.

3.2.2 Applicability of line mesas

For testing the line mesa concept in the II-VI heterostructure the design depicted in figure 3.17a and 3.17b in top and side view is chosen. Since an ideal Schottky contact used in the III-V material system is not available in the II-VI material system [Tyag 75, Swan 69], the pinch off by sidewall depletion is investigated by this means. II-VI RTD heterostructures with $(Zn_{0.92}Mn_{0.08})Se$ QWs of 5 nm and 9 nm in-between 6 nm $(Zn_{0.8}Be_{0.2})Se$ barriers are used as a testbed for the line mesa test structures. Micrometer sized RTD control structures fabricated from this material exhibit clean resonances at about 225 mV and 190 mV source-drain-voltage. Following the aforementioned processing steps for contact separation, line mesa fabrication and air-bridges the chosen design is then applied to the II-VI heterostructures for test device fabrication. The bonding contacts for the top and backside are separated by trenches ensuring the only possible current flow between them being through the mesa whose top metal is connected via air-bridge to the top contact bonding pads. Passing a current from a top contact to its corresponding counterpart ensures the connection to the mesa's top metal (fig.3.17c). With this property established

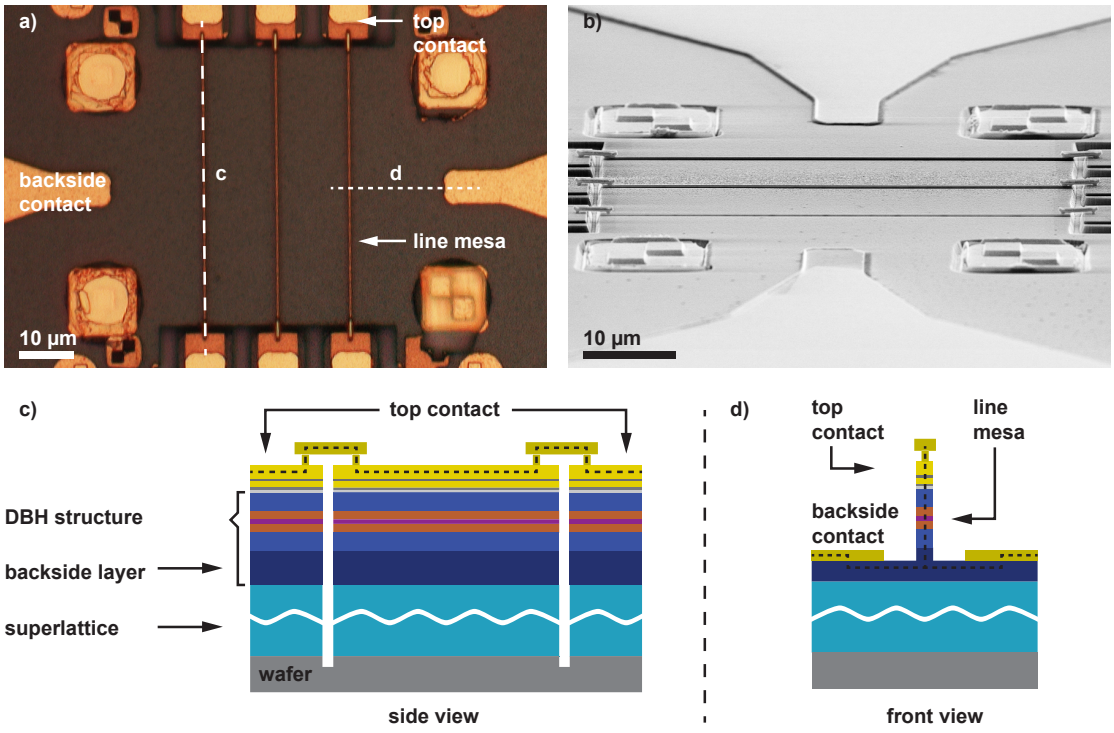

Fig. 3.17: a) Optical image and b) SEM micrograph display in top and side view respectively the structure used to electrically test the applicability of the line mesa concept. Schemes of the measurements used to test for c) the electrical contact to the line mesas top contact and d) the insulating properties of the semiconductor line mesa.

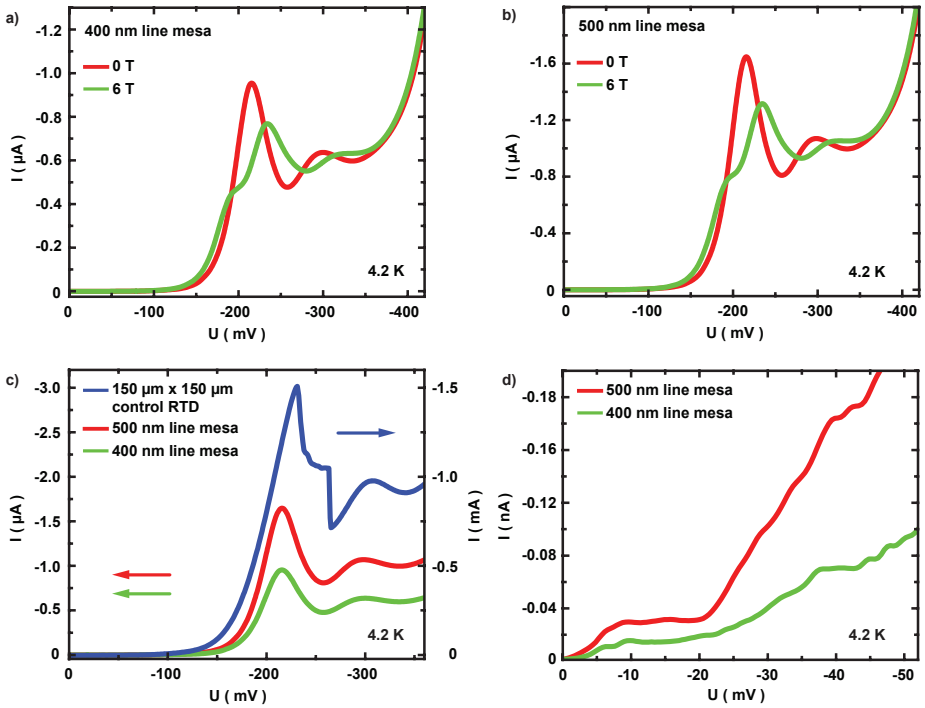

Fig. 3.18: I-U measurements at 0 T and 6 T of a) a 400 nm and b) 500 nm wide line mesa exhibiting the Giant-Zeeman splitting. c) The resonance position and current of the lines are compared to the characteristic control 150 μm $\times$ 150 μm RTD pillar. d) Zoom-in to the low bias regime.

the electric behavior of line mesas of different widths is checked by looking at the I-U characteristics as the current is passed from the top contact to the backside through the semiconductor RTD heterostructure (fig.3.17d).

Figure 3.18 displays different I-U measurements from structures with line mesa widths of 400 nm and 500 nm fabricated using a Ti metal mask for the lines and a PMMA positive resist mask for the trenches. First thing to point out is the RTD behavior of these line mesas which exhibit a resonant peak at the same position of about 225 mV similarly observed in the 150 μm $\times$ 150 μm RTD control structure, shown by figure 3.18c. Based on the I-U characteristics at 0 T and 6 T, depicted by figures 3.18a and 3.18b, by applying a magnetic field parallel to the current through the line and perpendicular to the heterostructure, the lines from both dimensions still exhibit Giant-Zeeman splitting. These two observations imply that down to a line width of 400 nm the line mesas do not become insulating and the RTD characteristics of the II-VI heterostructure remain unaffected. Since artificial atoms are operated at bias voltages of some mV down to some μV a closer look at the low bias regime (fig.3.18d) still shows a non negligible background current with additional features on top. The background current with the superimposed structure emphasizes that the lines do not become insulating in the low bias regime as well. Thus given these facts further decrease in line width is required in order to find out whether narrower lines become insulating and can offer a possible contacting method.

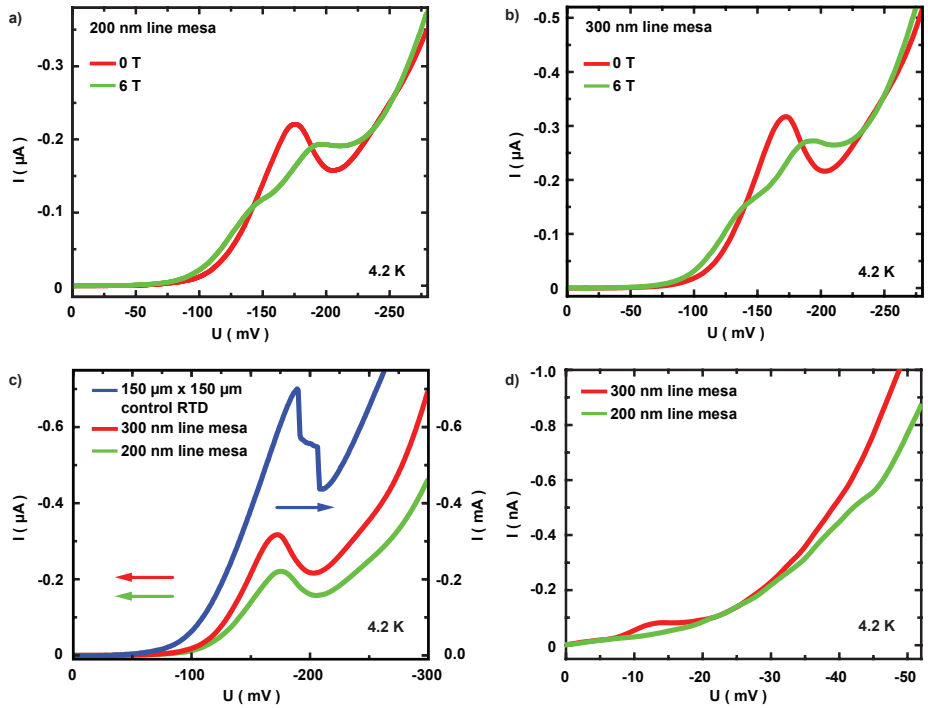

Fig. 3.19: I-U measurements at 0 T and 6 T of a) a 200 nm and b) 300 nm wide line mesa exhibiting the Giant-Zeeman splitting. c) The resonance position and current of the lines are compared to the characteristic control 150 μm $\times$ 150 μm RTD pillar. d) Zoom-in to the low bias regime.

Due to the aforementioned difficulties in fabrication using the listed steps, the process for fabricating 300 nm and 200 nm lines is changed such that the trenches are etched and the top metal is strengthened using the Ti / Au / Ti metal mask. Again the I-U measurements of 300 nm and 200 nm line mesas compared to the 150 μm $\times$ 150 μm RTD control structure, displayed in figure 3.19c, exhibit clean resonances at about 190 mV and imply that the pinch off dimension is still not reached. In addition to this fact the unchanged magnetic properties show that the II-VI RTD heterostructure of the line mesas remains fully functional (fig.3.19a and 3.19b). Likewise a high resolution measurement of the low bias regime reveals once again non negligible background current with additional structure superimposed (fig.3.19d).

Figure 3.20 shows the attempt to apply a gate to the 300 nm and 200 nm sample by depositing a 100 nm SiO/SiN insulator superlattice and evaporating Ti / Au on top. In the previous work of Austing *et al.* [Aust 97] the application of the Schottky gate helps to pinch of the line mesa due to depletion at the metal-semiconductor interface. Unlike there no such effect is observed for the II-VI line mesas, since the above presented I-U characteristic are recorded from such a gated structure. Applying a gate voltage does not influence the electrical behavior, probably due to the non optimized gating technique in this case.

From these experiments can be concluded that line mesas as small as 200 nm are

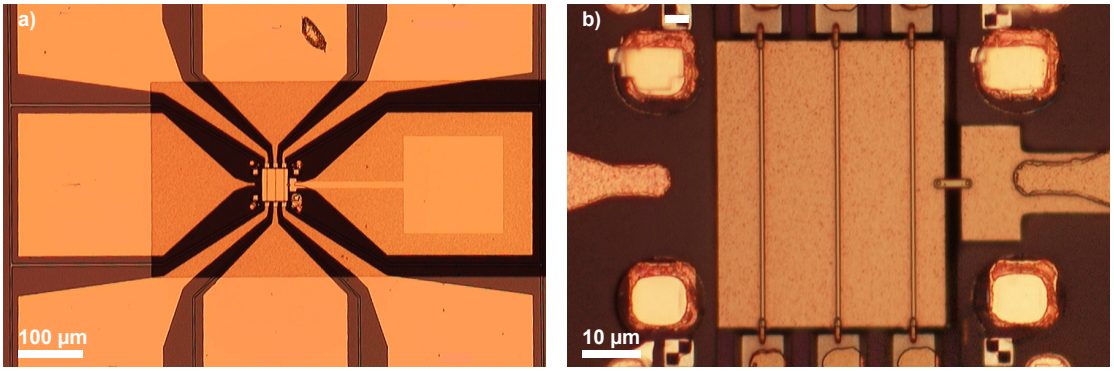

Fig. 3.20: a) Line mesa testing structure covered by insulator and gated. b) Zoom-in to the gated line mesas.

not applicable as contacting method to possible submicrometer RTDs. A further miniaturization of the lines becomes challenging in terms of contacting and therefore the line mesas lose their possible advantages over the contacting technique by air-bridges. Therefore the line mesa contacting method is abandoned and future submicrometer pillars are electrically contacted by an adjusted air-bridge technique.

3.2.3 Air-bridge technique

In addition to the development of an adequate fabrication step for submicrometer line mesas compatible with the II-VI heterostructure, their electrical connection to bonding pads while spanning the separating trenches has to be ensured. Alternatively to the sub micrometer bridge contacting technique the method of a suspended line, which can offer a simplification of the total fabrication process and facilitates a reliable electrical contact, is investigated at first. In silicon the fabrication of suspended micrometer sized structures by patterning an adequate mask by EBL, transferring the structure to the semiconductor by dry etching and suspending it with the assistance of isotropic etching has already been demonstrated in the early 90's by Lutwyche *et al.* [Lutw 91]. Wang *et al.* [Wang 94a] also present the fabrication and contacting, using freestanding GaAs bridges, of submicrometer RTDs by means of photolithography and selective wet etch. Moreover, 0.25 μm wide silicon wires spanning a 4 μm gap by using photolithography and isotropic etching are presented by Bruschi *et al.* [Brus 01].

The basic idea to be tested for consists from fabricating line mesas directly connected to the bonding pads, meanwhile the different contact areas are still separated by notches. For this purpose first the line mesas are defined, followed by the fabrication of trenches using dry etching and finalized by applying a isotropic wet etch dip in chromosulfuric acid to remove the underlying semiconductor, leaving behind a suspended metal junction between the bonding pads and the line mesa. In a first attempt the lines and the bonding pads are prepared by EBL using the established metal mask fabrication step (fig.3.15b and fig.3.21a). After dry etching down to the backside layer, the excess Ti remains

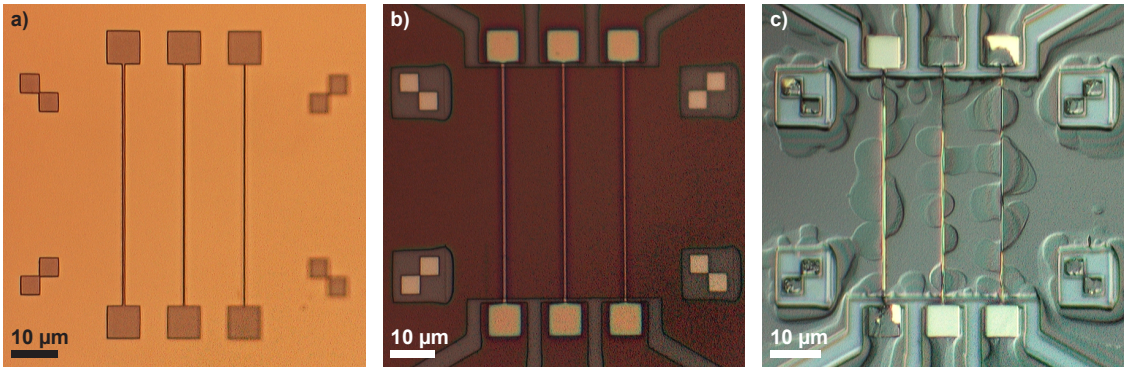

Fig. 3.21: Line mesas directly connected to the bonding pads are fabricated by a) applying a Ti metal mask, followed by dry etching down to the backside layer. b) A PMMA positive resist mask is used to define the trenches and to protect the structure during under etching the metal junctions. c) The resulting structure is strongly affected by the creeping of the acid along the resist - semiconductor interface.

on the lines and the trenches are patterned utilizing the PMMA positive resist mask processing step earlier described in this chapter (fig.3.3a,d and fig.3.21b). The PMMA resist mask remains on the structure while a 1 min wet etch in chromosulfuric acid is performed to remove the semiconductor underneath the line at the trenches by lateral etching. Based on figure 3.21c, displaying the sample after the resist mask has been removed, the chromosulfuric acid creeps laterally along the resist - semiconductor interface and attacks uncontrollably the structure. Therefore using the resist mask while wet etching the semiconductor beneath the metal proves to be unsuitable to manufacture the suspended metal link.

In a second attempt the PMMA resist mask used during wet etching is thus replaced by the patterned top metal. For this purpose once again the lines and the bonding pads

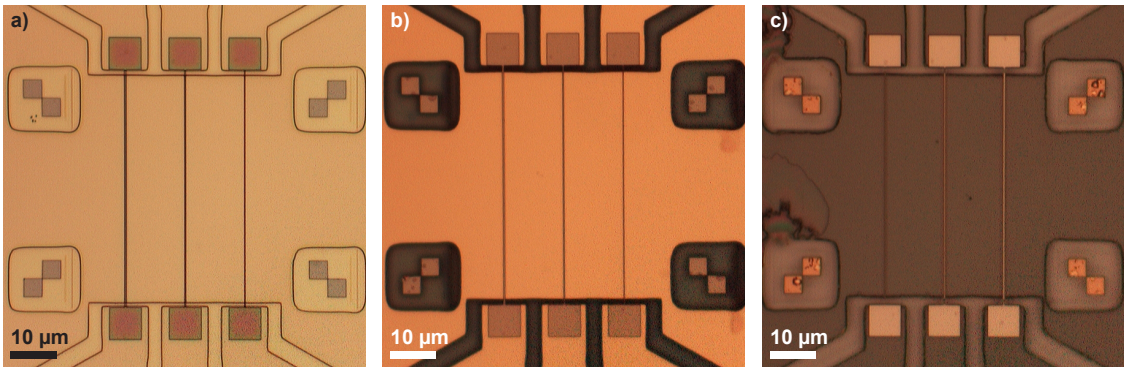

Fig. 3.22: Line mesas directly connected to the bonding pads are fabricated by a) applying a Ti metal mask and a PMMA positive resist mask is used to define the trenches. b) The top metal is used to protect the structure during under etching the metal junctions. c) The Ti metal mask is subsequently transfered to the semiconductor by dry etching down to the backside layer.

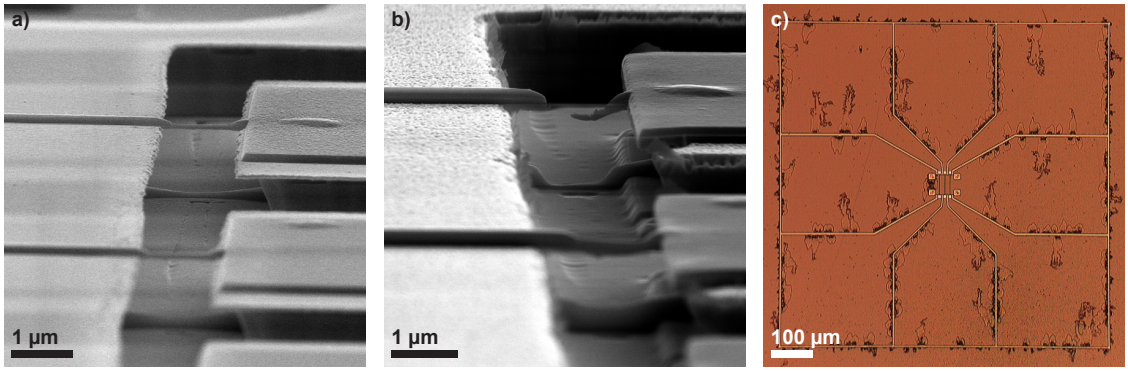

Fig. 3.23: SEM micrographs display a 200 nm wide metal junction: a) after dry etching the trenches and the wet etch step, b) being destroyed after the subsequent dry etching step down to the backside layer. c) Top view of the finished structure displaying strong lateral etching.

are created by the metal mask fabrication step (fig.3.21a). This time the metal mask is not immediately transfered to the semiconductor, but followed by the fabrication of the trenches applying the PMMA resist mask process step (fig.3.22a). After dry etching the notches the resist is removed and a wet etch in chromosulfuric acid is carried out for several minutes (fig.3.22b). The SEM image in figure 3.23a displays on the one hand the established metal junction and on the other hand some still existing semiconductor material underneath the metal line, which is more pronounced with increasing line width. Furthermore after continuing the process and dry etching down to the backside layer the junctions of about 200 nm wide lines are destroyed (fig.3.22c and fig.3.23b) and severe, uncontrollable lateral etching in different parts of the structure becomes visible (fig.3.23c). Especially due to the uncontrollable behavior of the wet etch when interacting with the heterostructure for longer etching times and the potential damage to lines $\leq$ 200 nm wide, the idea of suspended metal junctions is not further pursued.

Since the junctions are not applicable the utilization of metallic air-bridges remains the method of choice for contacting the line mesas or any other mesa structure. The main challenge in this context arises from the necessity of spanning deep separating notches, to connect mesas of low height avoiding any shortening by touching the highly doped backside layer. An example of this situation is presented in figure 3.24a showing a bridge spanning a separating trench to contact a micrometer sized pillar fabricated following the recipe in [Borz 05]. As a consequence of the > 1 μm deep groove around the RTD mesa the 4-layer PMMA resist system, consisting of two layers of 950K(3%) followed by two layers of 950K(5%), used to manufacture the air bridge does not level the rough surface sufficiently. Figure 3.24b, showing an attempt to connect the line mesa to its bonding pad, displays also a more serious situation regarding the planarity of the 4-layer resist related to the required > 1 μm deep trenches.

These challenges arising from topographically uneven surfaces and their planarization by spun-on resist/polymers have been investigated in detail in the 80's by different groups [Whit 83, Bass 83, Wils 86, Born 90]. They conclude that the spun-on resist/polymer

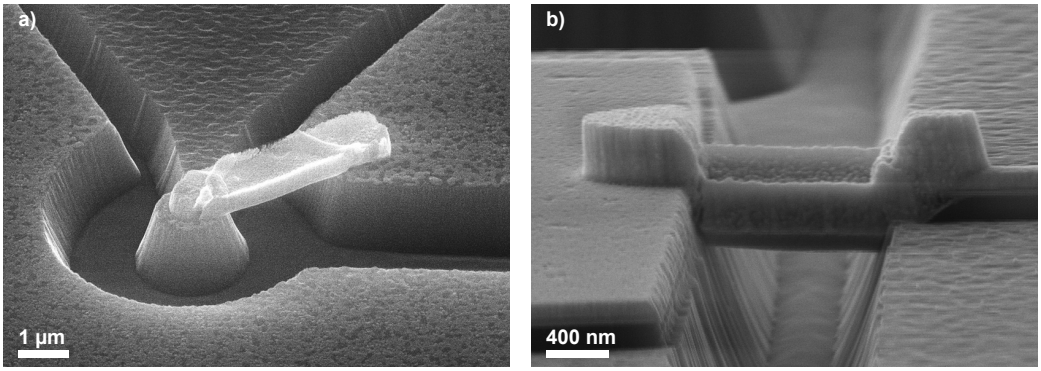

Fig. 3.24: Air-bridges fabricated by a 4-layer resist system are spanning ∼1.3 μm deep trenches to connect to a) a 1 μm pillar and b) a line mesa.

planarity depends on the step height and distance of isolated features as well as type and viscosity of the spun-on resists/polymers. The topography of the resist/polymer surface, even for multi layer resist systems, has thus a crucial influence on the patterned structures. In addition to this the difficulties in air-bridge fabrication emerging from topologically rough surfaces have also been investigated and addressed by Borzenko *et al.* during fabrication of non-planar transport structures [Borz 03].

In order to obtain a clear picture on the resist leveling above and near the deep separating notches in the line mesa devices, the 4-layer resist system is spun on and windows are opened in the resist by EBL exposure and development. The tilted evaporation of 5 nm Au prevents the charging of the resist and thus inhibiting its deformation during inspection. Figure 3.25a displays the resist profile around the $>$ 1 μm deep trench of a line mesa structure and indicates an extreme reduction of the 1.2 μm resist system, determined on a large-area flat surface, down to about 0.5 μm at the bonding pad edge to the trench. This extreme variation in the resist profile at the notches has a critical impact on the air-bridges fabrication utilizing the multiple acceleration voltage EBL presented by Borzenko *et al.* [Borz 04, Borz 05, Borz 07]. Exploiting the dependence of the electrons

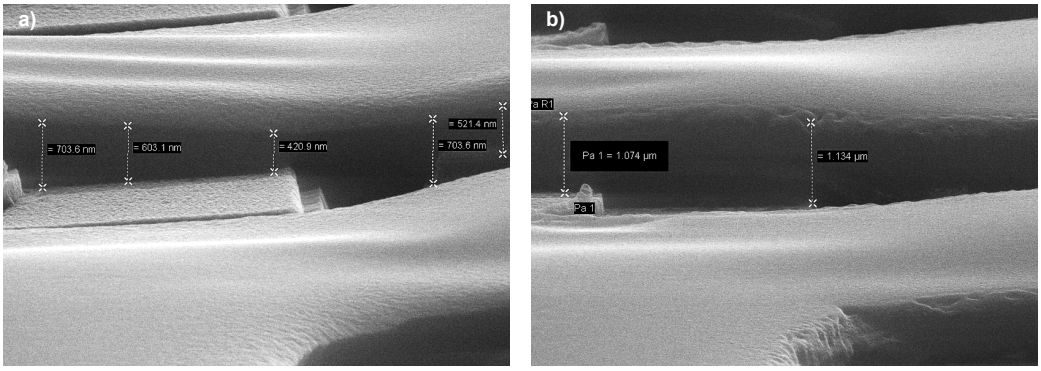

Fig. 3.25: Resist profile near ∼1.3 μm deep trenches in a line mesa structure when applying a) a 4-layer resist system and b) a modified 5-layer resist system.

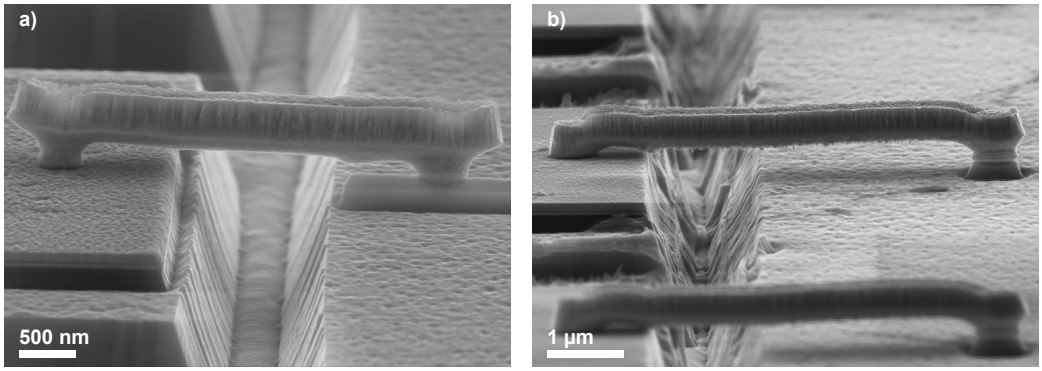

Fig. 3.26: Air-bridges fabricated by a 5-layer resist system are spanning ∼1.3 μm deep trenches to connect to a) a line mesa and b) a submicrometer sized pillar.

penetration depth in PMMA related to their energy, this method is used to define the bridge span in the resist. Since the penetration depth is fixed by the chosen parameters, extreme flatness imperfections in the resist lead automatically to a faulty design of the bridge. Furthermore the decrease of the acceleration voltage does not particularly help in this case, because the lift-off is inhibited after 400 nm Au needed for bridge fabrication have been evaporated onto the sample. A simple and easy solution is adding a further resist layer from 950K(3%) PMMA to the resist system as shown by Borzenko *et al.* for non-planar transport structures [Borz 03] in order to obtain a thicker and smoother resist relief. Doing so the resist profile gained from the 5-layer resist system is shown in figure 3.25b, where the sample has been prepared following the aforementioned technique. The resist thickness at the bonding pad edge to the trench increases to about 1.1 μm which enables the bridge fabrication using the penetration depth vs. acceleration voltage graph from [Borz 07] to reliably manufacture air-bridges, spanning the separating > 1 μm deep trenches. Figures 3.26a and 3.26b exemplarily display bridges fabricated by the adjusted method contacting the line mesas to be tested as well as later the pillars to form the artificial atom.

Therefore the 5-layer PMMA resist from three layers of 950K(3%) followed by two layers of 950K(5%) becomes the standard resist system for fabricating air-bridges to electrically connect to submicrometer structures.

Chapter 4

Pillar

State of the art artificial atoms from vertical quantum dots are based on submicrometer pillars from III-V semiconductor heterostructures containing a DBH [Taru 96, Kita 07b]. With a well developed II-VI RTD heterostructure the next step aims at the pillar mesa miniaturization in order to establish the vertical quantum dot. Thus the fabrication of pillars with diameters as small as 200 nm in terms of proper electrical connectivity and the possibility to attach a gate electrode occupies the center stage of this chapter. In this light different fabrication methods and process steps are investigated at first. In the final section electrical and magnetic measurements, accompanying the pillar mesa fabrication as well as miniaturization and showing the advancing lateral confinement, are presented.

4.1 Pillar mesa fabrication

The starting point of this working step is grounded in the research of Borzenko *et al.* [Borz 05], where pillar of about 1 μm diameter are manufactured, and which is also used in the framework of this thesis for wafer characterization in the beginning. This process utilizes the PMMA resist as an etching mask for the pillar, by first lithographically exposing the areas to be etched: the future trenches and the backside contact (fig.4.1a). In so doing the resist island in the center of the structure defines the pillar to be. In the second lithography step, depicted in figure 4.1b, just the separating notches are defined and the PMMA resist is used once again as an etching mask. This fabrication method reaches its limits when further pillar diameter miniaturization towards 400 nm to 200 nm is required. One inhibiting downside is again the utilization of the PMMA resist mask, which becomes more difficult to remove as the diameter is scaled down. As already mentioned in chapter 3.1 the prolonged bombardment with energetic ions hardens the resist and hinders proper mask removal in particularly for small diameters. Additionally the SEM micrograph in figure 4.1c, showing a final device consisting of a ~ 0.7 μm pillar, indicates the exceedingly narrowing of the junction to the backside contact. During the 15 min long CAIBE dry etching of the separating trenches, predefined in the second lithography step and closely surrounding the pillar, the lateral etching of the resist mask becomes non-negligible, described in chapter 3.1. Besides, the immediate proximity of ~ 1.3 μm trenches to the

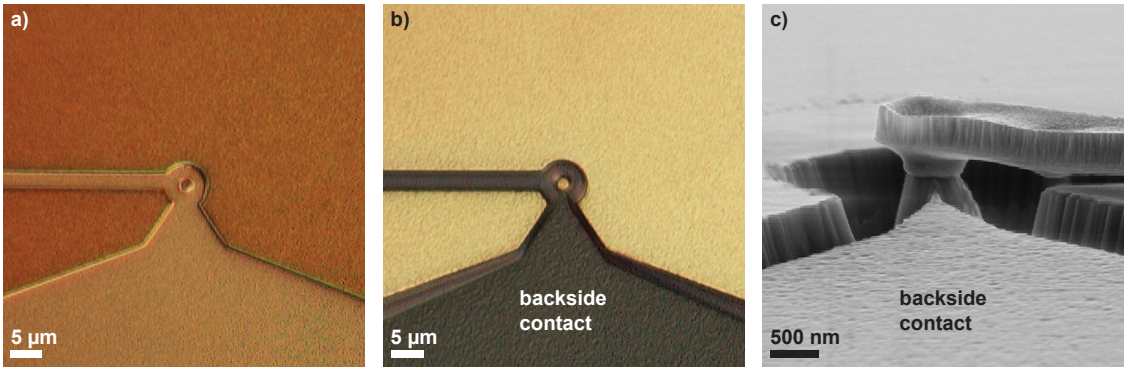

Fig. 4.1: a) Resist mask used to define the micrometer sized pillar in the 1st fabrication step and b) a top view on the pillar after etching the trenches in the 2nd step, following the recipe of T. Borzenko. c) SEM micrograph showing the narrow junction between a 0.7 μm pillar and its backside contact.

$\sim$ 200 nm high pillar does not only challenge the gate installation, but makes it rather impossible to align it within a few nm to the $\sim$ 7 nm QW, being a stringent requirement and discussed in chapter 5.2.1.

For this reasons this process is not further pursued and a new one, based on a readjusted device design with pillars further away from the notches, has to be developed. The idea behind the new process is to detach the fabrication of the trenches from the fabrication of the pillar. This is achieved by first fabricating the trenches following the recipe for the Ti metal mask presented in chapter 3.1. Subsequent to this step the pillar is lithographically defined and the pattern transfered by CAIBE dry etching to the semiconductor heterostructure.

One possibility to manufacture small mesas is the application of a resist mask whose dimensions predefine the lateral size of pillars. Since a resist mask from non-crosslinked PMMA exhibits lateral mask degradation, difficulty in removal and remaining residue afterwards, it is not favorable for implementation, see chapter 3.2.1. Alternatively the use of negative resist masks helps to overcome the lateral degradation due to their robustness against ion bombardment. At this point the application of crosslinked PMMA again is waived, because it can only be removed by oxygen plasma and no other resist strippers. The oxidation of the exposed semiconductor surfaces leads to uncontrollable effects on the elelctrical properties of small mesas and thus puts the use of oxygen plasma beyond dispute.

As previously discussed in chapter 3.2.1 the use of image reversal optical resist lithographically exposed by e-beam qualifies as an option. Figure 4.2a shows exemplarily such a negative resist column of $\sim$ 220 nm diameter from the image reversal optical resist ARU4060. This resist column is robust enough to perform CAIBE dry etching at an incidence angle of 70° using Ar chemically assisted by BCl_3 as previously described in chapter 3.2.1. Its result is displayed in figure 4.2b and shows, similar to the test for line mesas, that shadowing and redeposition take place. Once again the shadowing affects

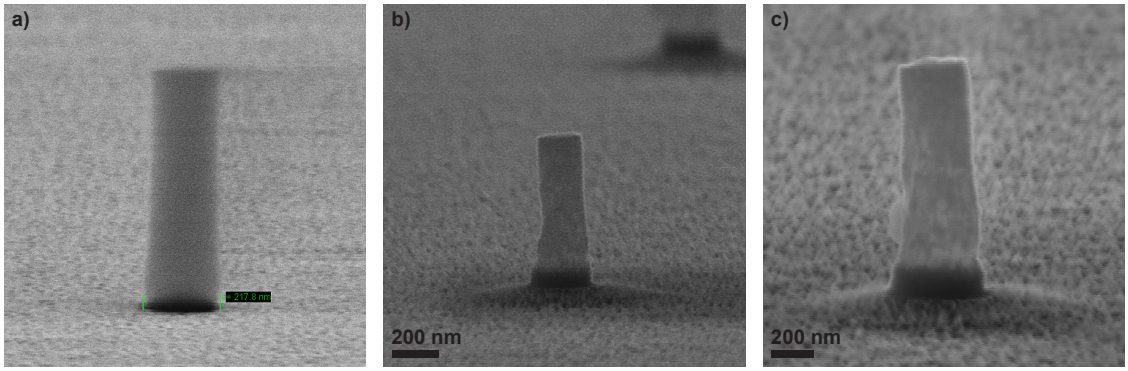

Fig. 4.2: a) SEM micrograph shows a ∼ 220 nm resist column from the image reversal optical resist ARU4060. Redeposition sidewalls are not removed b) after performing a CAIBE dry etching step and c) immerging the sample in hot resist stripper applying simultaneously ultrasonic agitation.

extremely the shape of the pillar especially when etching reaches the semiconductor. The smooth sloping structure inhibits the formation of a predefined mesa required to obtain a well 3D confinement. Additionally, after treating the structure in hot resist stripper and ultra sonic bath the redeposition walls are not removable (fig.4.2c). Due to the resist height of about 650 nm these walls inhibit any proper contacting of small pillars. Thus the application of the image reversal optical resist for submicrometer pillar fabrication is not practical and not further pursued.

Analogous to the line mesa fabrication the method of choice remains the implementation of a metal mask. Based on the etching experience gained from the line mesa fabrication once again the metal mask is formed from Ti (see chapter 3.2.1). In the beginning a PMMA bilayer resist from 600K (4%) followed by a layer of 950K (3%), both spun at 6000 rpm, is deposited, exposed and developed. Later on an additional 600K (4%) PMMA layer is added to the first one to ensure proper resist coverage of deep trenches and avoid difficulties during the subsequent lift off step. By metal evaporation and lift off the positive resist pattern is then transfered to the metal forming the mask on the topmost wafer surface. The described process is displayed schematically in figure 4.3 and represents the basis of the fabrication and miniaturization of the lateral pillar dimensions.

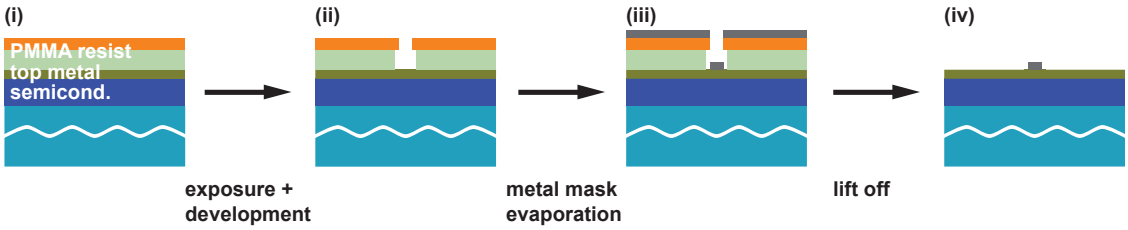

Fig. 4.3: Schematic process to fabricate the metal mask for submicrometer sized pillars using the PMMA bilayer resist system 600K (4%)/950K (3%).

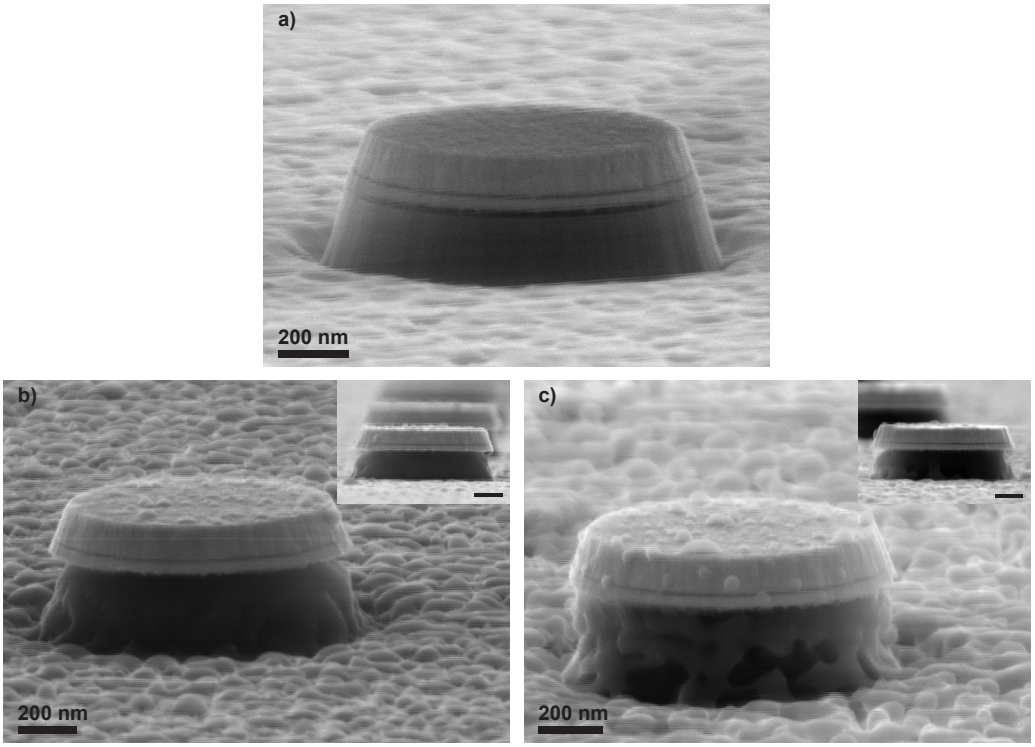

Fig. 4.4: a) A pillar etched at 90° angle of incidence by a single CAIBE step displays sloped sidewalls at 70° and trenching at its bottom. The influence on the pillar shape and surface are shown after b) a 1st 20 sec wet etch dip in chromosulfuric acid and after c) a subsequent 20 sec one.

Having developed the technique for fabricating the defining mask, transferring it to the II-VI heterostructure and obtaining well defined pillars is the next step to be established. Recalling that the II-VI heterostructure is *in situ* capped with Al / Ti / Au after MBE growth, this top metal has to be removed by dry etching. Wet etchants suitable to remove the top metal also take off the Ti metal mask and undercut gold due to their isotropic etching behavior which leads to the removal of the ohmic contact provided by the *in situ* metal layer stack.

The simplest way is to apply a single step CAIBE dry etching with Ar assisted by BCl_3 at a 90° angle of incidence, as usually used for control samples, to etch away both the metal and the semiconductor. Figure 4.4a displays exemplarily the obtained pillar mesa from this technique. Here on the one hand the pronounced trenching around the pillar is well observable as described by [Some 76]. On the other hand the pillar mesa exhibits sloped sidewalls at an angle of about 70° which leads to a significant widening of the mesa at position of the QW. Despite this downside the adaptability of the shallow wet etch concept of Austing *et al.* [Aust 96] to create a shadow mask from the mesas metal top contact may turn it into an advantage. The isotropic etching characteristic reduces the width of the pillar at the QW level and can simultaneously enable an accurate deposition of the gate electrode at its vertical height. To test this possibility the dry etched sample

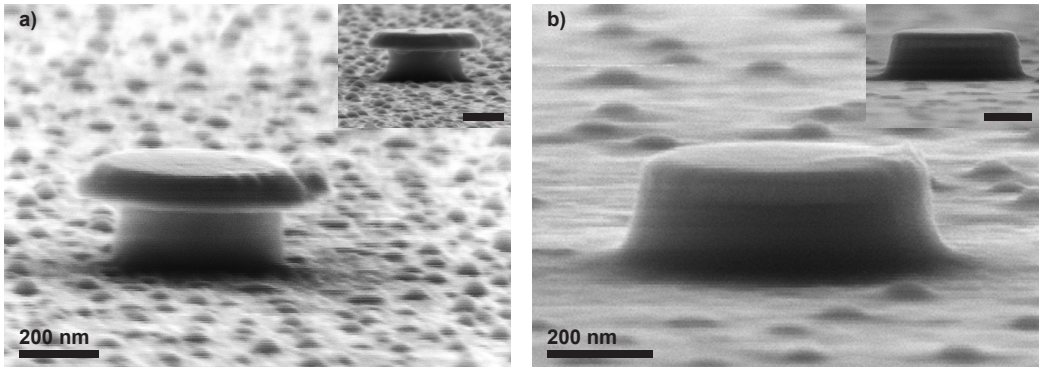

Fig. 4.5: a) Mushroom shaped pillar fabricated by first removing the top metal in IBE mode and then wet etching the semiconductor with chromosulfuric acid for 1 min. b) A submicrometer pillar, etched at 70° angle of incidence by 1st removing the top metal in IBE mode and 2nd etching the semiconductor in CAIBE mode, displays sloped sidewalls at $\sim 83°$ and no trenching at its bottom.

from figure 4.4a is dipped into chromosulfuric acid for 20 sec and the result is presented in figure 4.4b. Although a reduction in lateral pillar size combined with a distinct under cut of the top metal is accomplished, the condition of the mesa, its surrounding area and top metal is concerning. The surrounding surface together with the mesas sidewalls become rough and etching residue is indicated on the top contact metal. An additional 20 sec dip is performed to investigate the development of the mesa's state when further etched with the chromosulfuric acid. Figure 4.4c, displaying the wet etch result more pronounced, shows an unpredictable etching behavior combined with significant unidentified residue on all surfaces. As a consequence from these findings, pillars fabricated from a combination of dry and wet etching as suggested by Austing *et al.* are not applicable to the II-VI heterostructure.

Since the change in surface roughness during wet etching is suspected to arise from the previous ion bombardment and the chemical interaction of the semiconductor with Ar and BCl_3, a new approach is tested. The idea for this test is based on the tilted gate deposition in Kita's work [Kita 08] using the undercut top metal as an shadow mask. In order to apply this idea the top metal is first removed by Ar dry etching in IBE modus stopping about 10 nm into the semiconductor. A subsequent 1 min wet etch dip in chromosulfuric acid is performed, making use of the wet etching isotropy and the ZnSe's etching rate in chromosulfuric acid of about 200 nm/min. The first step ensures that the semiconductor is neither exposed to extreme ion bombardment nor to BCl_3 radicals. Meanwhile the second step on the one hand provides the necessary undercut and on the other hand simultaneously removes just about the required semiconductor material to obtain the necessary height of the pillar. A pillar fabricated following the described process is exemplarily displayed in figure 4.5a and on closer examination two issues arise. Once again the flat sample surface exhibits a high density of bumps most likely arising from the wet etching process and consisting of non soluble etching products, which could

not be determined up to date. Considering the fact that the gate electrode lies separated by an insulator directly onto the highly doped backside contact, these roughness can cause a decrease in gate range due to faster breakdown of the insulator. Additionally, despite the clear undercut Kita's shadow mask method is not applicable to this structure. Since lacking an ideal Schottky barrier the gate metal cannot be applied directly to the semiconductor and the implementation of a gate insulator is required, see chapter 5. This insulator is deposited by PECVD, which results in filling of the created undercut, because the CVD growth mechanism and the small gap under the top metal. Missing an accurate control over the insulator at the structure, the angle for the gate metal evaporation remains undeterminable. Despite the simplicity of this processing step, its implementation in the vQD fabrication is not further pursued.

To fabricate the pillar mesas the process solely based on dry etching is further optimized. From Somkeh's research [Some 76] and confirmed by investigations of Staub [Stau 10] during his experimental Bachelor education the change in angle of incidence from 90° to 70° helps avoiding the trenching at the bottom of the pillar mesa. Furthermore the dry etching process is divided in a IBE step with Ar, which first of all removes the top metal, and is followed by the CAIBE step. In doing so the total exposure of the sample to the BCL_3 radicals is reduces from about 6 min to 1 min, due to the faster etching rates of the metals in the IBE modus. The obtained mesa, displayed in figure 4.5b, has no trenches at its bottom as well as a clean surface. Additionally the steepness of its sidewalls has increased to an angle of about 83° from previously 70° ensuring a better control over the pillar width at the QW level. Based on the achieved improvements this fabrication method is thus integrated in the overall process for vQDs.

Having established an etching sequence to transfer the metal mask as accurately as possible to the semiconductor, the next fabrication step focuses on the electrical optimization of the top contact to insure a low resistance top metal air-bridge post junction. For this purpose the findings regarding the additional evaporation of *ex situ* Ti/Au (10 nm/100 nm) onto to the *in situ* top contact metal obtained during line mesa fabrication 3.2.1, are now implemented in the pillar process step. The first approach is based on evaporating the *ex situ* metal layers in the course of the metal mask preparation within the trenches fabrication step and thus using just a Ti metal mask to define the pillars in the subsequent step. In consequence of the $\sim$ 220 nm evaporated metal the lift off step, see fig.3.7, to remove the metal in the region of the future trenches is considerably impeded. Despite of the steep resist walls the evaporation of the relatively thick three-layer metal mask generates significant coverage of the walls inhibiting the contact between resist and resist stripper during lift off, resulting in a situation similar to the one shown in figure 3.9b. Ultra sonic agitation, which can help to crack these metallic sidewalls, regularly engenders the detachment of the entire top contact metal as already displayed in figure 3.10b.

Based on the mentioned obstacles the additional *ex situ* Ti/Au layers are shifted to the pillar fabrication step in the following. After trenches' fabrication using a single Ti layer, the metal mask defining the pillars, see fig.4.3, consists of the three-layer system 10 nm Ti/100 nm Au/60 nm Ti. As a result of the high amount of evaporated metal

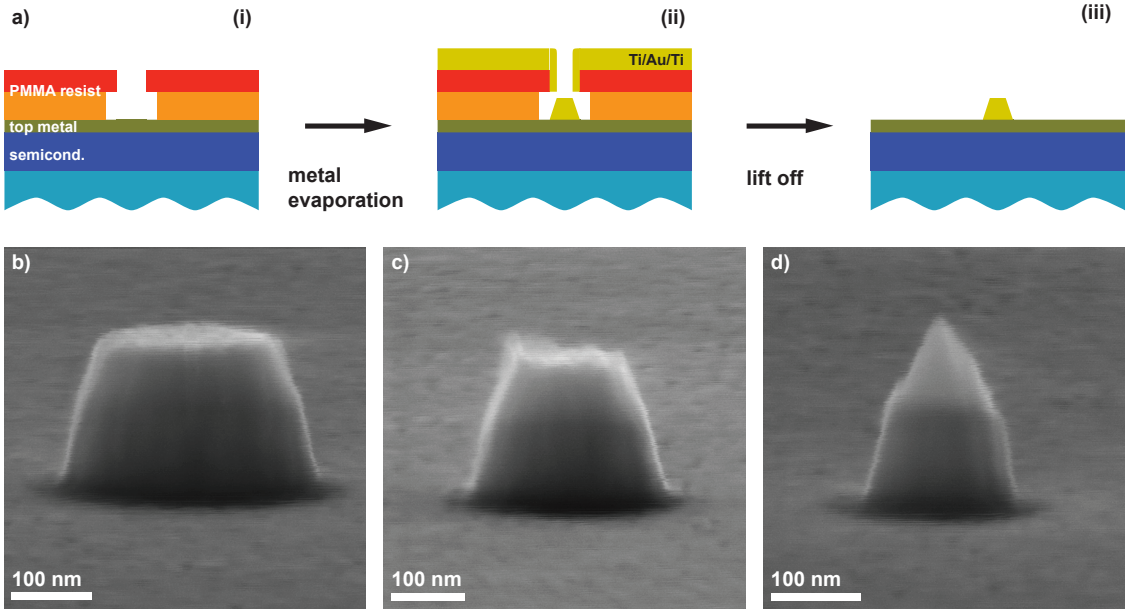

Fig. 4.6: a) Schematic illustration of the sloped mask shaping emerging from the metal deposition on the resist sidewalls especially observable for thick masking layers. SEM micrographs display b) 300 nm, c) 250 nm and d) 150 nm metal masks fabricated from 10 Ti/100 nm Au/60 nm Ti as described in a).

combined with the parasitic metal deposition at the topmost resist layer sidewalls the high metal mask exhibits faceting. This in figure 4.6a schematically depicted effect is revealed by the SEM micrographs in figures 4.6b, 4.6c and 4.6d displaying the resulting mask for diameters ranging from 300 nm down to 150 nm. On the one hand the sidewalls of all these structures are tilted at an angle of $\sim 73°$ and on the other the actual etching mask defined by the topmost 60 nm Ti layer is extremely reduced laterally as well as vertically with decreasing diameter. The former exposes the Au inside the evaporated three-layer metal stack with the result that the masking effect is diminished due to its low selectivity relative to Ti, being 4:1 in IBE mode and 8:1 in CAIBE mode. Therefore the final diameter as well as the shape of the etched pillar are not reliably controllable. The second effect leads to an earlier exposure of the Au to the BCl_3 radicals, which affects the device resistance as explained in chapter 3.2.1. Furthermore the evaporation of the *ex situ* Ti/Au layer during the pillar fabrication step does not rule out the generation of residue at the interface to the *in situ* top metal, inhibiting the device performance.

Moreover during pillar miniaturization and process step optimization the issue of interface cleanness at additional deposited metal layers as well as at the air-bridge post junctions arises. Remembering that the Ti/Au layer for contact strengthening is evaporated prior to fabrication start, a thorough cleaning procedure with hot MIBK and NEP followed by a low power oxygen plasma step to remove any organic residue precedes the metal deposition. This cleaning procedure is always performed after every major process step, if the sample surface is either gold or insulator but not the semiconductor. In the latter case the oxygen plasma treatment is skipped in order to avoid parasitic oxidation of

the submicrometer structures. These cleaning procedures proved to increase the reliability of the electrical contacts at critical interfaces.

Additionally, it becomes apparent that the sequence of wet etch dip and metal mask removal wet etch plays an important role for proper electrical contacts. Figure 4.4 and its findings imply that the wet etch dip performed to remove damaged semiconductor material from the surfaces also leaves behind undesired residue onto the pillars' top contact. Performing the diluted HF dip before the chromosulfuric acid wet etch exposes the top contact Au metal to the residue. For test devices without insulator coverages, this residue cannot be removed and deteriorates the electrical contact. Whereas for insulator covered devices an additional Ar dry etch sequence in IBE mode during insulator removal on the pillar's top contact can sputter away most of the contamination. However a better approach is to first perform the chromosulfuric acid wet etch and subsequently the diluted HF etching step. This way the top Au metal is protected by the Ti metal and does not come in contact with the contamination from the chromosulfuric acid wet etch.

To overcome the aforementioned downsides from metal mask fabrication and interface cleanness the *ex situ* Ti/Au metal layers are evaporated prior to fabrication start after thorough sample cleaning with NEP, MIBK and O_2-plasma. To ensure the correct layer thickness, which is critical for gate alignment later on, control measurements using the Dektak 6M profilometer have been performed. Therefore in the following processing steps both the trenches and the pillar are reliably prepared from Ti metal masks consisting of a single metal layer. The mask for the pillars is transfered to the II-VI heterostructure by dry etching at 70° first in IBE mode with Ar to remove the *in situ* top metal and second in CAIBE mode adding BCl_3 from the gas ring. Subsequently, in order to avoid the presented top contact contamination a wet etch dip in chromosulfuric acid removes ∼30 nm from the damaged semiconductor surfaces and the Ti mask is removed only then by a dip in diluted HF. A schematic of the complete fabrication process is drawn in figure 4.7. Resulting pillars with diameters ranging from 300 nm to 200 nm fabricated by the described process are displayed in figure 4.8.

During the fabrication of devices with and without gate from different substrates stripping of the Ti metal mask by diluted HF from the pillar's top contact proves to be strongly substrate dependent and affecting devices' functionality. From Williams *et al.* findings [Will 96, Will 03] it is well established that Ti and Al have a high etching rate in diluted HF. Although the etch rate of Ti and Al have not been explicitly measured during this work, nevertheless the high etching rate is confirmed repeatedly by the qualitative observation when stripping ∼ 30 nm Ti from flat surfaces within 20 sec using a HF:H_2O (1:200) solution. Despite the isotropy of wet etching, the Al/Ti layers inside the *in situ* top metal contact react more or less with the etchant resulting in a non-observable under cut or a strong one. This situation is visualized by figures 4.9a and 4.9b showing final devices from different substrates, both of which have been fabricated following the exact same recipe. In both samples the trenches have been created by applying a Ti metal mask for dry etching and stripped off by diluted HF at the end of the fabrication step. The subsequent pillar definition by dry etching down to the backside layer reveals the under cut caused by lateral wet etching based on the absence (fig.4.9a) or existence (fig.4.9b) of

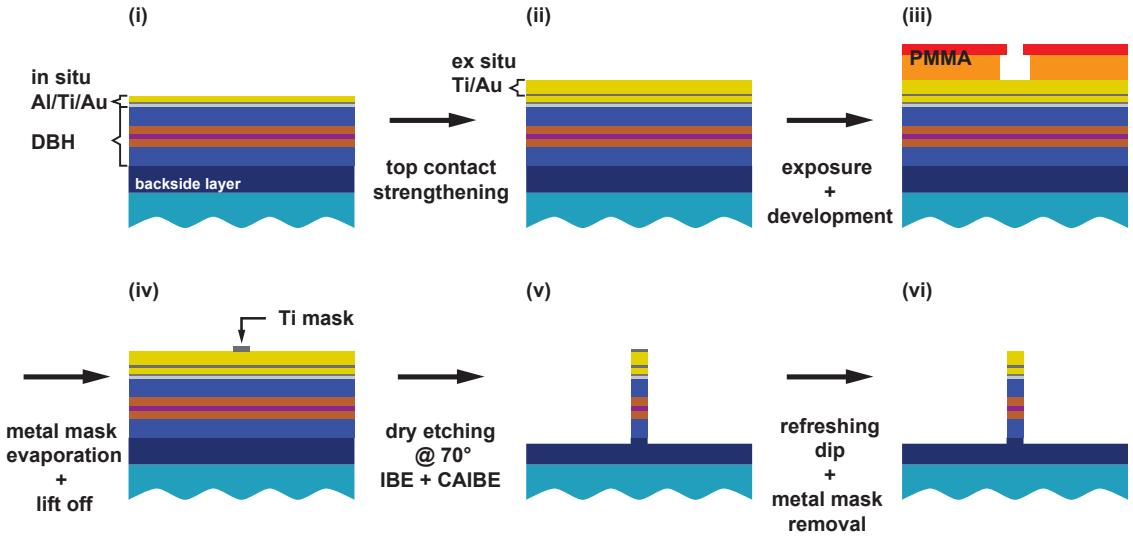

Fig. 4.7: Schematic of the pillar mesa fabrication process using the method of wet etch metal mask removal.

an additional pronounced step at the trench's edge. Figures 4.9b, 4.9c and 4.9d also show the drastic influence of this effect on a few hundred nanometer sized structures. This under cut of the *in situ* Au layer leads either as shown to detachment of the top contact or to non-working top contacts, if the metal remains attached to the semiconductor. The later results form the fact that it is established to apply a *in situ* Al/Ti layer to minimize contact resistance on highly doped n-ZnSe layers [Swan 69, Maxi 04].

To overcome this drastic effect from stripping of the Ti mask using diluted HF and to ensure an electrically working and low resistance top contact, this wet etch dip between steps (v) and (vi) in figure 4.7 is replaced by a new processing step using dry etching in IBE mode, see figure 4.10. After dry etching the pillar, performing the chromosulfuric acid

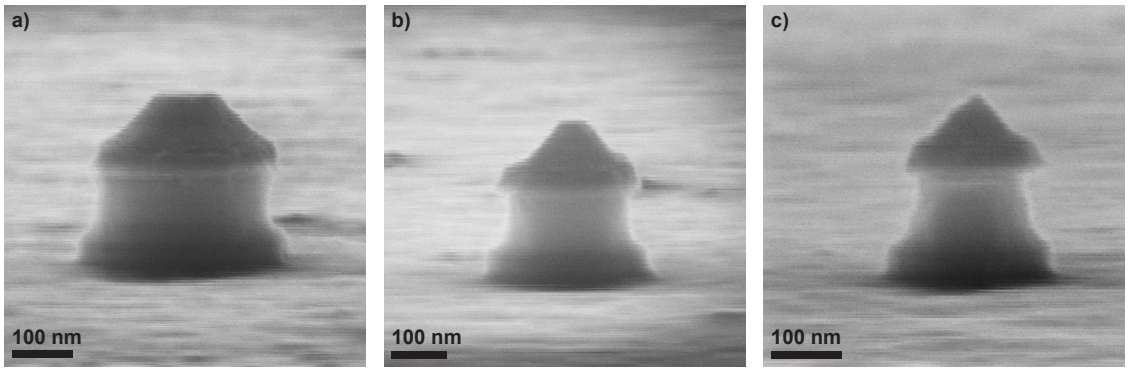

Fig. 4.8: Pillars of a) 300 nm, b) 250 nm and c) 200 nm diameter and ~260 nm height are fabricated by first removing the top metal in IBE mode, subsequently etching the semiconductor in CAIBE mode, followed by a surface refreshing dip in chromosulfuric acid and stripping of the Ti mask using diluted HF.

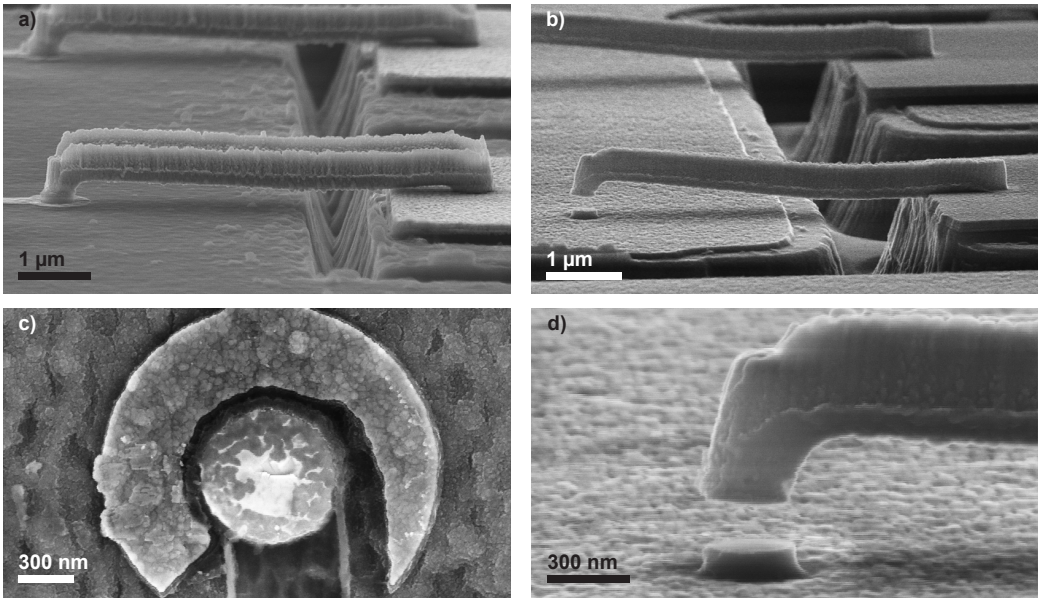

Fig. 4.9: a) A Final gated device fabricated from a wafer where no noticeable under cut from lateral etching of Al/Ti by diluted HF occurs. b) A Final non-gated device with detached top contact fabricated from a wafer where distinct under cut at the trenches' edge caused by lateral etching of Al/Ti by diluted HF is visible. c) The top view of a top contact missing device displays the severe under cut. d) A zoom of the non-gated device with detached top contact shows no Al/Ti metal left on the semiconductor surface.

dip and adding the backside contact by optical lithography, the excess Ti metal remains on the pillars top. In the following once again the previous three-layer resist system from 600K (4%)/600K (4%)/950K (3%) is spun on at 6000 rpm. With a total thickness of ∼410 nm it completely covers the pillar mesa of 250 to 280 nm height, depending on the previously chosen etching time. By exposing and developing a small rectangle the resist thickness during the subsequent fabrication steps can be monitored applying the Dektak profilometer. The resist mask is then thinned to about 50 to 80 nm below the pillar top by exposing the sample to a low power oxygen plasma in a RIE system. A subsequent ∼1 min Ar IBE step at 70° sputters the excess Ti metal from the pillar's top contact leaving behind a clean and non-contaminated Au surface. By immersing the sample in hot NEP and MIBK the resist is stripped off, the devices are cleaned and ready for the following processing steps. The described process step order applies for samples without insulator and gate. For gated samples the aforementioned procedure is best performed after the insulator has been removed from the pillar's top contact. This way a low power oxygen plasma can be added after the NEP/MIBK cleaning step to remove any organic residue, since the sample surface is protected by insulator and no oxidation of the semiconductor can occur.

Applying the described procedures and also performing the necessary cleaning steps devices with well working electrical contacts are fabricated.

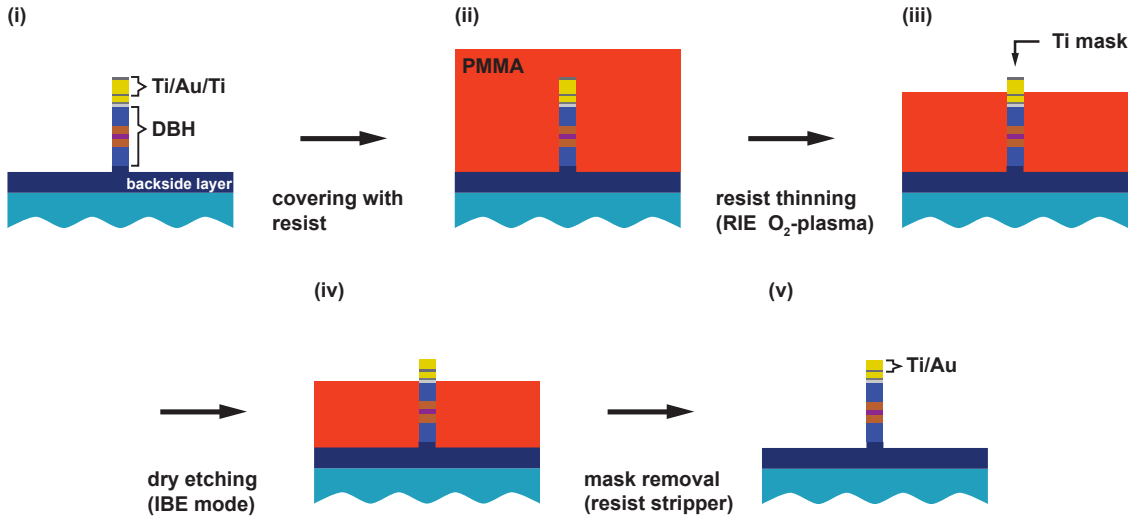

Fig. 4.10: Schematic of the alternative dry etch metal mask removal technique for Ti mask removal by IBE which uses a thinned resist mask for mesa and semiconductor protection.

4.2 Results of pillar mesa miniaturization

The findings of the presented pillar mesa fabrication methods are accompanied by the simultaneous miniaturization of the pillar mesa and the fabrication of fully functional devices, which are then electrically tested. In the following the results on pillar miniaturization are presented dependent on the fabrication method applied in each case.

Based on the discussion in chapter *2* it is known that for the fabrication of artificial atoms it is preferable to use RTD structures whose 2D resonant level is positioned at or below the Fermi energy. In figure 4.11 measurements are displayed of 100 μm $\times$ 100 μm pillars from two wafers used both for test devices and the final devices presented in chapter *6*. The heterostructure's nominal values for both wafers are identical except for the Cd content in the well which is 7.6 % for wafer I and 6.5 % for wafer II. This fact is well

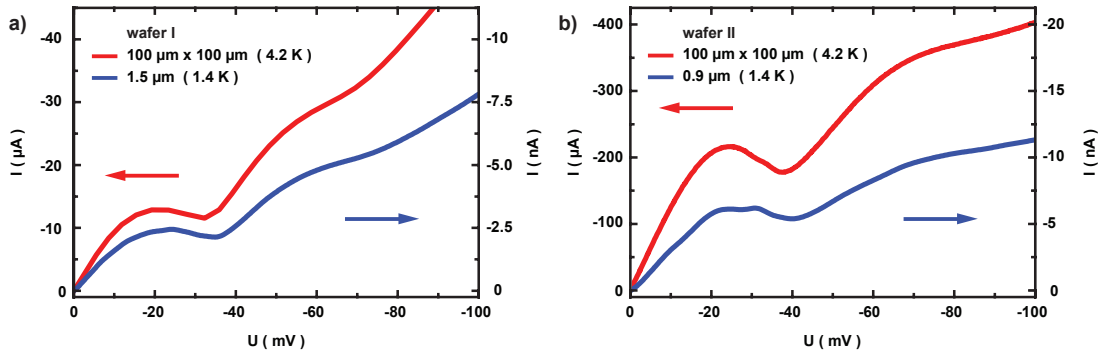

Fig. 4.11: I-U measurements of a 100 μm $\times$ 100 μm characterization RTD structures and micrometer sized RTD structures of Ø 1.5 μm and 0.9 μm fabricated from a) wafer I and b) wafer II.

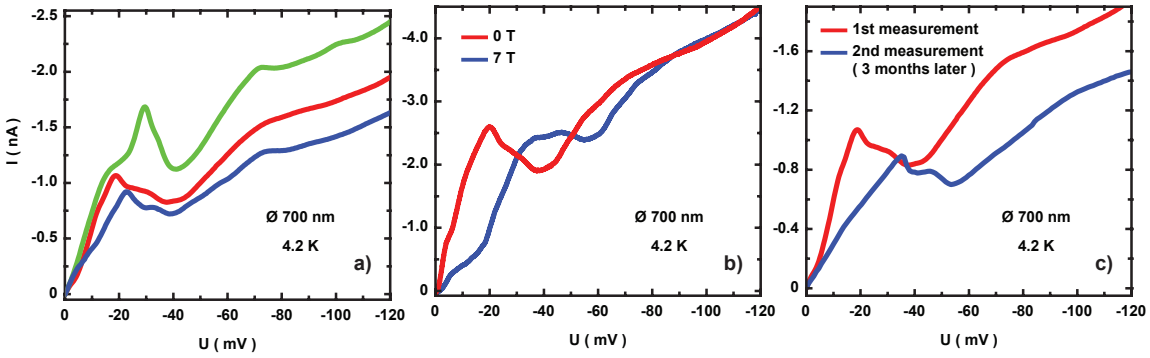

Fig. 4.12: a) I-U curves from pillars of 700 nm diameter fabricated from wafer II dry etched at 90◦ and the Ti mask removed prior to the chromosulfuric wet etch dip. b) I-U measurements of a 700nm pillar at 0 T and 7 T. c) I-U measurements of a 700 nm pillar recorded at an interval of 3 months showing the degradation due to oxidation.

observable in the displayed measurements such that the maximum of the current peak of wafer I is lower as the one of wafer II, as expected from an energetically lower conductor band edge. The difference in current arises from fluctuations during growth despite of aiming at nominally identical values. Figure 4.11 also shows measurements at 1.4 K of micrometer sized devices following the process of T. Borzenko [Borz 05], briefly presented in the previous section and the steps shown in figure 4.1. While for the 1.5 μm device the I-U curve exhibits no difference in shape to the big RTD, the 0.9 μm device however has additional structure. These new features originate from the beginning quantization in the x-y-plane of the QW. Due to the in the previous section mentioned downsides of this process, the fabrication of submicrometer sized pillars is switched to a metal mask one.

The first approach consists of dry etching the pillars using a single etching step at 90° in CAIBE mode. The excess Ti is removed by a short dip in diluted HF:H_2O (1:200) and subsequently the damaged semiconductor surface is removed also by a short dip in chromosulfuric acid. Then the pillars are contacted by air-bridges applying the technique described in chapter 3.2.3. Figure 4.12a shows I-U curves from different 700 nm diameter pillars fabricated in this manner from wafer II. Despite the difference in current through the structures, all of them indicate increasing confinement in the QW plane, since the resonance peak exhibits new features and its shape is distinctively modified. The comparison of a I-U measurement at 0 T to a I-U curve recorded at a field of 7 T parallel to the current through the pillar (fig.4.12b) indicates that both the magnetic properties of the QW are still existent and the additional structure is strongly magnetic field dependent. Due to the residue on the top metal after the chromosulfuric acid dip as well as the under cut of the *in situ* Al/Ti metal devices with pillar diameter < 700 nm did not worked. Additionally it has been observed that after the sample has been exposed to air for about two months most of the devices are not working anymore. For the working ones the I-U curve is changed as shown in figure 4.12c and indicates the addition of an extra series resistance. Following the findings of Rüth's RTD modeling [Ruth 11a] an additional series

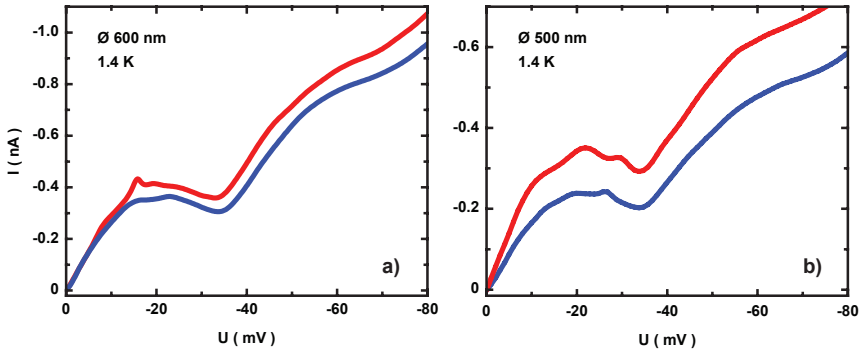

Fig. 4.13: I-U measurements of pillars with Ø of a) 600 nm and b) 500 nm from wafer I fabricated by first adding the air-bridges just after metal mask removal and then performing the chromosulfuric wet etch dip.

resistance on the one hand shifts the resonance to higher bias voltages and on the other simultaneously tilts it in the way shown in figure 4.12c. It is suspected that the reason for the change in electrical behavior is based on the oxidation of the under cut Al/Ti metal, when the sample is exposed to air for a longer period.

In order to avoid oxidation of the *in situ* metal from long period exposure to air, the process is changed such that samples with final devices where covered by insulator material in the following. Furthermore the processing has been switched to wafer I, which is barely subjected to under cut of the *in situ* Al/Ti, see figure 4.8a, and thus the fabrication technique using the dip in diluted HF for Ti mask removal can still be applied. As a first step after dry etching the pillars the metal mask is removed by the wet etch dip and the air-bridges are immediately fabricated. Prior to backside contact optical lithography and subsequent insulator deposition, the chromosulfuric acid dip is performed. This way the pillars' top contact is protected against contamination from the wet etch dip. Following this recipe pillars with diameters ranging from 600 nm and 500 nm are fabricated. The low temperature measurements performed on such pillars are presented in figure 4.13

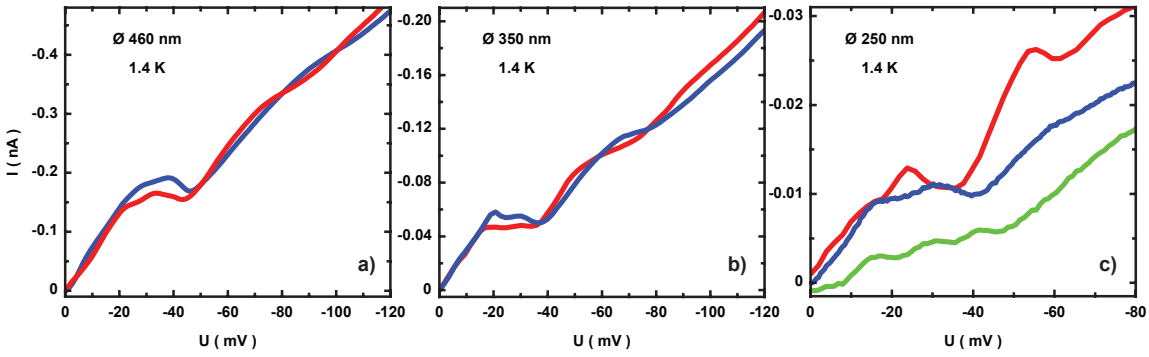

Fig. 4.14: I-U curves of pillars with Ø of a) 450 nm, b) 350 nm and c) 250 nm from wafer I fabricated following the the recipe from figure 4.7 and showing increasing confinement with decreasing pillar size.

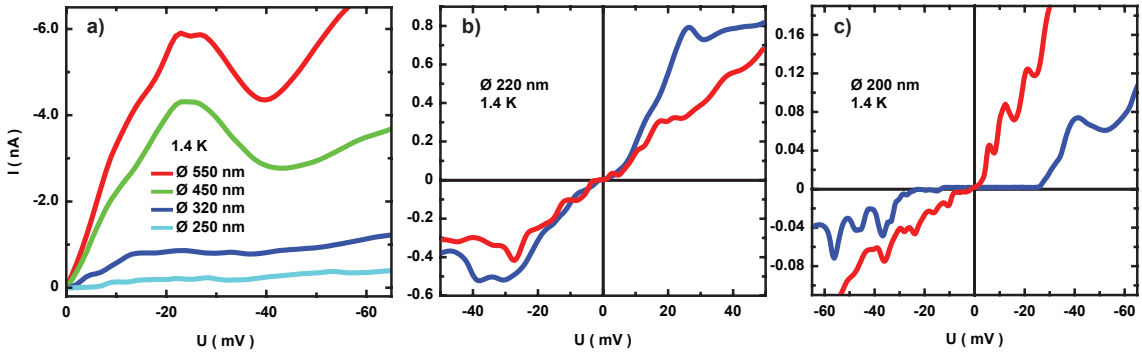

Fig. 4.15: a) I-U curves of pillars from wafer II fabricated applying the method of metal mask removal by dry etching presented in figure 4.10. I-U measurements of pillars with Ø of b) 220 nm and c) 200 nm from wafer II fabricated with the same method and showing strong confinement.

and again starting quantization is observable. Since at this stage the development of the gating technology also started, see chapter 5, the fabrication step has to be changed as a result.

In the following and final fabrication process for the method of wet etch metal mask removal (fig.4.7), meaning the excess Ti mask is removed by a diluted HF dip, the insulator is laid down before gate and air-bridge fabrication. By applying this way of processing the pillar diameters are further decreased from 450 nm down to 250 nm, where together with the proper gate technology the observation of atomic like behavior becomes possible. Figure 4.14 displays I-U measurements of devices with diameters of 450 nm, 350 nm and 250 nm indicating the increasing 3D confinement and the formation of a vQDot.

Given the findings from the pillar miniaturization on wafer I the process is then transfered to wafer II, which exhibits higher currents and thus facilitates measurements less influenced from shot noise. From the SEM micrograph in figure 4.8b displaying a device from wafer II, fabricated by the wet etch metal mask removal technique, it is obvious that the *in situ* Al/Ti is completely removed at the top contact. This under cut leads to non ohmic contacts or to the detachment of the top metal, as shown by the SEM micrograph, and thus these devices don't work. Therefore the wet etch metal mask method is replaced by the alternative newly developed technique dry etch metal mask removal presented in the previous section and schematically displayed in figure 4.10. Figure 4.15a shows I-U curves of non-gated devices with diameters from 550 nm down to 250 nm, once again indicating the increasing 3D confinement in the heterostructure and the formation of a vQDot. Implementing the developed gating technique working devices with pillars of 230 nm and 200 nm, shown in figures 4.15b and 4.15c with clearly observable 3D confinement can be prepared.

Chapter 5

Gate technology

In order to investigate the physical properties of artificial atoms formed in a semiconductor it is necessary to be able to actively influence the discrete energy levels of the 0D object. This is best achieved by adding a third electrode, the gate electrode, to the previously developed two terminal device. Based on the reduced II-VI-semiconductor to metal Schottky properties a dielectric material is required to separate the gate metal from the semiconductor and enable reliable device functionality. In the following the development of an adequate gating technology for the aforementioned vQDots from vertical pillars is presented. The first part of this chapter concentrates on the investigation of the insulating properties of the dielectrics SiO_2 and Si_3N_4 deposited by PECVD. Then the development of an adequate gate design and its fabrication is described considering the application of a thin layer of insulating material as well as the accurate alignment of the gate electrode to the QW. In the end the investigation of the gate's electrical performance is presented as well as the results from misalignment and leaking dielectric material.

5.1 Insulator

In 1986 Thornton *et al.* [Thor 86] suggested the use of metal Schottky contacts on top of a 2DEG heterostructure to define a narrow channel by depleting the underlying semiconductor. This technique also allows the formation of islands in the 2DEG [Meir 90] and the development of fully tunable lateral QDs [Goul 98, Cior 00]. For vertical DBH this method was first applied by Kinard *et al.* [Kina 90], Dellow *et al.* [Dell 91] and Gueret *et al.* [Guer 92b] in the early 1990's. By closely placing the pillar surrounding gate electrode on the semiconductor material above the barrier the lateral confinement in the QW results from the depletion from the Schottky contact. In this design [Dell 92b] the depletion is asymmetric at the DBH in growth direction and creates a non-uniform conducting channel. This issue is overcome by Austing *et al.* [Aust 96] by modifying the gating method. In their approach the gate electrode is applied directly at the DBH of the pillar, enabling the study of fully tunable vertical QDs from vertical RTD. As one can see all devices forming QDots from the GaAs/AlGaAs material system have in common that gating is provided by the application of one or more metal Schottky contacts.

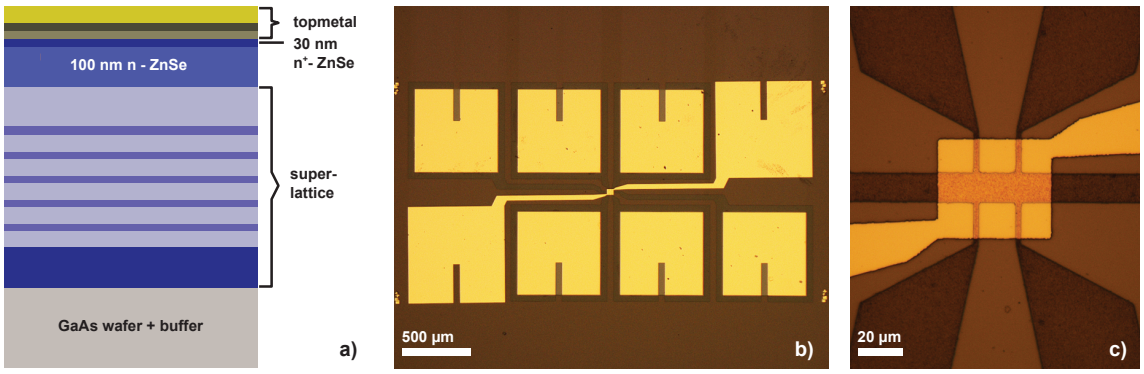

Fig. 5.1: a) The semiconductor heterostructure containing a 100 nm middle-doped ZnSe layer used to investigate the dielectric properties by Hall measurements. b) Top view of the entire gated Hall bar structure and c) a close view on the active region of the device.

For the ZnSe material system gating by means of metal Schottky contacts is however not applicable. Since the late 1960's many attempts have been made to understand and improve metal-ZnSe Schottky barriers [Swan 69, Mach 74, Tyag 75, Nede 77, Chot 82, Dhar 98]. But although nearly ideal Schottky barriers have been claimed [Tyag 75], the semiconductor preparation is not compatible at all with any device fabrication. The described wet etch process for surfaces preparation consists of a several minutes lasting immersion in 1% solution of bromine in methanol (BM) followed by a short dip in hot NaOH. On the one hand the application of BM as suggested results in the excessive removal of II-VI semiconductor, because of its high etch rate [Liu 95]. This fact has a crucial impact on critical device parameters. On the other hand the hot NaOH attacks the Al metal of the top contact leading to its detachment. Furthermore when optimizing the metal-ZnSe Schottky contacts the main focus concentrated on the forward bias region as opposed to the reverse voltage in which the gate electrode is operated in the QDot devices. In reverse bias configuration Tyagi *et al.* [Tyag 75] observe surface leakage and edge effects to be responsible for a reverse current several orders of magnitude larger than expected from thermionic emission theory. Based on this the fabrication of the gate electrode requires the implementation of an insulating layer to avoid parasitic leakage currents.

Due to the 3D topography of the sample a conformal coating of all device's facets is required when adding an insulator. For this purpose the use of the available plasma enhanced chemical vapor deposition (PECVD) of SiO_2 and Si_3N_4 is chosen. The chemical reactions for depositing SiO_2 and Si_3N_4 are shown by equations (5.1) and (5.2).

$$SiH_4 + 2N_2O \longrightarrow SiO_2 + 2N_2 + 2H_2 \tag{5.1}$$

$$3SiH_4 + 4NH_3 \longrightarrow Si_3N_4 + 12H_2 \tag{5.2}$$

In contrast to evaporation or sputtering methods, which are directional, the PECVD provides the necessary isotropy during material deposition. In order to gain some insight into the SiO_2 and Si_3N_4 insulators provided by the available PECVD equipment, these

film	SiO_2			Si_3N_4	
thickness	1st U^-_{Break}(V)	2nd U^-_{Break}(V)	U^+_{Break}(V)	U^-_{Break}(V)	U^+_{Break}(V)
50 nm	-8	-6	2	-9	3
100 nm	-15	-10	3	-17	6
150 nm	-17	-8	8	-33	20

Tab. 5.1: Breakdown voltages recorded at 4.2 K for insulator films of 50 nm, 100 nm and 150 nm from SiO_2 and Si_3N_4 deposited on Hall bars.

two materials have been investigated by Krammel [Kram 10] and Schäfer [Scha 10] during their Bachelor work in terms of breakdown voltage, hysteresis and dielectric constant.

As a testbed to investigate the insulator properties the II-VI heterostructure shown in figure 5.1a is chosen. On top of the superlattice a medium doped 5×10^{18} cm^{-3} 100 nm thick layer is grown, which is used for gated Hall transport measurements. A cap of 30 nm 2×10^{19} cm^{-3} highly doped ZnSe ensures ohmic contact to the *in situ* evaporated Al / Ti / Au (10 nm / 10 nm / 30 m) metal layers. By optical lithography and lift-off the contact pads are defined at first, then the *in situ metal* is removed by a wet etch. In the following the Hall bar mesa is dry etched by CAIBE applying again a Ti metal mask and the high doped ZnSe layer is removed by a wet etch dip at last. The entire sample is inserted into the PECVD system and covered with the desired insulator at 200°C. After fabricating the gate electrode by optical lithography and lift-off, the insulator on the contact pads is removed by dry etching in RIE applying a optical resist mask. Figures 5.1b and 5.1c display the entire final test device as well as a zoom into its active region.

For leakage and breakdown measurements the voltage across the insulator is swept by contacting the gate and the current leads, which are grounded. The voltage drop at a 100 MΩ resistor in series with the sample is recorded enabling the determination of the leakage current through the sample. The results obtained from these experiments are summarized in Table 5.1 for both insulators and different film thicknesses. First, the thin films from Si_3N_4 exhibit a higher U^-_{Break}(V) and U^+_{Break}(V) voltage than the SiO_2 films. Second, for all SiO_2 films the U^-_{Break}(V) is considerably reduced permanently after a first breakdown. In these samples the measured current densities at 1 V have an upper limit of 1.2×10^{-6} A/cm^2 for SiO_2 and 1.5×10^{-6} A/cm^2 for Si_3N_4.

Having determined the applicable voltage range to the gate, Hall measurements in either constant gate or constant B-field mode at 6 T are performed in the following. The goal is on the one hand to study the gate efficiency, meaning the deviation of the dielectric constant from its know value for each material, and on the other to investigate conceivably occurring hysteresis. In figure 5.2 the carrier density vs. U_{Gate} results for both insulators are presented and from the graphs' comparison immediately a distinct difference becomes apparent. While for SiO_2 the down and up U_{Gate} sweeps at B = 6 T are linear and overlapping, the Si_3N_4 film exhibits a pronounced hysteresis. On the basis of the change in carrier densities and assuming a simple plate capacitor model the dielectric constants from different samples are determined. For SiO_2 the test samples exhibited dielectric constants between 3.1 and 3.6. While the thermal oxide is typically denoted with a value

of $\sim$ 3.9, SiO_2 films from PECVD systems have usually dielectric constants of about 3.5 [Albe 05]. For Si_3N_4 the dielectric constant of the test samples is spreading over a wide range from 5 to 9. As shown by Albertin's *et al.* [Albe 05] research by varying the N_2O/SiH_4 flow ratio the composition of the SiO_xN_y film can be changed from SiO_2 to Si_3N_4 which also results in a change of the film's dielectric properties. Based on this the observed variation in dielectric constant for Si_3N_4 films might be attributed to fluctuation during different depositions as well as incorporation of H in the film [Samu 82].

The observed hysteresis for Si_3N_4 is most likely caused by interface states between the insulator and the semiconductor as well as traps within the insulator. In the regions of small slope the filling (lower branch) or emptying (upper branch) of the traps takes place and the gate influence is diminished. Hinz *et al.* [Hinz 06] reported on similar observation when depositing a SiO_2/Si_3N_4 insulator superlattice for gating onto a HgTe/HgCdTe heterostructure. From the maximal hysteresis a trap density of $\sim 2.1 \times 10^{17}$ cm^{-3} is deduced which is typical for silicon nitride thin films [Park 90, Park 93].

Figure 5.3 displays further investigations of the hysteresis. First the occurrence of hysteresis is explored when the starting point for up and down U_{Gate} sweeps is in the trap filling region. From figure 5.3a it is noticeable that up and down sweeps are almost indistinguishable as long as they don't return to the trap filling region (lower branch) of the envelope hysteresis. This means that measurements performed with the same filled trap configuration are reproducible and can be compared to each other easily in contrast to measurements performed at a different trap configuration. Furthermore figure 5.3b emphasizes on the one hand the existence of traps and on the other the importance of a required waiting time to ensure similar trap configurations in different measurements. At two points of the envelope hysteresis (U_{Gate} = -1.5 V and -6 V) the cyclic measurements have been interrupted for different amount of time. In both cases the measurements after longer waiting times are shifted towards more negative gate values indicating that the filling of the traps requires a certain period. Assuming an exponential decay of the filling, the filling constant τ is estimated to be $\sim$ 94 s.

In summary it can be concluded that from the presented observations three points have to be remembered when measurements are performed on samples with PECVD

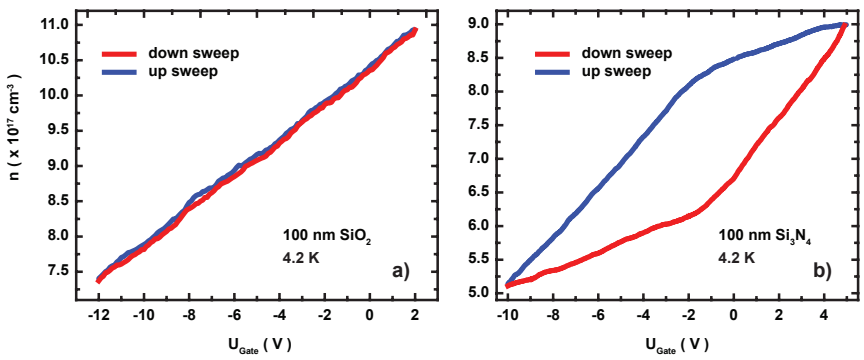

Fig. 5.2: The change in carrier density for a) 100 nm SiO_2 and b) 100 nm Si_3N_4 as the gate voltage is swept exhibiting a) no hysteresis for SiO_2 and b) clear hysteresis for Si_3N_4.

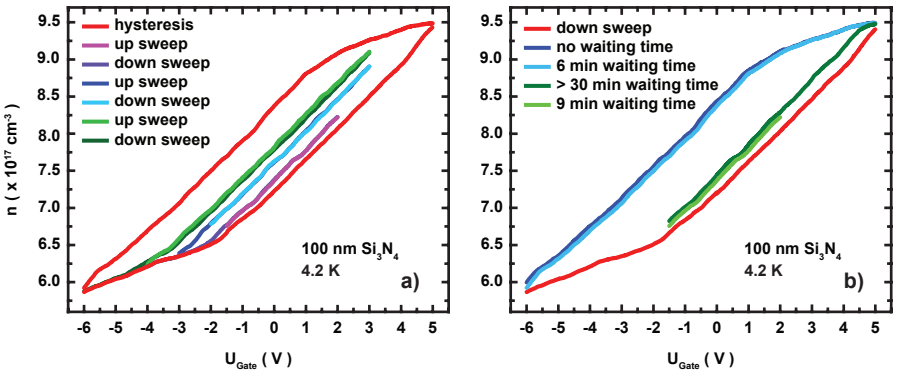

Fig. 5.3: a) Up and down U_{Gate}-sweeps for different charging of the semiconductor insulator interface traps. b) Influence of the charging on the hysteresis dependent on the waiting time at critical points.

deposited insulators. First, measurements on samples containing the Si_3N_4 insulator differ dependent on the sweep direction because of the occurring hysteresis. Second, the history of the U_{Gate} sweep has to be accounted for, when measurements are performed and compared. And third, a waiting time before each measurement is required to ensure similar filling of the traps.

5.2 Gating technique

The application of a gate insulator a solid gate design and gate alignment to the few hundred nanometer pillar mesas is developed in the following. Furthermore the conformal coverage of the sample by the insulating material necessitates proper etching methods to remove it from contacts. In order to electrically contact the gate electrode electrically and mechanically reliable bonding contacts are engineered as well. Finally different experimental results from various gating attempts during the development of the gating process are compared.

5.2.1 Gate designs and fabrication

In the course of this thesis various attempts to add a gating electrode to a heterostructure or pillar mesa containing a DBH have been briefly mentioned. Figure 5.4 summarizes once again the different approaches. First, the simplest gating attempt presented by Kinard *et al.* [Kina 90], Dellow *et al.* [Dell 91] and Gueret *et al.* [Guer 92b] has been by depositing a metal electrode above the DBH and as near as possible to the pillar, as shown in figure 5.4a. From the depletion caused by this Schottky contact the lateral confinement in the QW of the DBH is influenced. To overcome the asymmetry of the depletion at the QW level Austing *et al.* [Aust 96] first dry etch below the DBH and second create an under cut by a short wet etch. This enables the self alignment of the Schottky electrode at the QW level when the gate metal is then evaporated, displayed schematically in figure

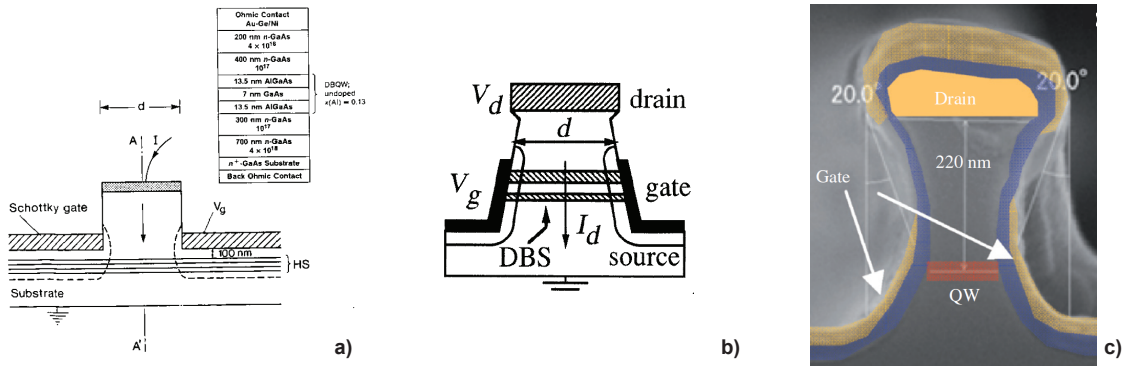

Fig. 5.4: Different gating approaches by depositing a) a Schottky contact above the DBH [Kina 90, Dell 91, Guer 92b], b) a self-aligned Schottky contact directly at the DBH [Aust 96] and c) a insulator separated gate electrode directly at the DBH by means of shadow evaporation [Kita 08].

5.4b. For the (In,Ga)As material system Kita *et al.* [Kita 08] follow this technique with additionally depositing a necessary gate insulator. As shown by figure 5.4c, in order to properly align the gate electrode with the QW tilted metal evaporation at $\sim 20°$ is essential. All layer structures in these designs have one characteristic in common: the source and drain leads, meaning the semiconductor heterostructure below and above the DBH, consist of several hundred nanometer thick low doped semiconductor material, as indicated in the publications on which figure 5.4 is based. For the structure in figure 5.4a the low doped layer acts as a spacer to the DBH. In figures 5.4b and 5.4c these thick leads facilitate the creation of the necessary under cut to apply the shadowed evaporation and position the gate electrode at the DBH level.

When the entire III-V heterostructure is compared to the II-VI one, depicted in figure 2.3 and used in this thesis, two important differences, already mentioned in previous chapters, bear repeating. First, the backside layer is not situated at the back surface of the wafer but is part of the II-VI layer structure. This fact requires its sectioning to separate the bonding contacts as discussed in chapter 3.1. Taking into account the second issue of 20 nm and 25 nm thin leads, below and above the DBH, it is situated in the proximity of the QW. Therefore the gate electrode is, though separated by insulating material, always placed on top of this highly doped layer enhancing any influence from leakage. Based on the second issue of thin leads neither the Austing nor the Kita approach can be implemented in the fabrication process, since the essential under cut necessary for shadowed metal evaporation is not feasible, as presented in chapter 4.1 on pillar fabrication. Furthermore, given the band structure of the RTD device's heterostructure [Frey 10b, Ruth 11a] the electron puddles before and after the DBH can easily be extremely influenced by gate electrodes. For this reason the Kinard/Dellow/Gueret idea (see fig.5.4a), even with the implementation of an insulating material, is not applicable to the II-VI system.

A new design and mounting method for the gate electrode is therefore necessary. The new design requires the gate electrode to be situated as accurately as possible at the

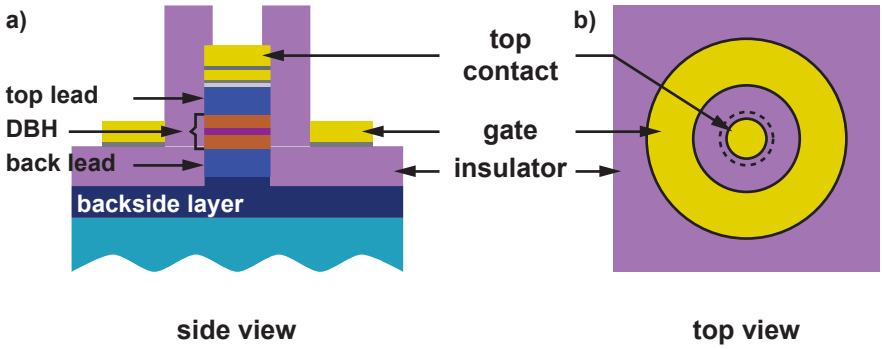

Fig. 5.5: Layout of the proposed gating method shown in a) side and b) top view.

QW level and its thickness to be smaller than the DBH itself. This way the parasitic influence to the electron puddles of the thin leads is minimized and the gating effect at the QW level maximized. In order to accomplish these stringent requirements the reliable dry etching CAIBE process and exact deposition of insulator material are exploited. By reliable etching to a predetermined level into the backside layer with an accuracy of ± 5 nm and subsequently depositing the necessary thickness of insulator, based on the known deposition rate, the gate electrode is placed at the QW level with great precision. A side view of a gated structure fabricated on the basis of this technique is schematically depicted in figure 5.5a. Using the e-beam lithographic metal mask fabrication step for pillars, see figure 4.3, the gate electrode is fitted with great accuracy to the pillar, schematically shown by the top view in figure 5.5b. While the suggested gating process has already been implemented in the entire device fabrication, a similar approach has been published by Wensorra *et al.* [Wens 09] on resonant tunneling transistors from the GaAs/AlGaAs material system with thin heterostructure leads. On the one hand this fact confirms the validity of the chosen gating approach. On the other hand the gating method of this thesis, in contrast to the one by Wensorra *et al.* which uses hydrogen silsesquioxane as insulator, is more universal in terms of insulator application for sample fabrication. The presented technique requires only the knowledge of the insulator's deposition rate, but does not constrain its type, and avoids any influence on the semiconductor material from dry or wet etching steps.

The outline in figure 5.5b suggests the fabrication of a donut shaped gate electrode. From tests performed to determine the correct exposure parameters for this type of gate conflicting results have been obtained. Despite many lithographically clean structures as shown by figure 5.6a there are also a large number of structures similar to the one in figure 5.6b. For the later situation when the lift-off step is conducted the metal on top of the central resist pillar is not properly removed from the structure, it slides down to the surface and sticks to it. In the case of figure 5.6c where this situation occurred when a device has been fabricated, the metal cap shortens the top contact and the gate, rendering the structure unusable.

In order to avoid the parasitic metal cap instead of the closed donut a fork design

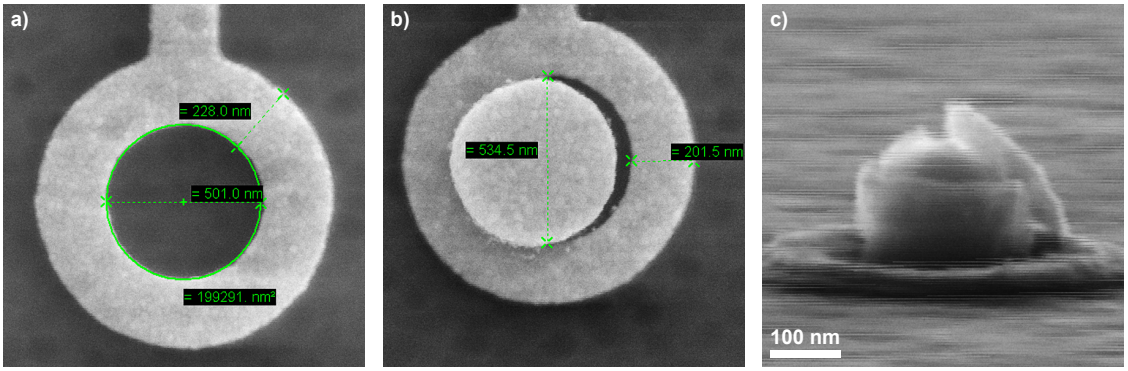

Fig. 5.6: SEM micrographs of a) a donut shaped gate electrode, b) a gate electrode with the metal cap of the hole not properly removed during lift-off and c) a pillar with a fitted annular gate electrode and the metal cap of the hole not properly removed during lift-off.

is investigated and applied. By leaving out a piece of the gate donut, the metal on the resist inside the ring is now connected to the metal outside the ring facilitating a reliable lift-off step. Figure 5.7a presents a test from the described design in which a ∼20° break is built in. In figure 5.7c an insulator covered pillar is perfectly fitted with this type of fork gate. In order to mount the gate electrode as accurately as possible to the pillar a multi step procedure is used. First, it starts with the fabrication of a new pair of alignment marks simultaneously with the definition of the pillars. This way the error accumulated from previous lithography steps is avoided. Second, about 4 to 5 additional pillars, called dummy structures, are added to the structure for testing purposes. These dummy structures are then used in the following for a first gate fit by performing the gate fabrication step just on these structures. In the following these dummy structures are inspected with the SEM and any misalignment, shown in figure 5.7b, is recorded. From the determined deviation the design in the CAD program is modified such that a optimal

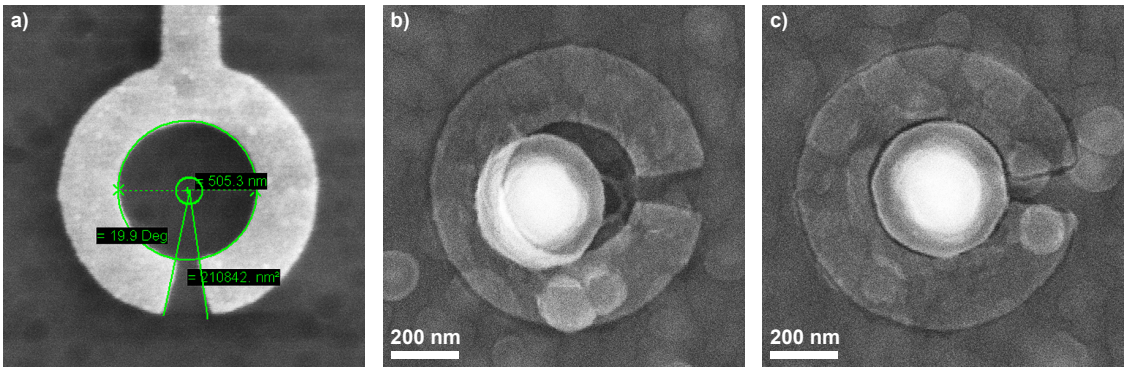

Fig. 5.7: SEM micrographs of a) the annular gate electrode with a 20° notch for more reliable lift-off, b) a displaced gate electrode due to a systematic offset during the EBL and c) a pillar with a perfectly aligned gate electrode after the systematic offset has been corrected in the EBL file.

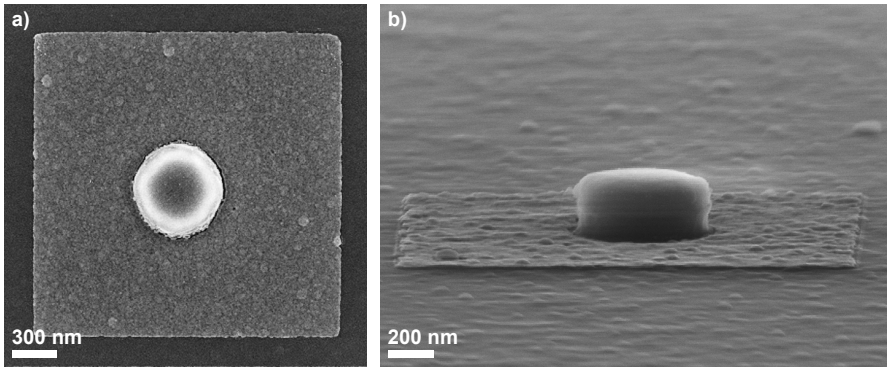

Fig. 5.8: SEM micrographs: a) top and b) side view of a insulator covered pillar gated by the planar gate technique. Here the gate metal on the pillar's top has already been removed.

gate fit is achieved. Furthermore at the start of each e-beam lithography step a reset of the stage is required in order to remove the accumulated errors from previous work.

In case that the misalignment determined from the dummy structures is not systematic and cannot be removed by the described procedure a third option remains: the planar gate approach. Since the pillar's sidewalls are quite steep, a square or round shaped area around the pillar is exposed and the gate metal is evaporated, generating the result displayed in figure 5.8a. As can be seen from the side view micrograph in figure 5.8b for conformal coverage with insulator the gate is closely aligned to the pillar. The excess metal on the pillar top and on its side walls is then removed by the resist mask dry etching process presented in figure 4.10 from chapter 4.1. This way a metal free insulator surface onto the pillar is achieved and the gate electrode is protected from any damage, as shown by figure 5.8b.

Having established the alignment and design of the gate electrode, the next step is to implement it in the fabrication of the three terminal devices. As previously mentioned in chapter 4.2 the first attempt in gating sub micrometer sized pillars consists of adding the gate electrode at the end of the fabrication process. After the pillar has been etched, the backside contact as well as the top contact air-bridge added and the entire sample covered with insulator of necessary thickness, the gate and its bonding contacts are exposed as well as finally connected to each other by air-bridges. Some results from this fabrication sequence are displayed in figure 5.9 and emphasize two issues arising in this case. For structural stability the fabricated air-bridges have a width of 500 nm, similar to the diameter of the connected pillar, and the width is further increased by covering the sample with insulator. This widening leads to shadowing and inhibits a narrow attachment of the gate electrode, when the metal is evaporated. Furthermore based on figure 5.9b it is clearly visible that the bridge inhibits the attachment of the gate along half the circumference of the pillar and the necessary confinement is not achievable. Since the pillar size has to be further decreased, as presented in chapter 4.2, and at the same time the bridge span width cannot be scaled similarly, the gate coverage is drastically diminished and thus the ability to achieve the required confinement.

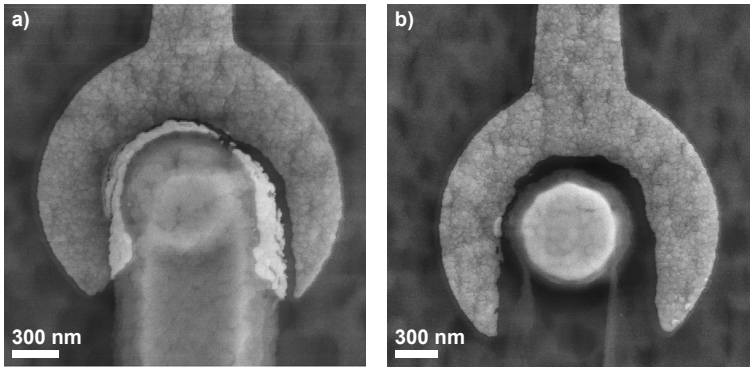

Fig. 5.9: SEM micrograph of a) a device to which the gate electrode has been added after air-bridge fabrication and coverage with insulator and b) a similarly fabricated device with missing air-bridge showing the bad fitting of the gate electrode.

The solution to overcome this obstacle for pillars ≤ 500 nm is to rearrange the process steps. Right after pillar and backside contact fabrication first the insulator is deposited and then the gate electrode is lithographically added. In the following the insulator on the pillar's top contact as well as the bonding pads has to be reliably removed and then the air-bridges added. Figure 5.10a displays a 450 nm pillar fitted with a gate and the insulator on its top contact removed. The top view micrograph in figure 5.10b shows in contrast to figure 5.9b that now the gate can be fitted to the pillar without restrictions. Finally the complete structure consisting of an insulator covered pillar fitted with an annular gate electrode and contacted by a bridge after removing the insulator on the pillar top is presented in figure 5.10c.

In order to ensure proper electrical contacts after insulator removal in the last presented fabrication method, a reliable etching method has to be developed. Since the available insulator materials are SiO_2 and Si_3N_4 a first idea is to use dry etching to make

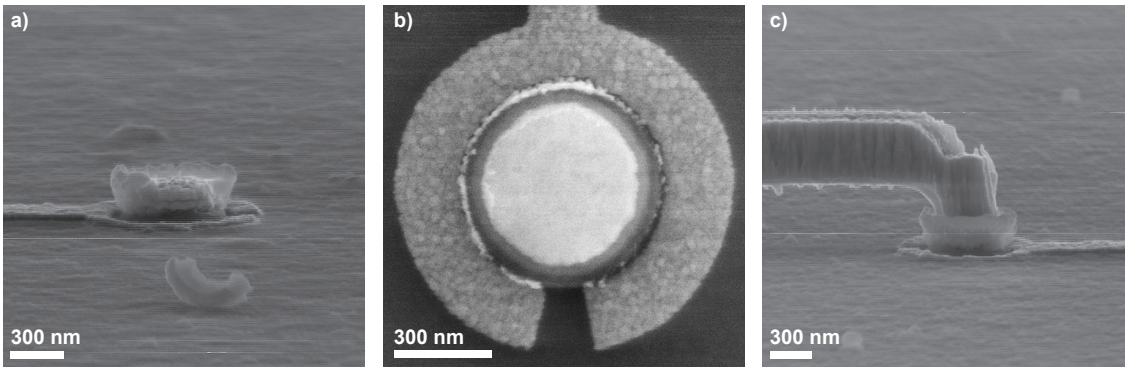

Fig. 5.10: SEM micrographs: a) Side view of an insulator covered pillar fitted with a gate electrode and the dielectric material on its top contact removed, b) top view of a pillar gated right after insulator deposition, c) side view of a final device to which the gate is added right after insulator deposition.

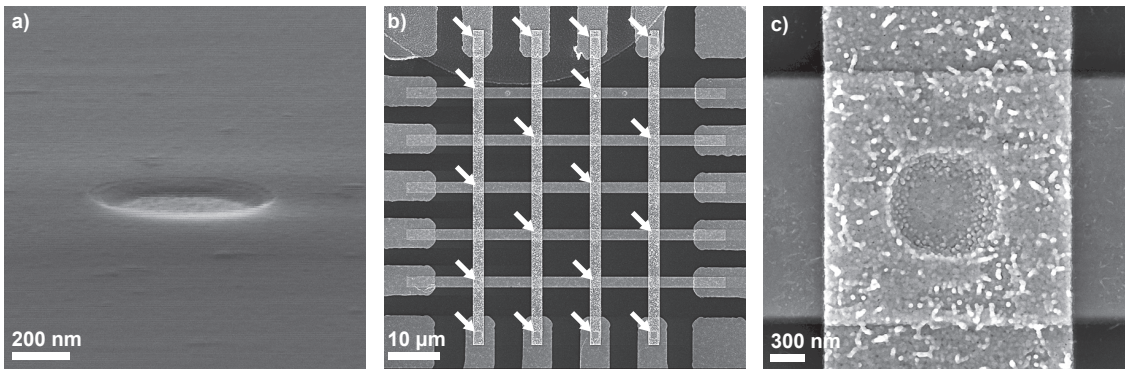

Fig. 5.11: a) SEM micrograph of a 400 nm hole in Si_3N_4 etched by RIE. b) SEM Top view of the test sample used to check the electrical contact of etched holes (indicated by arrows). c) Close view of the electrical contact at an etched hole.

holes in the insulator. For this purpose a flat test sample is covered with 60 nm of insulator and then the 5-layer resist system presented in chapter 3.2.3 is spun on. Since both SiO_2 and Si_3N_4 can be etched by a mixture from CHF_3 and O_2 [Stei 85, Dula 91], the available RIE system equipped with these gases is used. The etching procedure consists of first applying a dry etching step using a CHF_3:O_2(8:1) mixture for 40 sec. In the second step a 30 sec low energy O_2-plasma is performed to remove any organic residue originating from the CHF_3 [Kuo 90]. Figure 5.11a displays the obtained hole, which is perfectly clean in the center and has sloped sidewalls due to the lateral etching of the resist mask. To test the electrical properties of the etched holes a test sample shown by figure 5.11b is prepared. First, five parallel Au lines as well as the bonding pads are lithographically prepared on an insulating substrate and then a 60 nm thick Si_3N_4 layer is deposited by PECVD. Following the aforementioned process holes are fabricated in the insulator at the positions marked with arrows in figure 5.11b. Finally Au stripes perpendicular to the first ones are lithographically fabricated. Evident from figure 5.11b two groups of contacts are formed: one group in which the two pairs of lines are connected by holes as shown in figure 5.11c and a second group in which the two pair of lines are disconnected. Electrical measurements within each group of contacts reveal resistances of some 100 Ω, where as no electrical link between the two groups is measurable. Hence the RIE dry etching process facilitates clean surfaces for good contacts and it can be used in the artificial atoms fabrication process.

Apart from the just presented fabrication process, which is restricted to SiO_2 and Si_3N_4, a second more general one has also been developed. Its advantage is that it has less restrictions on the applicable insulator. The basic idea is based on the resist mask for metal mask removal method presented in chapter 4.1 and schematically depicted in figure 4.10. In contrast to figure 4.10 the starting point is now the insulator covered pillar fitted with an either annular or planar gate, as described earlier in this chapter. Then steps (ii), covering the sample with resist, and (iii), thinning the resist just below the pillar's top, from the technique in figure 4.10 are carried out unaltered. At this point

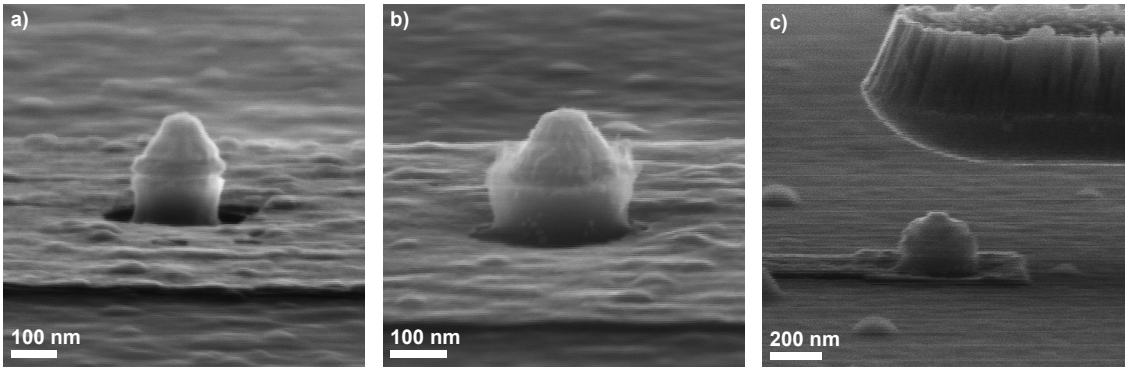

Fig. 5.12: Side view SEM micrographs of a) a pillar after performing a wet etch step to remove Si_3N_4 from its top contact, b) a pillar after performing a RIE dry etch step to remove Si_3N_4 from its top contact, c) a final device when the Al_2O_3 is dry etched by CAIBE.

an adequate etching method has to be chosen in order to remove the insulator from the pillar's top contact. At first, a wet etch step has been executed, because of its simplicity. However from the result presented in figure 5.12a this idea proves to be not applicable. The wet etchant removes not only the insulator at the top of the pillar but also at the sides and leaving the mesa completely uncovered. Therefore dry etching remains the method of choice also in this situation. Dependent on the deposited insulator the adequate dry etching method, e.g. RIE, RIBE, IBE or CAIBE, has to be used. From the technique in figure 4.10 steps (iv), dry etching, and (v), resist removal, are carried out. At this point merely one restriction regarding the insulator has to be taken into account. It is necessary that the selectivity of the insulator is higher or at least equal over the applied resist mask. In the case that the insulator etching rate for the best applicable dry etching technique is lower than the one of the protecting resist mask, it is best to perform this dry etching method several times and thus stepwise remove the insulator from the pillar's top contact.

Figure 5.12b displays the final result of this method on a pillar covered by Si_3N_4 and dry etched with RIE. To emphasize the universality of the technique figure 5.12c shows a final device, where the pillar has been covered by Al_2O_3 using a self-made ALD device. Here the insulator has been removed by CAIBE and at the end the pillar's top protrudes the insulator.

In addition to the pillar the insulator has also to be removed from the bonding contacts. For that purpose it is sufficient to expose holes in the resist at the required spots. Meanwhile all other surfaces are protected and not affected by the dry etching in any way. Finally after the necessary spots have been freed from the capping insulator material, the Ti-mask can be removed by dry etching with Ar in IBE mode. This step facilitates also a clean Au top surface at the end of the dry etching processing steps and ensures good electrical contacts.

During process development and its implementation in the existing fabrication process for sub micrometer sized pillars another issue arose. Not only the application of the gate

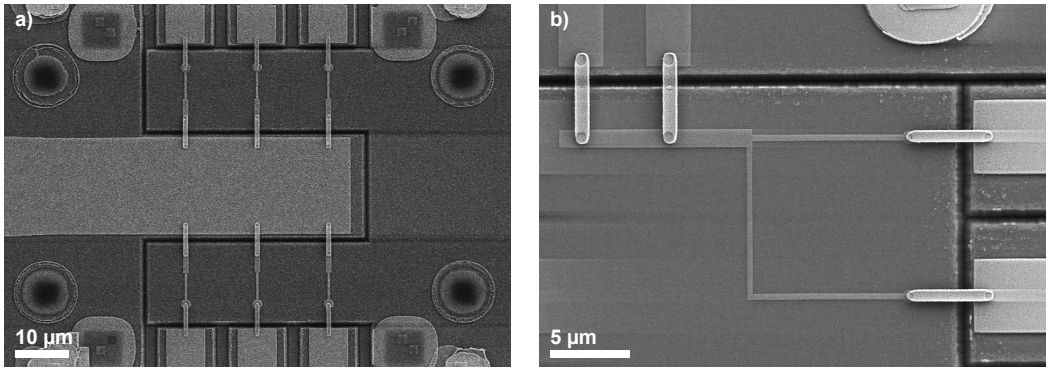

Fig. 5.13: SEM micrographs of samples from a) a design with a single bonding contact for the gate electrodes and b) a improved design with two gate bonding pads per device group.

electrode has to be ensured, but the corresponding bonding pads have to be reliably manufactured as well. From the presentation in chapter 3.1 the different contacts have to be separated by trenches and thus the gate bonding pad is connected by bridges to the gate electrode. In the beginning all gate electrodes are connected to a single bonding pad as shown by the SEM micrograph in figure 5.13a. This design turned out to be unfavorable to work with for several reasons. First, there is only a single bonding contact, which does not allow any statement about the electrical contact to the gate electrode. Furthermore, in the case that either before or during measurements one of the gate electrodes starts to leak, all other pillars become unusable, because all devices have also a common backside contact. To overcome these issues the design is switched to a double bond pad architecture displayed by the SEM micrograph in figure 5.13b. This design first of all separates different devices into independent groups, which still share a common backside contact, but have separated gate contacts, hence leaking in one group does not affect the other ones. The double gate design allows for testing the electrical contact to the gate electrode by passing a current from one gate bonding pad to the second one. Linear resistances of some 100 Ω indicate good contacts between the bonding pads and the electrodes. Is this resistance on the other hand non-linear or non-determinable, because of an open circuit, the redundancy of the bonding contacts still can facilitate a working device, increasing the yield on the complex process devices.

Finally the bonding of the gate pads itself turns out to be challenging and has to be done very carefully. A major difficulty arises from the sticking of the insulator to the ZnSe surface of the backside contact layer. By evaporating 2 nm of Ti on the area of the future bonding pads and exposing the sample to a pure O_2 atmosphere for 10 min, without removing the protecting resist a thin titanium-oxide layer is created. This thin film improves sticking of the insulator to the semiconductor surface. Nevertheless extreme caution has to be used when the actual ultra sonic bonding procedure is performed. Since the insulator can be easily perforated when the normal bonding procedure is applied, shorting of the gate bonding pads to each other as well as ripping the contacts off the surface is highly probable. To avoid these dangers, a soft bonding method is deployed.

The prepared bonding wires are pressed onto the bonding pads with minimum power as well as force and the electrical contact is then provided just through the ultrasonic welding between the gold wire and gold pad.

Following the processes, procedures and recipes described in this section both gate electrodes and bonding pads can be reliably manufactured and working three terminal devices are fabricated for tests on artificial atom properties.

5.2.2 Gate performance

Once again the device fabrication is accompanied with continuous electrical characterization. For this purpose the advancing development of the gating technology has been carefully monitored in terms of electrostatic influence on the QW.

In order to achieve the necessary lateral confinement in the QW the alterable parameters in the fabrication process have to be assessed. For this purpose it is useful to look at the gate and the mesa in the basic configuration of a cylindrical capacitor, which is described by equation 5.3

$$C = 2\pi\epsilon_0\epsilon_r \frac{l}{ln\frac{R_{out}}{R_{in}}} \tag{5.3}$$

$$C = const \times \frac{\epsilon_r}{ln\frac{R_{out}}{R_{in}}} \tag{5.4}$$

where R_{in} and R_{out} denote the radii of the inner and outer cylinder, l the length of the capacitor, ϵ_0 the vacuum permittivity and ϵ_r the relative permittivity of the dielectric material. Since the thickness of our gate electrode, being equivalent to l, is the same for all samples, it can be combined with $2\pi\epsilon_0$ into general constant value *const*. Hence just three parameters remain which can be modified as shown by the simplified equation 5.4. These three parameters are: ϵ_r given by the applied insulator material, R_{in} corresponding to the pillar radius and R_{out} being the gate electrode inner radius composed of R_{in} plus the dielectric thickness.

Given the pillar mesa miniaturization delineated in chapter 4.2, starting with diameters < 600 nm insulator material is deposited onto the samples to protect these from oxidation. At the same time this offers the possibility to start testing the outlined gating technique, applying the annular gate design. Based on the findings from section 5.1 first SiO_2 is deposited as gate insulator, deploying a PECVD process at 200 °C. Figure 5.14 presents the I-U measurements on a gated 500 nm wide pillar fitted with 70 nm of SiO_2. First thing to be pointed out is the positive evidence of a gating effect being clearly observable. Nevertheless the influence is rather small and does not change the characteristic of the I-U curve drastically, except for the obvious decrease in current based on the diminished cross-section available for transport. From the simple cylindrical capacitor scheme and as one expects, more gating influence is provided when the dielectric material is replaced by one with higher ϵ_r. As presented in section 5.1, PECVD deposited Si_3N_4 has a higher ϵ_r than SiO_2.

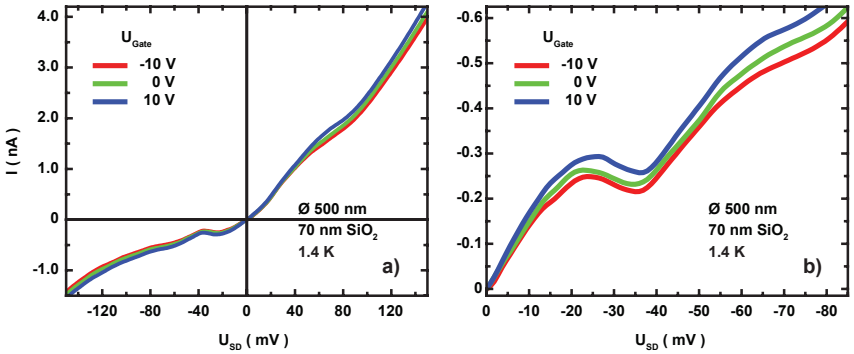

Fig. 5.14: a) I-U_{SD} curves at different U_{Gate} for a pillar size of 500 nm fitted with 70 nm of SiO_2. b) Zoom of the 3^{rd} quadrant showing the small gate influence.

Figure 5.15a displays the I-U measurements again on a 500 nm wide pillar but now fitted with 110 nm of Si_3N_4, making use of a PECVD process at 200 °C. Although for comparison reasons a similar dielectric thickness would be ideal, due to deviations in the etching depth a slightly thicker insulator layer is necessary to align the gate electrode with the QW. However, in contrast to the SiO_2 device a distinct modification of the on resonance structure when the gate voltages is swept in the same range. Along with the increasing gate effect also the occurrence of higher leakage currents is noticeable, vertically shifting the I-U curves relatively to each other. The gate voltage U_{Gate} sweep at a constant source drain DC voltage U_{SD} of 0.5 mV, presented in figure 5.15b, indicates a linear change of the leakage current of approximatively 50 pA within the voltage sweep range of 10 V to -10 V. Furthermore also the previously observed hysteresis typical for Si_3N_4 is clearly visible. Far more important in this case is however the similar structure on top of the linearly changing leakage current for both the up, 10 V to -10 V, and down, -10 V to 10 V, gate voltage sweep. The observed structure is qualitatively similar, but shifted in its gate voltage position, which the charging of the insulator traps accounts for.

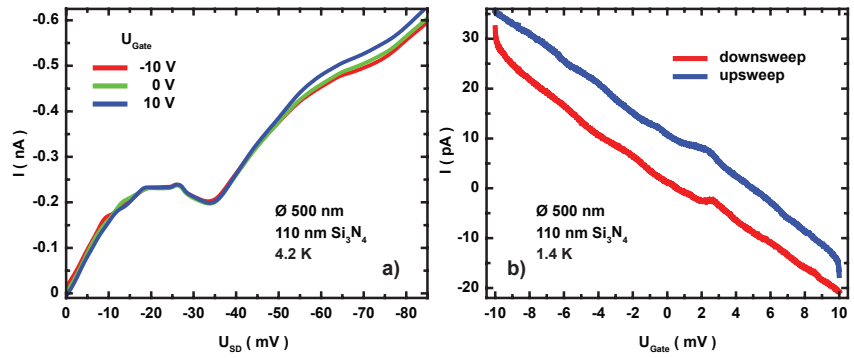

Fig. 5.15: a) I-U_{SD} curves at different U_{Gate} for a pillar size of 500 nm fitted with 110 nm of Si_3N_4 showing modification of the resonance as well as a vertical shift because of increased leakage. b) I-U_{Gate} curves at $U_{SD} = 0.5$ mV documenting the leakage current as well as similar structure in down and up sweep.

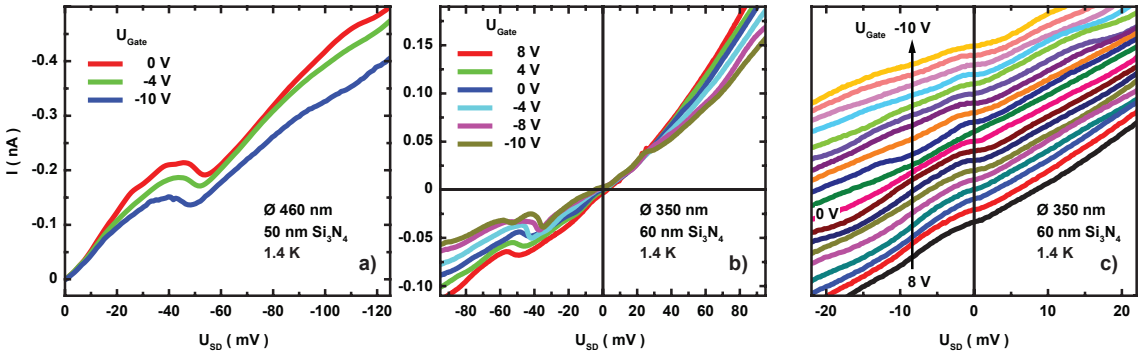

Fig. 5.16: I-U_{SD} curves at different U_{Gate} for a) a pillar size of 460 nm fitted with 50 nm of Si_3N_4 and b) a pillar size of 350 nm fitted with 60 nm of Si_3N_4 showing increasing gate influence as well as modification of the resonance because of growing lateral confinement. c) I-U_{SD} curves at intervals of $\Delta U_{Gate} = 1$ V showing alteration of the slope at $U_{SD} \approx 0$ V (offset for clarification).

Since at this stage no other higher k insulator material with conformal application is on hand, there is an other possibility to increase the gate effect according to the simple cylindrical capacitor picture. The capacity increases by reducing the ratio between R_{out} and R_{in}, which is equivalent to bringing the two plates nearer to each other. In a device this is realized by further decreasing the dielectric thickness, which leads to an increase of the gate capacity as well as the gate effect likewise. Due to the accuracy of the fabrication process and the minimum required etching depth, because of the necessary contacting of the backside layer, insulator thicknesses between 40 nm and 60 nm are used in the following. This limited variation in dielectric thickness leads to the second possibility to increase the gate influence based on the reduction of the pillar diameter. Although a reduction in R_{in} for a fixed insulator film thickness entails a slight reduction in capacity according to the simple picture from equation (5.4), the diminishment of the mesa's lateral physical dimensions also leads to a stronger but unalterable confinement. Combining both ideas the goal of studying artificial atoms can be achieved by further decreasing the pillar width and fine tunning the respective potential landscape with a thin film insulator gate. Following this path devices with pillar diameter < 500 nm have been fabricated and fitted with Si_3N_4 films < 100 nm.

Figure 5.16a presents I-U measurements at different U_{Gate} for a 450 nm device exhibiting a pronounced gate dependence. Comparing the I-U curves in figure 5.15a at different U_{Gate} to the ones in figure 5.16a when the voltage is changed from 0 V to -10 V a stronger gating effect becomes obvious. Taking into account that the change in diameter is rather small, but the thickness of the dielectric material is reduced by 50% the increased gate influence follows the expected assumption from the simple cylindrcal capacitor picture. Having established a greater gating effect in this device, in the next step is the further reduction of the later physical dimension. In fabricating devices with diameters of 350 nm and an insulator film thickness of 60 nm the increasing 3D confinement and thus the formation of a vQDot becomes considerably visible in the I-U curves

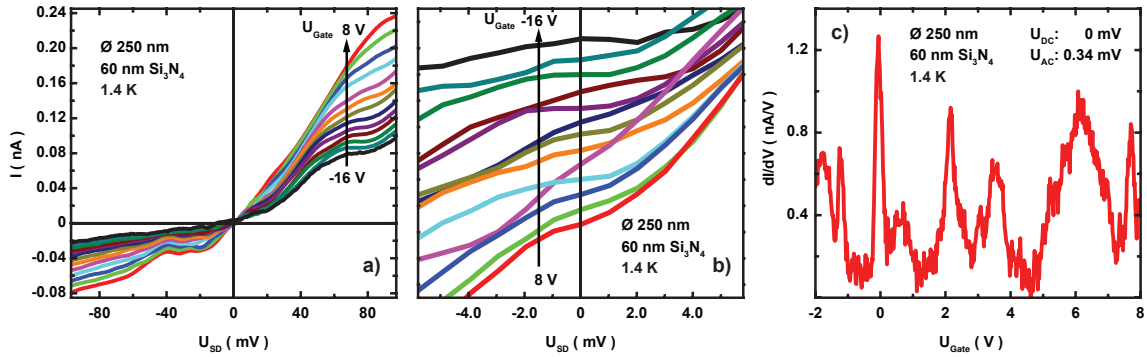

Fig. 5.17: a) I-U_{SD} curves at different U_{Gate} for a pillar size of 250 nm fitted with 60 nm of Si_3N_4 showing clear gate influence as well as modification of the resonance because of growing lateral confinement. b) I-U_{SD} curves at intervals of $\Delta U_{Gate} = 1$ V showing alteration of the slope at $U_{SD} \approx 0$ V (offset for clarification). c) Differential conductance vs. U_{Gate} at U_{SD} of $U_{DC} = 0$ V and $U_{AC} = 0.34$ mV showing resonances from energy levels aligning with the Fermi energy.

for increasing negative U_{Gate} displayed by figure 5.16b. Although this devices once again exhibit a small leakage current, the closer view, shown by figure 5.16c, on the I-U_{SD}-U_{Gate} characteristic around $U_{SD} \approx 0$ V, reveals unambiguously the change in slope as U_{Gate} is modified. This alteration in slope is a unmistakable indication that energy levels of the vQDot are passing through the small Fermi energy window. The stepwise character of some I-U_{SD} measurements also emphasizes this picture.

By further reducing the pillar diameters down to 250 nm while the Si_3N_4 film thickness is kept at 60 nm, the confinement is increased and the gating effect becomes more pronounced, as displayed in figure 5.17a. The enhanced gate influence is best identifiable by the reduction of the backside current through the device, which is considerably enhanced in contrast to devices of diameters > 350 nm earlier presented. In addition to this the investigation of the I-U curves at $U_{SD} \approx 0$V for different U_{Gate} presented in figure 5.17b reveals a periodic alteration of the slope between 0 and a finite value. This fact indicates on the one hand that the confinement within the device reaches the 0D limit and on the other that several energy levels of the forming vQDot can be swept through the small Fermi energy window as U_{Gate} is modified.

To verify this assumption the U_{Gate} sweep at constant $U_{SD}^{DC} < 1$ mV has to be investigated. However, to exclude the effects of the small leakage current superimposed on the resonant signal in the DC measurement, similar to the situation in figure 5.15b, the differential conductance $\frac{dI}{dU}\big|_{U_{SD}=const}$ is determined by Lock-in measurements. Figure 5.17c displays the result of a measurement recorded at $U_{SD}^{DC} = 0$V, $U_{SD}^{AC} = 0.34$ mV and an excitation/detection frequency of 11.3 Hz. The observable resonances coincide with the alteration of the observed I-U slope and hence confirm the previous assumption of the manipulation of energy levels within the vQDot.

Alternatively to the annular gate design, a planar gating scheme (figure 5.8) combined with the resist mask dry etching process(figure 4.10) for removing gate excess metal, the

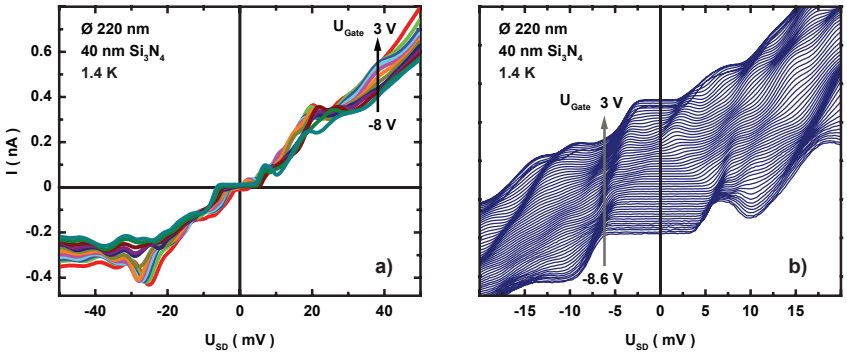

Fig. 5.18: a) I-U_{SD} curves at different U_{Gate} for a pillar size of 220 nm fitted with 40 nm of Si_3N_4 showing clear gate influence as well as modification of the resonance because of growing lateral confinement. Sample has been fabricated following the planar gate method. b) I-U_{SD} curves at intervals of $\Delta U_{Gate} = 0.2$ V showing alteration of the slope at $U_{SD} \approx 0$ V (offset for clarification).

insulator as well as the Ti metal mask on the pillar top has also been applied. These methods have been used to manufacture devices from wafer II with diameters as small as 200 nm. Figure 5.18a presents the I-U-U_{Gate} measurements on a 220 nm pillar from this batch proving that this design is also well applicable to tune the lateral confinement of the QW. In addition to this also an alteration of the slope at $U_{SD} = 0$ V in figure 5.18b, when U_{Gate} is swept, is clearly evident and emphasizes the formation of a 0D object. Together with the annular gate design there are now two processes at hand allowing to reliably manufacture 0D objects which can be investigated regarding their atomic like properties.

Finally in figure 5.19 some cases of malfunctioning gates are presented. For a start, the simplest possible defect is a poor quality insulator, which becomes obvious by the occurrence of leakage. Thus such a leakage current, in absence of any gating effect, simply

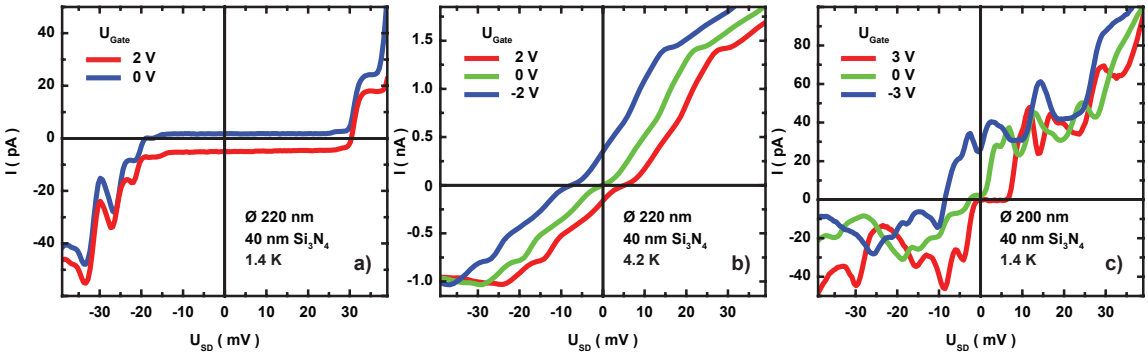

Fig. 5.19: I-U_{SD} curves at different U_{Gate} for a pillar size of 220 nm fitted with 40 nm of Si_3N_4 showing no gate influence but a) a vertical shift because of leakage and b) a horizontal shift due to the influence on the Fermi energy of the leads. c) I-U_{SD} curves at different U_{Gate} for a pillar size of 200 nm fitted with 40 nm of Si_3N_4 showing gate influence as well as a horizontal shift due to the influence on the Fermi energy of the leads.

shifts the I-U curves vertically along the current axis, shown in figure 5.19a. To avoid this case the quality of the applied insulator has to be ensured beforehand by optimizing the growth and deposition parameters. Additionally a vertical misalignment of the gate electrode can occur in case that the combination from semiconductor etching and subsequent insulator deposition fails. The resulting effect on the I-U characteristic, as shown in figure 5.19b , in absence of any gating effect on the QW, expresses itself by a lateral shift of the curves when U_{Gate} is swept, since the Fermi energy in the gated lead is influenced. By carefully monitoring the etching parameters as well as the dielectric deposition there is great success in preventing such a case. Most likely is although that the gate is placed at one of the barriers which leads to influences on the adjacent lead as well as the QW simultaneously. From figure 5.19c showing this case, the I-U measurement are both modified and shifted laterally when $U_{Gate} \neq 0$ V. The latter two issues emphasize once again how critical the correct positioning of the gate electrode with the QW is. Nonetheless working devices showing tuneability of the 0D confinement by the gate prove the feasibility of the process when the necessary caution is exercised during device fabrication.

Chapter 6

Magnetic artificial atoms

Having established the prerequisite heterostructure and all necessary manufacturing steps, magnetic artificial atoms from the II-VI DMS (Zn,Cd,Mn)Se can be fabricated. The first part of the following chapter presents two entire fabrication processes for vQDots enabling magnetic artificial atoms to be formed. The first manufacturing method which was published in Dengel *et al.* [Deng 12], represents the basic vQDot process. Subsequently an improved and more general vQDot process is depicted. The second part of the chapter presents the physical observations indicating the formation of magnetic artificial atoms in devices manufactured using both processes.

6.1 Manufacturing processes

The starting point of all manufacturing processes is based on a II-VI DBH of the (Zn,Cd, Mn,Be)Se material system with low doped injector and collector leads, which has been developed by Slobodskyy *et al.* [Slob 03]. The heterostructure is grown by molecular beam epitaxy (MBE) on a standard epi-ready GaAs wafer and buffer layer. To eliminate the influence of electrical fields and charging at the polar III-V/II-VI interface[Frey 09, Farr 91, Frey 10a], a 200 nm thick highly doped ZnSe screening layer is grown, followed by 7 periods of an undoped ZnSe / $Zn_{0.9}Be_{0.1}Se$ (50 nm / 20 nm) superlattice and a 300 nm thick undoped $Zn_{0.97}Be_{0.03}Se$ layer. A two-layer backside contact is deposited on this base. It consists of a 300 nm thick $Zn_{0.97}Be_{0.03}Se$ (2×10^{19} cm^{-3}) doped layer, which is perfectly lattice matched to GaAs and does not add strain to the structure. This is followed by a 100 nm thick ZnSe (2×10^{19} cm^{-3}) doped layer to minimize contact resistance [Miya 92]. The resonant structure proper is then grown. 10 nm $Zn_{0.97}Be_{0.03}Se$ (1×10^{18} cm^{-3}) and 10 nm undoped ZnSe act as the source to the $Zn_{0.75}Be_{0.25}Se$ / $Zn_{0.844}Cd_{0.076}Mn_{0.08}Se$ / $Zn_{0.75}Be_{0.25}Se$ (6 nm / 7.2 nm / 6 nm) DBH forming the QW. Drain and top contact of the device are provided by 10 nm undoped ZnSe followed by 15 nm $Zn_{0.97}Be_{0.03}Se$ (1×10^{18} cm^{-3}) and 30 nm ZnSe (2×10^{19} cm^{-3}) capped in situ with Al / Ti / Au (10 nm / 10 nm / 30 nm), again to minimize contact resistance [Maxi 04].

The entire schematic of the heterostructure is depicted in figure 6.1. It highlights the previously mentioned challenges to device fabrication: the need for > 1 μm deep trenches

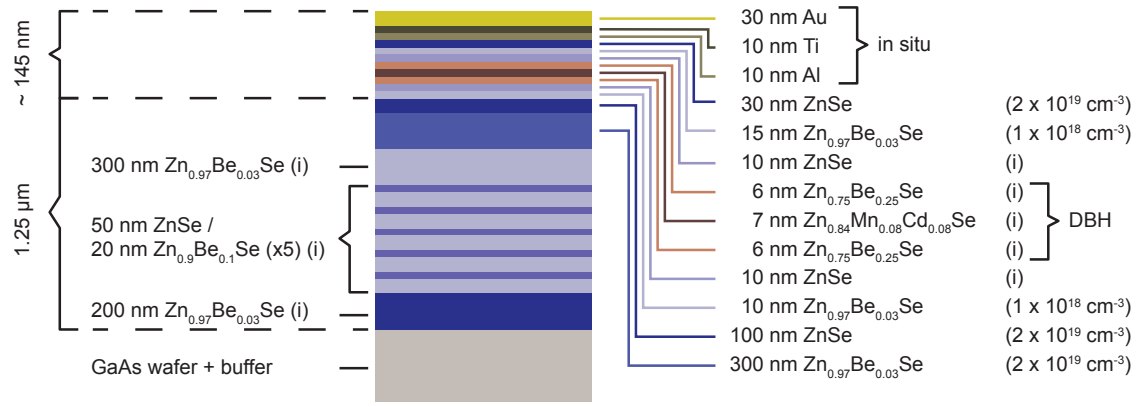

Fig. 6.1: Schematic of the entire layer structure being the starting point of the manufacturing process of magnetic artificial atoms.

down to the buffer to prevent shorting through the superlattice (ch.3.1), the requirement of a gate insulator and the necessity of a very thin (15 nm) gate aligned to be exactly at well level (ch.5.2).

In order to create vQDots pillars are carved from this material. By applying contacts to the top of the pillar as well as to the conducting backside layer, electrically addressable devices are then produced. Surrounding the pillar by an annular electrostatic gate enables the manipulation of the band structure and hence the energy spectrum of the 0D object.

6.1.1 Basic vQDot process

The manufacturing process consists of five major steps. First the trenches electrically dividing top, back and gate contacts are carved. Second, the pillar and the top contact bonding pads are defined in the heterostructure. The backside contact and gate insulator are put down in a third step. This is followed by fabrication of the gate and its bonding contacts in the fourth step. In a fifth and final step, bridges are added to connect top contact and gate to their respective bonding pads.

Trenches

In the beginning to remove any organic residue from the topmost metal layer, the MBE grown heterostructure is thoroughly cleaned by immersing the wafer piece in heated NEP, heated MIBK and finally exposing it to a low power O_2-plasma in a RIE system. The cleaned sample is immediately transfered to an UHV metal evaporation chamber and Ti (7 nm) and Au (80 nm) are evaporated to strengthen the top contact. Prior to the first major EBL step a set of global and local alignment marks are manufactured by an e-beam and lift-off step. This is required to enable an accurate alignment in the following multi writing field exposure. Subsequently the first EBL step defines the trenches separating the top, backside and gate contact areas. First the trench pattern is created in a 640 nm thick

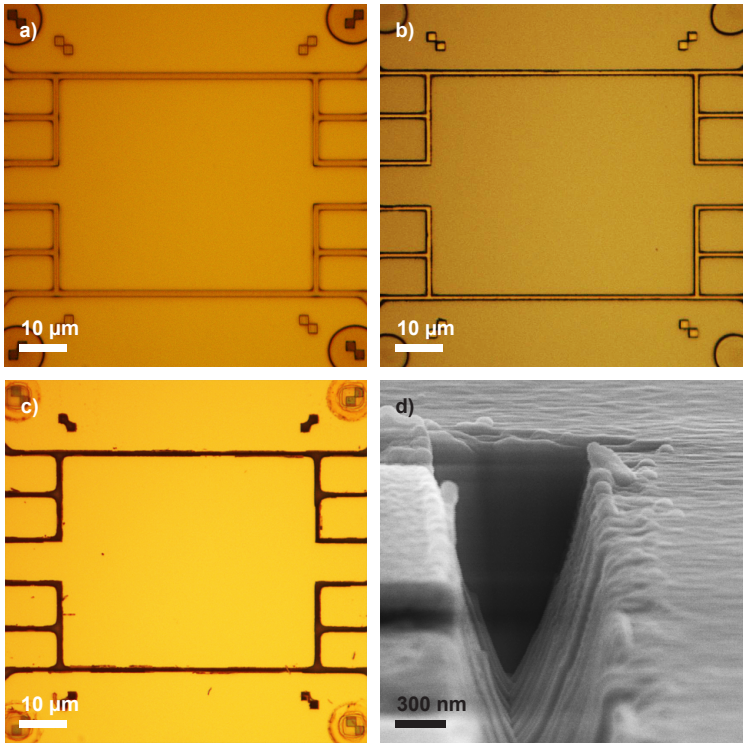

Fig. 6.2: Optical images of the trench fabrication showing a) the negative resist mask, b) the Ti metal mask after lift-off and c) the sample after dry etching in CAIBE as well as excess Ti metal removal by HF. d) SEM micrograph of a 1 μm wide trench (at a later step in the process).

negative resist, specifically the image-reversal resist AR4060 (fig.6.2a). After evaporating 165 nm Ti, standard lift-off leaves a Ti coating on the surface with gaps where the trenches are to be, generating the essential metal mask (fig.6.2b). In the device's center region the gaps are 1 μm wide, while 5 μm wide ones are used for outer zones around the big bonding pads. The gaps are converted into trenches in the heterostructure by two steps of anisotropic dry-etching at 90°, using a chemically assisted ion beam etching (CAIBE) system. First, the top contact metal is removed by Ar using the ion beam etching (IBE) mode. In the second step BCl_3 is added as a chemical assistant from the gas ring to etch the semiconductor down into the undoped GaAs buffer.

Its low dry-etching rate of $\sim$ 5 nm/min in CAIBE mode makes Ti an ideal masking metal when mesas with high aspect rations are needed [Krum 73, Some 76]. Additionally, the excess Ti metal at the end of the dry etching process is easily removed by a 20 to 25 sec dip in diluted HF. This is in contrast to the more complicated and difficult removal of a resist mask, whose surface hardens during the $\sim$ 20 min ion bombardment. At the end of this processing step, a clean, unpolluted Au topmost surface is left behind and 1.3 μm deep trenches have been carved down to the III-V host wafer (fig.6.2c,d). These deep trenches assure the electrical separation of the various contact zones.

The depth of all etching steps during all fabrication processes is monitored via several control structures fabricated in parallel to real devices. The depth and height profiles are

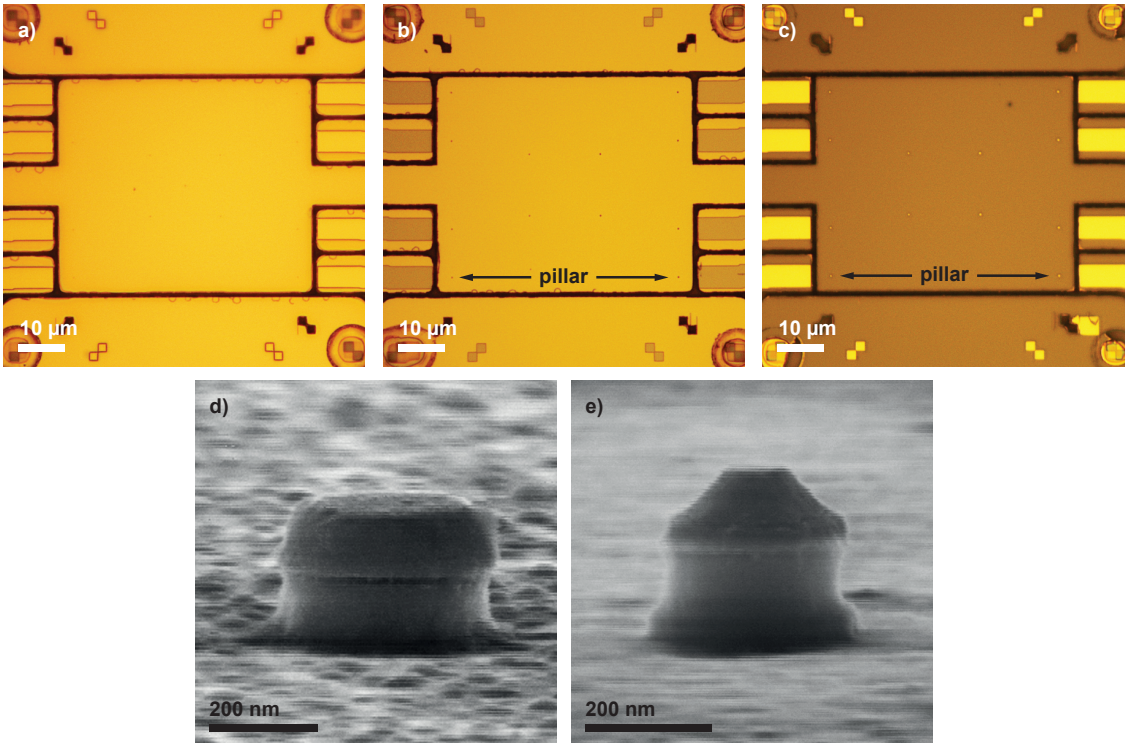

Fig. 6.3: Optical images of a) the resist and b) Ti metal mask as well as c) the sample after dry etching in CAIBE and excess Ti metal removal by HF (pillars indicated by arrows). SEM micrographs of a d) 350 nm and e) 250 nm pillar after dry etching in CAIBE and chromosulfuric acid dip.

measured using a Dektak 6M stylus profilometer. The accuracy of this measurement has been verified by direct imaging using a secondary electron microscope (SEM) and has an uncertainty of $\sim$ 10 nm for 1 μm and $\sim$ 5 nm for 100 to 300 nm etching depths.

Pillars and top contacts

In the second major EBL step, the pillar as well as the bonding pads, which will later connect to the top contacts, are defined. This time, a positive three-layer PMMA resist made from 2 times 600 K (4%) PMMA as bottom layers and a 950 K (3%) top layer is patterned (fig.6.3a). The developed pattern is then once again converted to a 65 nm thick Ti metal mask by metal evaporation and lift-off (fig.6.3b). The mask thickness is kept as small as possible, but still thick enough to avoid the contamination of the topmost Au layer with chloride radicals, as discussed in chapter 4.1. The reason for minimizing the mask thickness is twofold. First, as presented in chapter 4.1, this prevents the formation of facets. Secondly and much more important is the diluted HF dip for the mask removal later on in the manufacturing process. The thinner the excess metal, the faster it is removed, the shorter the HF dip and thus less under cut occurs at the pillars top metal, ensuring proper electrical contact.

Additionally a new set of local alignment marks is defined in this step. In doing so the misalignment caused by accumulated errors from stage movement during previous work at the EBL-machine is eliminated. These alignment marks simultaneously defined with the pillar allow an accurate lateral adjustment of the gate electrode and the air-bridge, crucial for proper device functionality.

After the mask fabrication, the pattern is then transfered to the semiconductor using a similar CAIBE etching sequence as above, but in this case at a 70° angle of incidence. A total of approximately 5 min are needed to etch down to the top of the 400 nm thick backside contact layer (see fig. 6.1). Since about 4 min of the etching is performed in IBE mode and only about 1 min in CAIBE mode, the exposure of the entire sample to BCl_3 radicals is kept to a minimum. This etching process leaves a mesa with walls having a profile angle of $\sim 85°$. The excess mask metal is left on the Au surface to protect it during a subsequent wet-etch step. A dip of no more than 5 sec in chromosulfuric acid removes $\sim$ 20 nm of semiconductor from all surfaces, and also creates even steeper mesa profiles (fig.6.3d,e). This wet etching step is crucial to remove the surface of the semiconductor, which has been damaged by ion bombardment. Without this step the electric fields from surface defects completely deplete the device.

Backside contacts and insulator deposition

In the next step bonding pads to the backside are fabricated by optical lithography and evaporation of Ti/Au directly onto the conducting backside layer. Prior to metal evaporation once again a 5 sec chromosulfuric acid dip refreshes the contact area and ensures ohmic backside contacts. Subsequently a 10 to 15 sec dip in diluted HF then removes the 5 to 10 nm excess Ti from the previous step, leaving clean Au on the pillar top as well as all the bonding pads (fig.6.3c).

Furthermore, bonding experience has shown that it is necessary to increase the adhesion between semiconductor and insulator. The reason is that the bonding pads, which will be needed to connect the gate, lie on top of the insulator, covering the entire sample. To enhance the mechanical stability of these pads, optical lithography is used to cover the area where they will be by 2 nm of Ti which is allowed to oxidize, greatly enhancing the adhesion.

The desired insulator is immediately deposited in the next step. This way the unavoidable oxidation of the semiconductor surface through exposure to air is kept at a minimum. In this work the entire sample is covered with 60 nm of Si_3N_4 deposited by PECVD at 200 °C. The required insulator thickness is determined after carefully monitoring the total height of the pillar produced in the previous step. On the basis of the identified growth rate of the insulator (which in the case of Si_3N_4 is it approximately 40 nm/min) it is made certain by depositing the appropriate layer thickness that the top insulator surface lies at the height of the lower tunnel barrier.

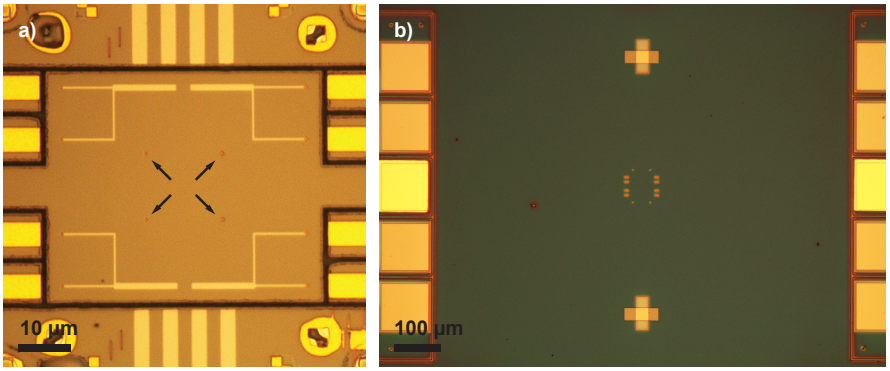

Fig. 6.4: a) Optical image of the center region of the device. Arrows indicate control structures (pillars) within the device. b) Optical image of the region in between two devices showing a control structure built up only from the center region of a device.

Gate and gate bonding pads

The third major EBL step defines an annular gate around the pillar. But before attaching the gate electrode to the pillar the existence of a systematic misalignment is checked with the aid of control structures within, figure 6.4a, and in between, figure 6.4b, actual devices. As previously pointed out, here the new alignment marks defined together with the pillars are used, improving the adjustment. Having corrected the shift in the device design, the gate electrode is exposed and developed using the aforementioned three-layer resist of 600K (4%) and 950K (3%). This gate pattern is then metalized with Ti/Au (5 nm/10 nm) and lifted off with the result depicted in figure 6.5a. Its thickness is chosen such that it covers the QW as well as parts of the lower and upper barriers of the DBH. In this way, gate influence on the artificial atom is maximized, while parasitic effects on source and drain are kept to a minimum. An additional EBL exposure defines the gate bonding contacts which are formed from much thicker Ti/Au (10 nm/120 nm) to provide the needed stability for bonding (fig.6.5b).

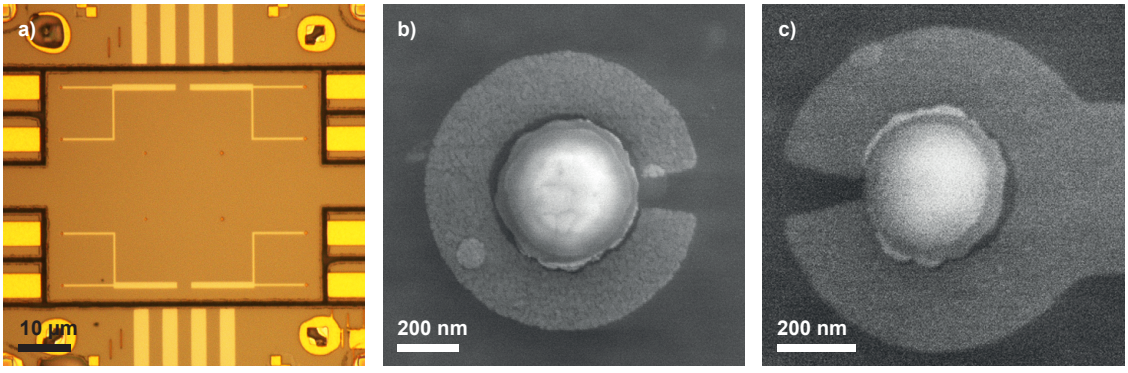

Fig. 6.5: a) Optical image of the gate electrodes. Top view SEM micrographs of a b) 350 nm and c) 250 nm pillar covered by insulator and fitted with a gate electrode.

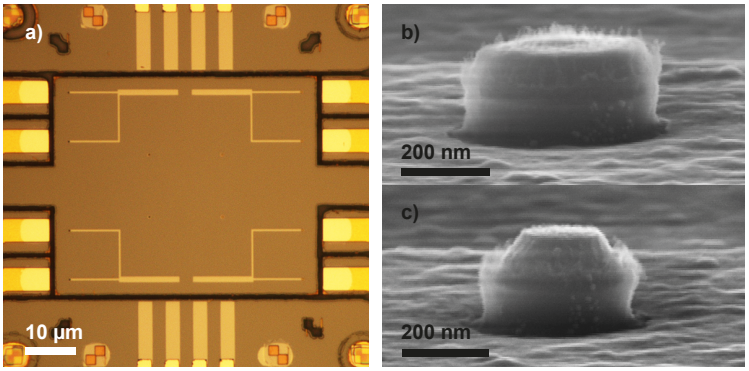

Fig. 6.6: a) Optical image of the central region showing the bonding pads after insulator has been dry etched. Side view SEM micrographs of a b) 350 nm and c) 250 nm pillar after dry etching the insulator off the top contact.

Removing of insulator and air-bridges

In order to electrically address the few-hundred nanometer sized pillar, the insulator has to be removed from the pillars top contact and its bonding pads as well as the back side contact. Furthermore the pillars top contact has to be connected to the bonding pad by applying the air-bridge technique.

Appropriate openings in the insulator are achieved by first lithographically exposing holes in a $\sim$ 1.32 μm thick PMMA multilayer resist of 3 layers 950K (3%) followed by 2 layes 950K (5%). After the EBL step the positive resist profile is then used as an etching mask. For SiO_2 and Si_3N_4 etching is done in a RIE reactor, using a gas mixture of CHF_3:O_2 (8:1) followed by a low power O_2 cleaning step to remove any organic residue left behind by the etching, each step of the procedure lasting 30 sec. Dependent on the deposited insulator thickness, this sequence is repeated several times since its etching rate is $\sim$ 40 nm/cycle. The chosen resist system is thick enough to protect the sample surface from etching and contamination. When a different insulator material is deposited, the appropriate dry etching method has to be used. A requirement to the etching process is that the etching rate of the dielectric is not much smaller than that of the resist mask. Otherwise the resist is removed before the insulator is etched. In the end with the resist mask still in place a further 10 sec Ar IBE step at 90° sputters the surface to leave a clean Au top contact, displayed in figure 6.6a for the bonding pads. The SEM micrographs in figures 6.6b and c display the insulator freed pillars' top contacts at the end of this step. Heated NEP assisted by a few low power ultrasonic pulses every 5 min is applied to strip off the resist mask and is followed by a heated MIBK bath for further surface cleaning. Since the semiconductor surface is covered by insulator and Au is the topmost metal at any place where the insulator has been removed, an additional low power O_2-plasma in the RIE reactor removes any organic residue from the previous step without affecting the device in any way. The result is an electrically addressable sample thoroughly cleaned for proper contacting.

The pillar top contact as well as the gate electrode are then connected to their bonding

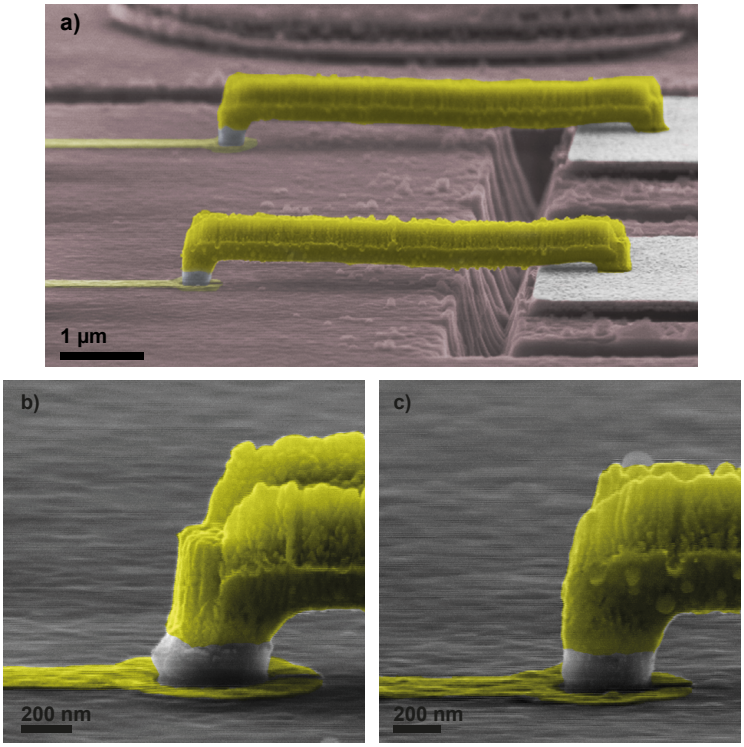

Fig. 6.7: a) SEM microgrph of air-bridges spanning a trench and connecting the pillars to bonding pads. SEM micrographs of a b) 350 nm and c) 250 nm pillar contacted by an air-bridge in the final device.

pads by 5.5 μm long and 300 nm wide air-bridges. On the pillar end, post diameters of 250 nm are manufactured while 500 nm diameter posts are defined at the bonding pad and for the gate air-bridges. This is done using the modified multi-voltage air-bridge fabrication process developed by Borzenko *et al.* [Borz 04, Borz 07] and presented in chapter 3.2.3. A five layer PMMA resist from 3 layers 950K (3%) and 2 layers 950K(5%) is required such to properly span the 1.3 μm deep trenches. The total thickness of this multilayer resist is about 1.32 μm[1] with respect to a flat surface. After metal evaporation and lift-off air-bridges spanning the trenches, similar to the ones depicted in figure 6.7a, are manufactured. Furthermore figures 6.7b and 6.7c present a zoom-in on fully functional pillars contacted by air-bridges with diameters of 350 nm and 250 nm, respectively. After cleaning, the devices are bonded and ready to be characterized.

Figure 6.8a depicts a sketch of the completed device fabricated from the II-VI heterostructure, shown in figure 6.1, and highlights the challenges regarding the manufacturing process. A top view of the entire final device is presented in figure 6.8b where the trenches electrically dividing the different contact areas are visible. A zoom into the active region of the structure is depicted in figure 6.8c providing a top view on the three terminal devices. These are divided into four groups, each of them containing two pillars

[1]On a single piece of wafer the resist thickness variates by $\pm$ 0.01 μm. For different pieces, dependent on their lateral dimensions and the resist age, the resist thickness variates between 1.32 μm and 1.36 μm.

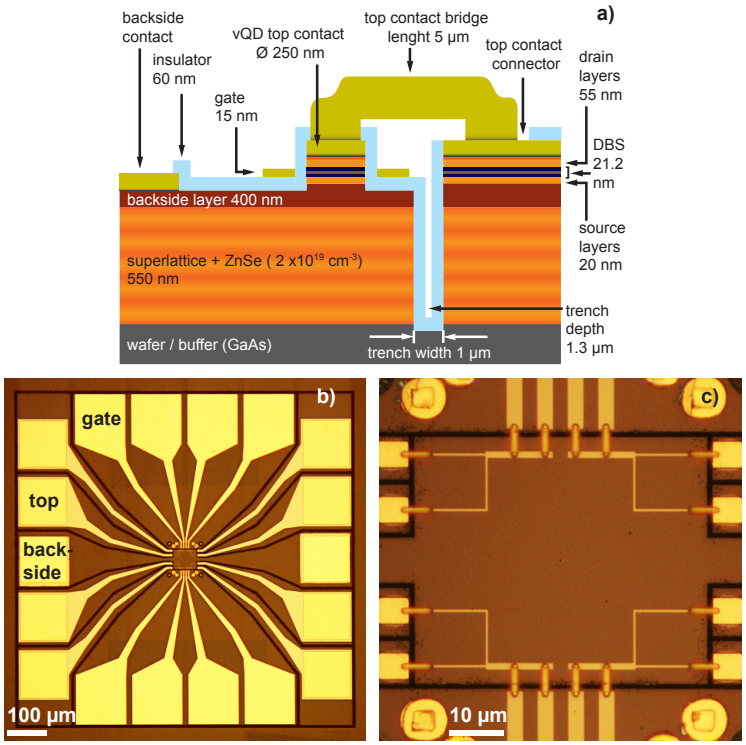

Fig. 6.8: a) Sketch of the layer structure and device. Optical images providing b) a top view of the entire structure showing the arrangement of the contacts within the frame defined by trenches and c) a close view of the central region showing four pair of devices, each with a common gate.

sharing one gate and a pair of gate bonding contacts. The joint used of a single gate for two pillars has no effect on device functionality, but rather results from a practical consideration of the limited number of 18 electrical leads on the chip carriers. This structure is now ready to be wire bonded and electrically characterized.

6.1.2 Improved vQDot process

In chapter 4, describing the pillar fabrication and characterization, it is pointed out that the step of excess Ti-mask removal by a short dip in a diluted HF solution is a critical fabrication step. Despite the fact that numerous working samples have been prepared following the basic vQDot process, it is not always portable from wafer to wafer due to differences in etch rates of Ti and Al layers resulting from normal growth to growth variations. In order to overcome this issue and have a more growth and wafer independent manufacturing method, the aforementioned basic fabrication process is modified such, that the use of the short dip in a diluted HF solution becomes obsolete. This improved vQDot process has then been used to fabricate devices from wafers, which did not allow the application of the basic process.

The improved manufacturing process is again built up from five major steps. Step

one **Trenches** and step two **Pillars and top contacts** from the basic process remain unchanged and are also the first two steps in this manufacturing method.

In the third step **Backside contacts and insulator deposition**, the first modification is introduced. While the optical lithography of the backside contacts and the dip in chromosulfuric acid are carried out as described above, the subsequent dip in diluted HF is left out. Instead the removal of the excess Ti metal mask on the bonding pads as well as the pillar top contacts is conducted in a two steps procedure after the titanium oxide adhesion layer has been deposited. The first of the two is used to take off the metal on the bonding contacts. For this purpose it is easiest to use optical lithography and fabricate 100 μm $\times$ 100 μm openings in the 1.4 μm thick resist ARU4040 at the bonding contacts. Following this either wet etching by a dip in diluted HF or dry etching with Ar in IBE mode can be applied to remove the excess Ti metal at these spots. Which of the two is more appropriate has to be decided based on the estimated thickness of the excess Ti layer from preceding Dektak measurements. Thicker layers require longer dry etching times, because the resist is exposed longer to the ion beam, which reduces the ability to strip off the resist. In the second step of this procedure the resist mask removal process described in chapter 4.1 and depicted in figure 4.10 is applied by using the PMMA bilayer resist system with 600K(4%) as the bottom layer and 950K(3%) as the top layer. After thinning the $\sim$ 310 nm thick resist using low power O_2-plasma in a RIE reactor to the required thickness $<$ 250 nm such that the pillar top protrudes the surface, the Ti metal is taken off by IBE with Ar at an angle of 70°. In the end the resist mask is stripped off by immersing the sample in hot NEP and MIBK solutions assisted with periodic low power ultrasonic pulses. Now the third major fabrication step is again completed by depositing the desired dielectric making use of the adequate conformal deposition technique. For the sample fabricated on the basis of this improved process, once again Si_3N_4 deposited with PECVD at 200 °C has been used. As a consequence of an unstable PECVD deposition rate 40 nm of dielectric instead of the necessary 30 nm are covering the sample and the resulting asymmetric alignment of the gate electrode at the DBH results in its diminished operability. In a case like this where the PECVD deposition cannot be reliably stabilized to provide adequate alignment of the gate electrode, other conformal deposition methods should be used. The atomic layer deposition is the type of technique, which provides reliably the aimed dielectric thickness by a self limited growth procedure.

The fourth major fabrication step **Gate and gate bonding pads** is conducted unmodified. In case that the annular gate design cannot be deployed due to uncorrectable misalignment in previous fabrication steps, the flat gate design described in chapter 5.2.1 and shown by figure 5.8 can be used. The fabrication of the flat gate electrode comprises the same methods as for the annular gate except for the layout.

The fifth and final step **Removing of insulator and air-bridges** also requires some modification. Though the aforementioned procedure for removing the insulator at bonding pads and the pillar yields good results, misalignment issues have led to a revision of the method. On the one hand the misalignment endangers the gate electrode by exposing it to the dry etchants and on the other it may hinder a proper insulator removal at the pillar top contact. To overcome this issue it is appropriate to use once again the resist

mask method for the pillar top contact insulator removal. As in the case of the Ti-mask removal the PMMA bilayer system 600K (4%)/950K (3%) is deployed and thinned to the necessary thickness by low power O_2-plasma. It should be mentioned that in the case of a flat gate design there is metal on the insulator at the top contact. At first by using the resist mask technique this metal is easily taken off by IBE as in the case of the excess Ti-mask. After this intermediate step the resist is stripped off and a new bilayer is spun on. The dry etching of the insulator follows the same procedure: the resist is thinned at first and then etching of the dielectric is performed. SiO_2 and Si_3N_4 are removed in a RIE reactor by a mixture from CHF_3:O_2 (8:1) at 30 W. For other dielectric materials the appropriate dry etching technique has to be chosen considering the etching rate, e.g. CAIBE for Al_2O_3 dry etching. As pointed out in the previous section the selectivity of the insulator over the PMMA resist should not be much smaller than 1. In this case if no other alternative method is at hand, the etching step is repeated several times and as often as needed to take off the insulator. In each of these steps it has been made sure that there is still enough resist protecting the surrounding gate electrode from being destructed by the etching ions. Afterwards the insulator on top and backside contacts is removed by either spinning the $\sim$ 1.3 μm 5-layer PMMA resist system and exposing 100 μm $\times$ 100 μm openings by EBL or using optical lithography with the $\sim$ 1.4 μm ARU4040 for the openings. Both resists are thick enough to protect the rest of the sample while the dry etching is conducted. After resist stripping in the final step air-bridges at the pillars and the gates using the described method are manufactured. In case uncorrectable misalignment hinders an accurate alignment the alternative manufacturing method of top touching described in appendix B should be applied. Finally the sample is cleaned in hot MIBK to remove any organic residue coming from the resist.

6.2 Observations in magnetic artificial atoms

In the course of each process a batch of samples are fabricated on a 5 $\times$ 5 mm^2 semiconductor wafer piece. After separating them by cleaving the piece, each sample is wire bonded to a chip carrier enabling electronic characterization. Preliminary measurements are performed in a bath cryostat at 1.4 K identifying the most promising devices, which are subsequently cooled in a dilution refrigerator (dilfridge).

Running the dilfridge at a base temperature of 30 mK, the thermal energy of the system is expected to be in the order of 2 μeV. From incipient broadening of the Coulomb blockade peaks' width as the temperature of the system is increased, the actual temperature of the electronic system is about 200 mK. This is typical for measurements performed on such closed system. The added power to the system, during electrical measurements, is used to heat up the electrons in the QDot device, since the weak electron-phonon coupling at these temperatures inhibits the heating to be transfered to the lattice. The resulting thermal energy of the electronic system is then about 17 μeV. In order to compare this energy to the charging energy E_C of the QDot and determine whether the system is in the Coulomb blockade regime the capacitance of a 250 nm wide QDot is roughly

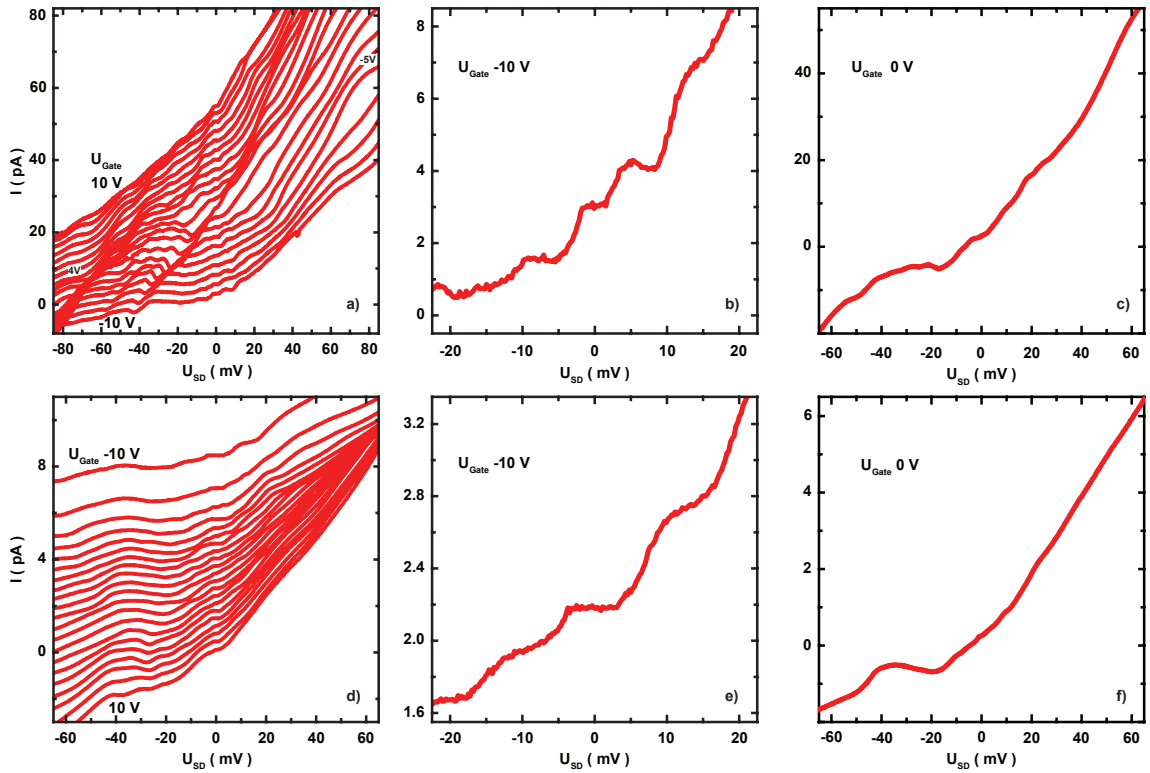

Fig. 6.9: a) and d) display I-U$_{SD}$ curves for -10 V $\leq$ U$_G$ $\leq$ 10 V in steps of 1 V for two different vQDots of a diameter of 250 nm. b) and e) show the Coulomb staircase in the I-U$_{SD}$ curves at U$_G$ = -10 V for both vQDots. The I-U$_{SD}$ curves at U$_G$ = 0 V are shown in c) and f), emphasizing the high resistance of the devices.

estimated. From Oosterkamp [Oost 99] and Kouwenhoven [Kouw 01] it is known that a QDot's real capacitance is much better approximated by two capacitors in series: a source-dot plus a dot-drain capacitor. In this picture the dot's capacitance C is defined as $C = C_S + C_D = \frac{\epsilon_r \epsilon_0 \pi d_{eff}^2}{2d_b}$. Here ϵ_0 is the vacuum permittivity, $\epsilon_r = 9$ denotes the relative permittivity of ZnSe, $d_b = 6$ nm represents the barrier thickness and the effective diameter of the dot is assumed to be $d_{eff} \approx 200$ nm, by taking into account a small depletion at the pillars' side wall. The resulting capacitance of about 0.8 fF leads to a charging energy e^2/C of about 0.2 meV. This value for E_C represents a lower limit, since a fairly large QDot has been assumed in this rough calculation. Nevertheless it shows that the system is in the Coulomb blockade regime and charging effects should be observable.

In order to test for this anticipation I-U$_{SD}$-curves at different gate voltages are recorded. Discrete charging of the QDot manifests in a staircase characteristic of the I-U$_{SD}$-curves as more and more quantized levels are added to the bias window. As described in chapter 2.1 the addition energy E_{add}, necessary to pay in order to add an electron to the dot, is just the charging energy E_C, when the single-particle energy spectrum is neglected at first (see eq.2.4). Figure 6.9a and 6.9d present a set of I-U$_{SD}$-curves for two different 250 nm wide vQDot devices, where the gate voltage U_G changes from 10 V to -10 V in steps of 1 V. The staircase characteristic is identifiable in all curves, but becomes more pronounced

as the gate voltage is made more negative. The later causes an increase of the lateral confinement and with it a decrease of the QDot's capacitance as well as an increase of the charging energy. Therefore the staircase characteristic becomes more visible within a given source-drain voltage range. Figures 6.9b and 6.9e display the I-U$_{SD}$-curves at U_G = -10 V for each of the two devices. In both cases the Coulomb staircase is well observable.

Furthermore, the Coulomb blockade regime manifests in the change of slope at U_{SD} $\approx$ 0 V. For instance, from figure 6.9a a flat curve at U_{SD} $\approx$ 0 V, i.e. U_G = 4 V or -5 V, indicates a constant number of electrons trapped in the QDot. This means no electrochemical potential is aligned within the bias window and therefore no current passes the QDot. Whereas when the gate voltage is either increased or decreased the I-U$_{SD}$-curve's slope changes to a finite value. This denotes the variation of the QDot's electronic configuration by one electron. In this case an electrochemical potential is located within the bias window which allows a current to flow through the device. Therefore the QDots are in the Coulomb regime as expected from the earlier rough estimation.

At this point the typical device resistance has to be pointed out. Devices fabricated by Tarucha [Taru 97] exhibit at 0 V gate voltage an on-peak resistance of about 12 MΩ and 20 MΩ, in positive and negative bias voltage respectively. For the two aforementioned devices the I-U$_{SD}$-curves at U_G = 0 V are displayed in figures 6.9c and 6.9f and have an observable resonance only in the negative bias regime. The on-peak resistance at this resonance, taking into account the constant leakage current, reads as ∼2 GΩ and ∼20 GΩ respectively. The three orders of magnitude higher resistance of these II-VI QDots plays an important role when it comes to measure the Coulomb oscillations, making the detection extremely challenging. Additionally, from figures 6.9b and 6.9e also the vertical shift in I-U$_{SD}$-curves catches one's eye. As discussed in chapter 5.2.2 this shift is caused by the leakage from the gate through the insulator to the backside layer, which is unavoidable as the gate electrode lies on top. It is expected that this leakage is going to strongly affect the measurement of Coulomb oscillations in I-U$_G$ mode at a constant DC source-drain

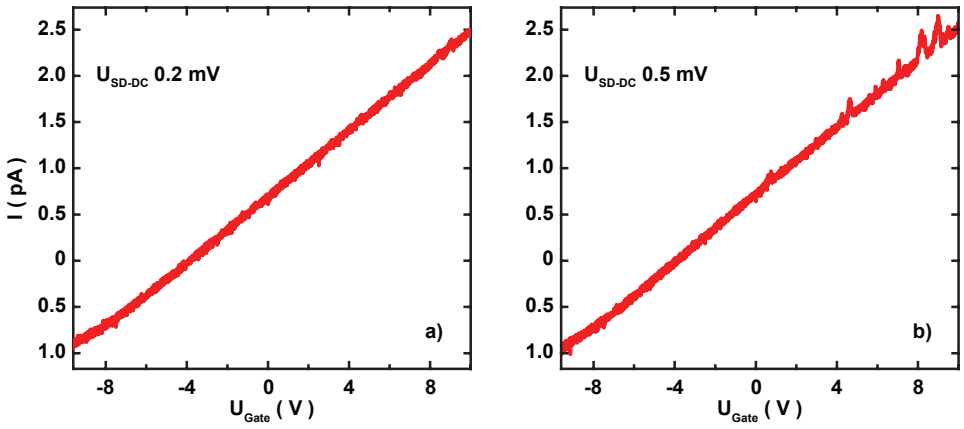

Fig. 6.10: I-U$_{Gate}$ measurements on a 250 nm wide vQDot at a DC bias voltage of a) U$_{SD}$ = 0.2 mV and b) 0.5 mV dominated by the U$_{Gate}$ dependent leakage. Coulomb oscillations are only observable for U$_{SD}$ = 0.5 mV.

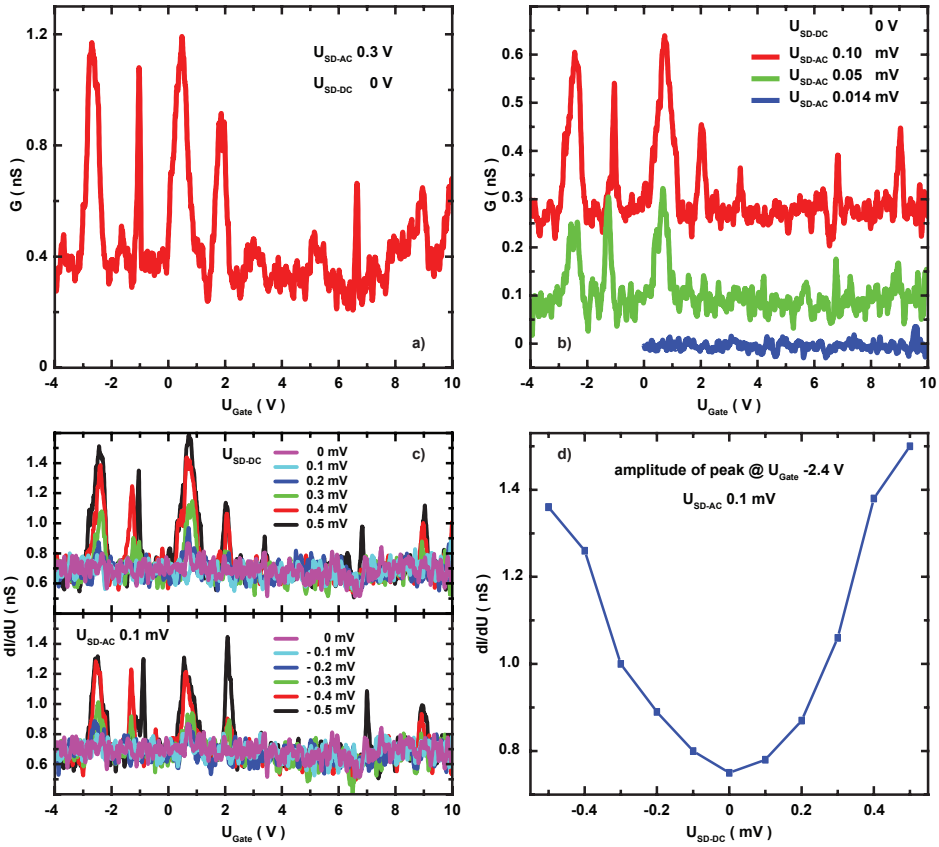

Fig. 6.11: a) G-U$_G$ measurement at $U_{SD}^{AC} = 0.3$ mV and $U_{SD}^{DC} = 0$ mV on a 250 nm wide vQDot, where the background leakage is removed by the Lock-in measurement and distinct Coulomb oscillations are observable. b) Same G-U$_G$ measurement for U_{SD}^{AC} voltages increasing from 0.014 mV to 0.1 mV showing increasing signal. c) dI/dU-U$_G$ measurement at a fixed AC excitation of $U_{SD}^{AC} = 0.1$ mV and a varying DC voltage of -0.5 mV $\leq U_{SD}^{DC} \leq$ 0.5 mV showing alternating peak intensities with the DC voltage. d) Amplitude of the Coulomb peak at U$_{Gate}$ = -2.4 V vs. U_{SD}^{DC} showing non-linear dependence.

voltage at $U_{SD} \approx 0$ V.

When performing their investigations on Coulomb oscillations in the III-V QDots Tarucha *et al.* [Taru 96] measured the source-drain current I with respect to the gate voltage U_G at a DC source-drain voltage $U_{SD} = 150$ μV. Their measurements don't show any sign of leakage and the background is flat within the gate voltage range. Unlike in the III-V case, for the II-VI QDots the study of Coulomb oscillations in the constant source-drain bias mode at $U_{SD} \approx 0$ V is not applicable. Figure 6.10 shows a I-U$_G$ scan at DC-voltages U$_{SD}$ = 0.2 mV and 0.5 mV. First, as expected the measurement is in both cases dominated by the change in leakage current as the gate voltage is swept. Second, no distinct Coulomb oscillations are noticed at U$_{SD}$ = 0.2 mV, whereas at U$_{SD}$ = 0.5 mV some Coulomb blockade peaks emerge. In both measurements any signal is strongly superimposed by the white noise in the measurement. Furthermore the difference between both curves suggests a possible blockade in series with the QDot at low bias voltage.

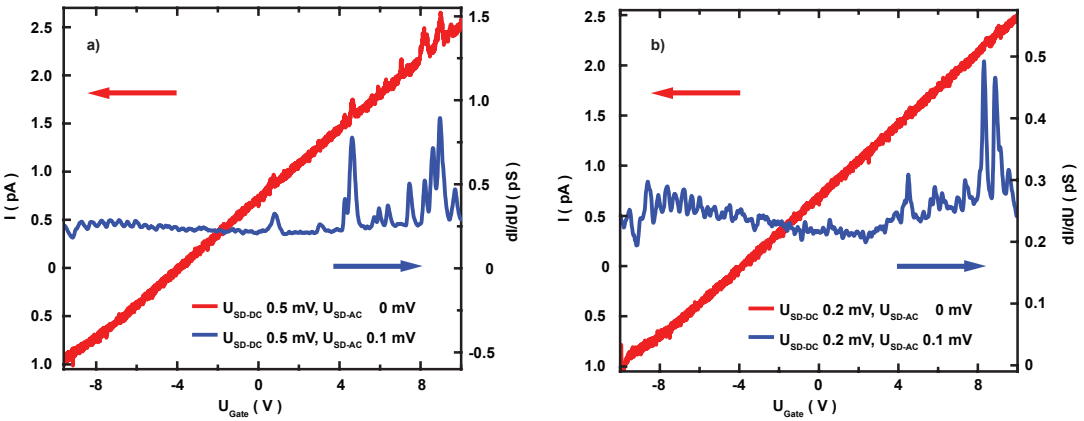

Fig. 6.12: I-U$_G$ curves at a) U_{SD}^{DC} = 0.5 mV and b) U_{SD}^{DC} = 0.2 mV with no U_{SD}^{AC} compared to the dI/dU-U$_G$ curves when U_{SD}^{AC} = 0.1 mV is added. The position of the observed Coulomb oscillations remains unaffected, but their visibility is improved.

A possibility to overcome the contributions from leakage as well as to reduce the noise level is by performing I-U$_G$ measurements with just an AC source-drain bias voltage U_{SD}^{AC} applied. Figure 6.11a displays such a I-U$_G$ measurement at U_{SD}^{AC} = 0.3 mV and U_{SD}^{DC} = 0 mV, recorded on a different more promising device than the one shown in figure 6.10. The resultant change in current through the device is then detected by a Lock-in technique while the gate voltage U_G is swept. Due to capacitative leakage in the system at frequencies above 100 Hz and the best results being obtained at low excitation frequencies, all AC-measurements are carried out at 11.3 Hz. As a result, the background from leakage is clearly removed and the signal-to-noise ratio has increased enabling the clear observation of Coulomb oscillations. Similar measurements have been performed by Tarucha *et al.* [Taru 95] in their early samples, but an AC excitation voltage of only U_{SD}^{AC} = 92 μV has been used. However, such low excitation voltages can't be applied to the II-VI QDots, because below 0.3 mV no signal is again observable. This fact once again indicates the existence of some sort of blockade in series with the QDot in these devices.

In order to reduce the necessary AC excitation voltage a combination from AC and DC bias voltage is investigated. Figure 6.11b presents dI/dU-U$_G$-measurements on the same device from figure 6.11a, where U_{SD}^{DC} = 0.5 mV and U_{SD}^{AC} is 0.014 mV, 0.05 mV and 0.1 mV. As a result, the AC excitation at 0.1 mV appears to be best suitable, since at this AC voltage the Coulomb peaks are best observable. Having established a lower AC excitation, it is also worth checking if the DC bias voltage can be further reduced. Figure 6.11c presents dI/dU-U$_G$-measurements on the same device, , where U_{SD}^{AC} = 0.1 mV and U_{SD}^{DC} is increased from 0 mV to 0.5 mV. Once again all Coulomb peaks in the investigated U$_G$ range are best observable for U_{SD}^{DC} = 0.5 mV. For $U_{SD}^{DC} \leq$ 0.2 mV the Coulomb oscillations are not visible and for 0.3 mV $\leq U_{SD}^{DC} \leq$ 0.4 mV only the more pronounced once are noticeable. Hence, for exploring the Coulomb blockade regime in these II-VI QDots the combination from AC plus DC source-drain excitation voltage with U_{SD}^{AC} = 0.1 mV at 11.3 Hz and U_{SD}^{DC} = 0.5 mV is best.

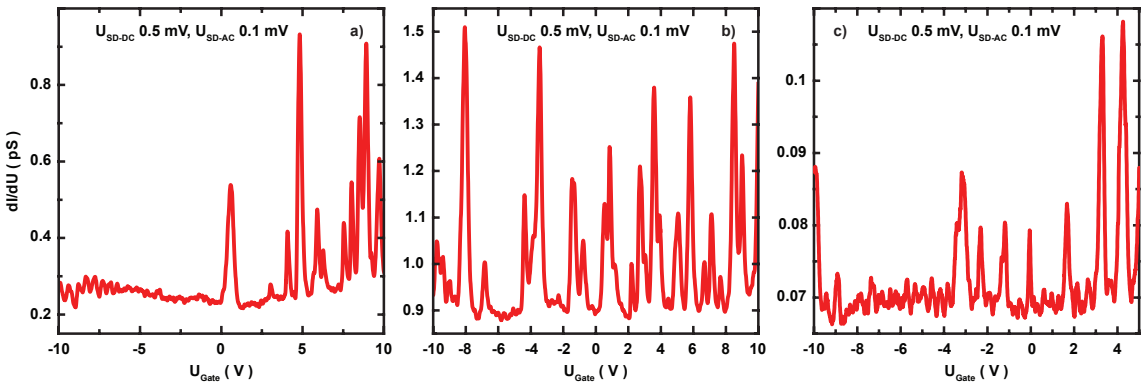

Fig. 6.13: dI/dU- U_G measurements recorded on different vQDots using the Lock-in technique and applying a source-drain bias voltage of $U_{SD}^{DC} = 0.5$ mV and $U_{SD}^{AC} = 0.1$ mV at 11.3 Hz for different 250 nm wide vQDots. The irregular spacings of the Coulomb oscillations indicate the observation of contributions from quantum confinement.

Figure 6.12a presents the U_G-sweep measurement on the device earlier presented in figure 6.10, but performed using the Lock-in method with an excitation voltage of U_{SD}^{AC} = 0.1 mV at 11.3 Hz and U_{SD}^{DC} = 0.5 mV. As expected the contribution from the leakage current is removed. Also the signal to noise ratio has been strongly improved, which now allows the clear observation of the Coulomb oscillations in the measurement. A confirmation that the combination of the source-drain bias voltage from a DC plus an AC voltage is helpfull, is given by figure 6.12b. When the U_{SD}^{AC} = 0.1 mV excitation voltage is added to the U_{SD}^{DC} = 0.2 mV, not only that the leakage and noise are removed from the measurement, but now also Coulomb oscillations appear. Nevertheless, the number of Coulomb peaks is less than in figure 6.12a, which once again indicates the existence of a blockade in the QDot at low excitation voltages. Consequently the choice of U_{SD}^{AC} = 0.1 mV at 11.3 Hz and U_{SD}^{DC} = 0.5 mV proves once again to be best to investigate the Coulomb blockade regime in the II-VI QDots.

As discussed in chapter 2.1 the addition energy, meaning the spacing between the Coulomb peaks, consists of the charging energy and the single particle energy states (see eq.2.4). As shown by Tarucha *et al.* [Taru 96] and discussed by Kouwenhoven *et al.* [Kouw 01] in few-electron QDots the spacing of the single particle energy states can be of the order of or even exceed the charging energy. This manifests itself in varying spacings of the Coulomb blockade peaks. Figure 6.13 displays dI/dU$_{SD}$-U$_G$-measurements recorded at an excitation voltage of U_{SD}^{AC} = 0.1 mV at 11.3 Hz and U_{SD}^{DC} = 0.5 mV for different devices. It is clearly observable, that the peak spacings are in all samples unequally distributed. On the one hand there is bunching observable and on the other there are also large spacings between the peaks indicating a contribution from single particle energy spacings.

In order to verify this assumption the stability diagram of each working device is recorded by performing U$_G$-U$_{SD}$-scans and plotting the determined differential conductance dI/dU$_{SD}$. As known from Kouwenhoven *et al.* [Kouw 97, Oost 99] the stability

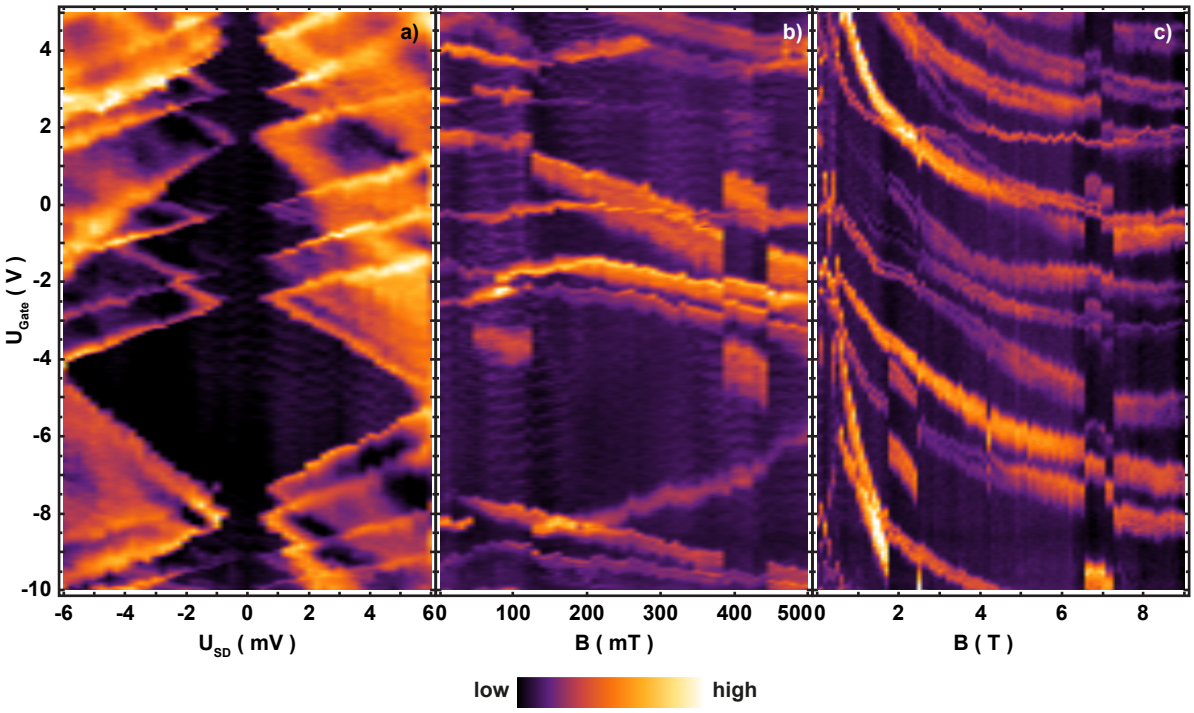

Fig. 6.14: a) dI/dU plotted in color scale in the plane of (U_G,U_{SD}^{DC}) displaying the stability diagram on a 250 nm vQDot already presented in figure 6.13c. In the black, diamond shaped areas, also denoted as Coulomb diamonds, the number of electrons on the QDot is fixed. Electronic transport occurs only at their edges. The different sizes are based on the contributions from quantum confinement in the vQDot. An intrinsic blockade in series with the QDot leads to open diamonds at bias voltages $U_{SD}^{DC} \approx 0$ mV. Evolution of the electrochemical potentials $\mu(N)$ vs. the magnetic field on this vQDot is displayed for b) low and c) high magnetic fields. The measurements are affected by telegraphic noise and the high sample resistance.

diagram consists of different sized diamonds. Inside these diamonds the number of electrons on the QDot is fixed, while at the edges of the diamonds electronic transport takes place via single-electron tunneling (upper edges: N $\rightarrow$ N + 1; lower edges: N – 1 $\rightarrow$ N). Figure 6.14a presents such a stability diagram recorded on a vQDot device. Additional Coulomb diamond diagrams are shown in appendix A and are not further discussed here, since no additional information is revealed.

The first obvious observation to be pointed out is, that within the working gate voltage range the fabricated vQDots cannot be fully emptied. The reason for this fact lies within the limited influence of the gate on the vQDot. As shown in chapter 5.1 during the introduction of the available dielectric materials, the depletion of a 100 nm thick $\sim 1 \times 10^{18}$ cm^{-3} iodine doped ZnSe is rather moderate for Si_3N_4. As a result, unlike in the Tarucha [Taru 96] devices where more than 30 electrons can be removed from the vQDot in a rather small gate voltage range, in the II-VI devices presented here only 10 to 15 electrons are removed in the entire working gate range.

A second issue is the gap at the boundary points of the Coulomb diamonds when $U_{SD} \approx$

0 mV. The size of the gap is about 1 mV and thus consistent with the previous observation, that the entire Coulomb oscillations are only observable for an applied source-drain bias voltage of $|U_{SD}| \geq 0.5$ mV. Within this gap no current passes the device, suggesting an energetic blockade, which has to be overcome before electrons can reach the actual QDot. Consulting the depicted flat band diagram from figure 2.3 as well as the simulated band diagrams from Rüth's [Ruth 11a] and Frey's [Frey 12] theses, the small barrier of $Zn_{0.97}Be_{0.03}Se$ in front of the 400 meV high $Zn_{0.75}Be_{0.25}Se$ barriers of the DBH are the most likely candidates to form the blockade. It has to be taken into account that the lateral confinement, resulting from the nano-pillar fabrication, also occurs in this layer. The formation of an additional barrier is therefore enhanced due to the now non-negligible additional depletion of the pillars sidewalls. Determining the pillar amplitude from figure 6.11c and plotting it against the applied U_{SD} voltage, as shown by figure 6.11d, the non-linear increase is an indication for this assumption. However, measurements performed at $U_{SD} = 0.5$ mV contain all Coulomb peaks and can thus be used for further characterization measurements. It has though to be pointed out that in this case no reliable information can be extracted from the shape and width of these Coulomb oscillations.

Nevertheless a third and most important observation, typical of all characterized devices, is the occurrence of differing Coulomb diamonds. As in the case of the III-V artificial atoms the size of the Coulomb diamonds is varying with the number of electrons on the vQDot. Since, as already mentioned, the addition energy has a component from the energetic spacing of the single-particle states, the observation of the different sized Coulomb diamonds indicates the observation of quantum confinement. This means the energetic spacing of the single-particle states $\Delta E_{n,l}$ is larger than the charging energy E_C of the device. Furthermore, following the interpretation of Tarucha *et al.* [Taru 96] and Kouwenhoven *et al.* [Kouw 97] the large Coulomb diamonds are an evidence of shell filling effects. Nevertheless an exact number of the electrons trapped in the vQDot is not possible, but an estimation of 10 to 20 electrons is most probable.

At this point the investigation of the Fock-Darwin spectrum of these II-VI vQDots offers a possibility to gain more insight. Figure 6.14b shows the evolution of the electrochemical potentials at low magnetic fields, $B \leq 0.5$ T. First, it is obvious at first sight that the energy levels of the QDot are strongly magnetic field dependent. There is also the interplay between the different electrochemical potentials as known from the measured Fock-Darwin spectra in the III-V QDots. Second, at a closer look there are however energy levels which don't pair with any of the other and even cross them but even cross the other, i.e. the level at $U_G \approx 0$ V. Similar behavior is also in other QDot devices visible, as shown by the scans in appendix A. This fact suggests the formation of more than one QDot in these devices and thus inhibits a clear as well as unambiguous investigation of the electrochemical potential traces. Additionally the telegraphic noise as well as high sample resistance intrinsic to the devices pose a challenge to the recording of the data, inhibiting its proper analysis. However, as shown by figure 6.14c, when the magnetic field is further increased the contribution from the Giant-Zeeman splitting becomes clearly recognizable. This fact proves the preservation of the magnetic properties of the $Zn_{0.844}Cd_{0.076}Mn_{0.08}Se$ QW and the formation of a paramagnetic vQDot. Furthermore

the magnetic behavior qualitatively resembles the calculated Fock-Darwin-spectrum from figure 2.4c, confirming the simple picture, in which the Zeeman splitting is just added to the regular single-particle energy. Even the alternating character of the calculated energy spectrum is partially reproduced at high fields. Nevertheless, again the irregular behavior of some energy level traces strengthens the assumption of the formation of at least one additional QDot.

Finally also the evolution of the quantized levels in a magnetic field should be emphasized. From findings in QW-RTDs one would naively expect to observe for each at B = 0 T degenerate single-particle energy level a set of spin-up and spin-down levels following the Brillouin shaped traces typical for Giant-Zeeman energy splitting, see fig. 2.4a. However the recorded energy spectrum vs. magnetic field, displayed in figure 6.14c, severely differs from this simplistic notion. Instead, at increasing magnetic fields the observed quantized levels in the fabricated magnetic QDots decrease to lower energies following the Brillouin dependence expected from the Giant-Zeeman energy splittings. This behavior, however is in good agreement with the calculated Fock-Darwin spectrum in figure 2.4c, which is based on the combination of the constant interaction model and the Giant-Zeeman splitting. Unlike in III-V QDots, where the Zeeman splitting is minor, here the energetic scale is dominated by the Giant-Zeeman energy, which is about one order of magnitude larger than the energy spacings from lateral confinement and charging. This fact together with the rapid evolution of the Brillouin function at low fields makes that the contribution of the spin-up levels (here the levels, which energetically increase with increasing magnetic field) to the observable Fock-Darwin spectrum is limited to the low magnetic field region. The colored graph in figure 2.4c, in which the spin-up levels are marked blue and the spin-down levels are colored red, displays the situation graphically. Therefore the energetic spectrum of the QDot levels with increasing magnetic field is strongly dependent on the Giant-Zeeman energy as the dominant energy contribution. Furthermore, from comparing the calculated Fock-Darwin spectrum to the measured energy vs. magnetic field dependence it can be concluded, that the observed levels are basically spin-down as the magnetic field is increased. Therefore, unlike the III-V QDots the II-VI artificial magnetic atoms are quickly fully spin polarized. This fact underlines once more the paramagnetic character of the fabricated QDots from the II-VI DMS (Zn,Cd,Mn)Se.

From the presented observations in the fabricated II-VI vQDots can be concluded that on the one hand artificial atoms are formed and on the other the paramagnetic properties of the DMS are still present. Though a more thorough analysis of the electronic and magnetic properties is severely limited by intrinsic device properties, the described manufacturing process enables the fabrication of artificial magnetic atoms from the II-VI DMS (Zn,Be,Cd,Mn)Se.

Chapter 7

Conclusion and Outlook

This thesis presents the detailed development of the fabrication process and the first observations of artificial magnetic atoms from the II-VI diluted magnetic semiconductor alloy (Zn,Cd,Be,Mn)Se. In order to manufacture the vQDot device which exhibits artificial atom behavior a number of development steps have to be conducted. First, the II-VI heterostructure as well as already established methods are adjusted, i.e. air-bridges. Second, state of the art vQDot fabrication techniques in the III-V material system are investigated regarding their portability to the II-VI heterostructure. And third, new approaches to the fabrication process are developed, taking into account the complexity of the heterostructure and its physical properties. These steps lead to the achievement of a working three terminal device, a gated vQDot, which shows artificial magnetic atom properties.

In the early 1990's the extensive study of III-V RTDs towards their applicability for QDots led to the development and optimization of their bandstructure for the linear transport regime. This knowledge is built on in this work to optimize the II-VI heterostructure. In this process it turns out that the increase of the QW width does not sufficiently lower the resonant level towards the Fermi energy in the leads. Instead much better results are achieved by incorporating about 7.6% Cd into the QW. The QW resonance is thus situated at the Fermi level providing the intended linear transport.

The fabrication progress in the III-V vQDots resulted in the application of $\sim$ 200 nm wide depleted line mesas, which provide the top contacting of the pillars top metal through their metal cap [Aust 96]. First, the study of the applicability of the line mesa concept to the II-VI heterostructure revealed that these semiconductor lines remain conducting to widths as small as 200 nm. This fact led to abandoning the line mesa concept and return to the air-bridge method, which is then adjusted to the particular device requirements. Second, in the course of these experiments the separating trenches manufacturing step is reconsidered and a reliable process using a protective Ti metal mask during CAIBE dry etching is introduced. Along with its robustness, it facilitates an easy way to be removed after the dry etching step by hydrofluoric acid, leaving a non-contaminated gold surface behind. Finally, the study of the line mesas and the necessity for a fabrication process resulted in manufacturing insights which eased the development of submicron pillars.

Applying again a Ti metal mask and varying the dry etching angle working pillars as small as 200 nm exhibiting a sidewall steepness of 85° have been manufactured. Normal growth to growth variations between the wafers resulted in a further development of the pillar fabrication step which avoids the use of hydrofluoric acid by using a protective resist mask during the excess Ti removal from the top contact metal. This way a more general manufacturing step for the submicron pillars, which is more tolerant to physical variation in the material, is established.

The most important element in the fabrication process is the application of the third electrode, the electrostatic gate, to enable the manipulation of the quantum levels. Unlike in the III-V vQDots, there is no known ideal Schottky contact to ZnSe and certainly not one suitable to incorporation in complex heterostructures. Therefore the available dielectrics, deposited by PECVD, are characterized in terms of their dielectric constant and occurring hysteresis. Si_3N_4 seem to be more suitable than SiO_2 in regard to the gating efficiency, but one has to deal with a pronounced hysteresis, which most likely arises from interface defects between the dielectric and the II-VI semiconductor. Furthermore the simple shadow mask deposition of the gate metal in the III-V vQDots is not transferable to the II-VI heterostructure. In the later, a severe contamination of the top metal along with a roughening of the surface occurs when trying to create the undercut by a wet etch dip in chromosulfuric acid. Thus a direct electron beam fabrication step is developed to manufacture annular gate electrodes around the insulator covered pillars. Here a very careful monitoring of etching depths and dielectric deposition rates proved to be crucial for proper influence of the gate on the QW.

Combining all fabrication steps, summarized in chapter 6, resulted in the achievement of working vQDots in the II-VI diluted magnetic semiconductor alloy (Zn,Cd,Be,Mn)Se. Along with a basic fabrication process an additional improved and more general process is outlined. Low temperature measurements in a dilution refrigerator confirm the formation of a QDot in these vertical pillars. Though a functioning gate electrode with good influence on the vQDots energy levels exists, the entire depletion of the vQDot has not yet been achieved. Additionally an unintended blockade, in series with the QDot, is clearly observable and prevents reasonable operation of the devices at bias voltages below 0.5 mV. A low energy barrier in front of the actual DBH is suspected to cause this effect. Furthermore the leakage from the gate electrode to the backside layer underneath significantly influences DC measurement and requires the application of a Lock-in method. This technique is however limited to low frequencies by the high sample resistance in our devices, which causes capacitative leakage in the cryostat leads at even moderate frequencies.

The observed Coulomb oscillations and Coulomb diamonds in these devices confirm the formation of QDots within the DBH of the pillars. Furthermore the irregular spacings between the Coulomb peaks and the varying size of the Coulomb diamonds reveal that the devices are operated in the quantum Coulomb blockade regime, where the quantization from the 3D confinement is also observable. The magnetic field dependence of these single-particle states qualitatively follows the calculated Fock-Darwin spectrum added with the Giant-Zeeman splitting in the II-VI DMS. Along with the Brillouin like behavior

of the quantized levels the domination of the spin-down contribution at high magnetic fields is clearly evident. However, due to the limitation in the devices and the observation of superimposed contributions from the formation of more than one QDot, a more quantitative analysis of the results is not possible.

However, it has to be pointed out that the original II-VI RTD heterostructure has not been developed for devices with submicron dimensions. Therefore an adaption of the RTD's heterostructure may be necessary. RTD heterostructures used for III-V vQDots [Taru 96, Kouw 01] or III-V nano-pillars with similar vertical dimensions [Wens 09] don't have a small energy barrier in front of the DBH. For this reason the layer layout has to be reconsidered. Then the presented fabrication processes for gated or non-gated submicron devices allow to verify in detail the impact of the modifications on the device performance. With the heterostructure optimized this will lead to an improved observation and investigation of the physical properties of artificial magnetic atoms.

Moreover, because of its general nature this fabrication process can easily accommodate other conformal deposition methods for dielectrics, i.e. atomic layer deposition. Then high k dielectrics, such as Al_2O_3, HfO_2 or ZrO_2, can be deposited by the ALD method. These dielectrics can provide a promising path to improve the QDot performance in the future. For example we expect, by using these high k dielectrics, to achieve the same gate action at smaller voltages.

A second advantage of the general nature of the fabrication process is the fact that it can be used on II-VI heterostructures similar to the ones used in this thesis. With this said, it can also be used to fabricate submicron pillars from RTD heterostructures containing self-assembled CdSe QDots embedded in magnetic barriers, for example. The fabrication of submicron pillars on one hand reduces the number of the electrically sampled QDots. On the other hand the application of a gate voltage allows to select a specific QDot from the ensemble. Hence, the observed physical effects [Goul 06, Ruth 11a] can then be studied by means of an applied gate voltage on a specific QDot.

Appendix A

Artificial magnetic atoms gallery

The chapter shows Coulomb diamonds and magnetic field dependent energy spectra of additionally investigated magnetic artificial atoms.

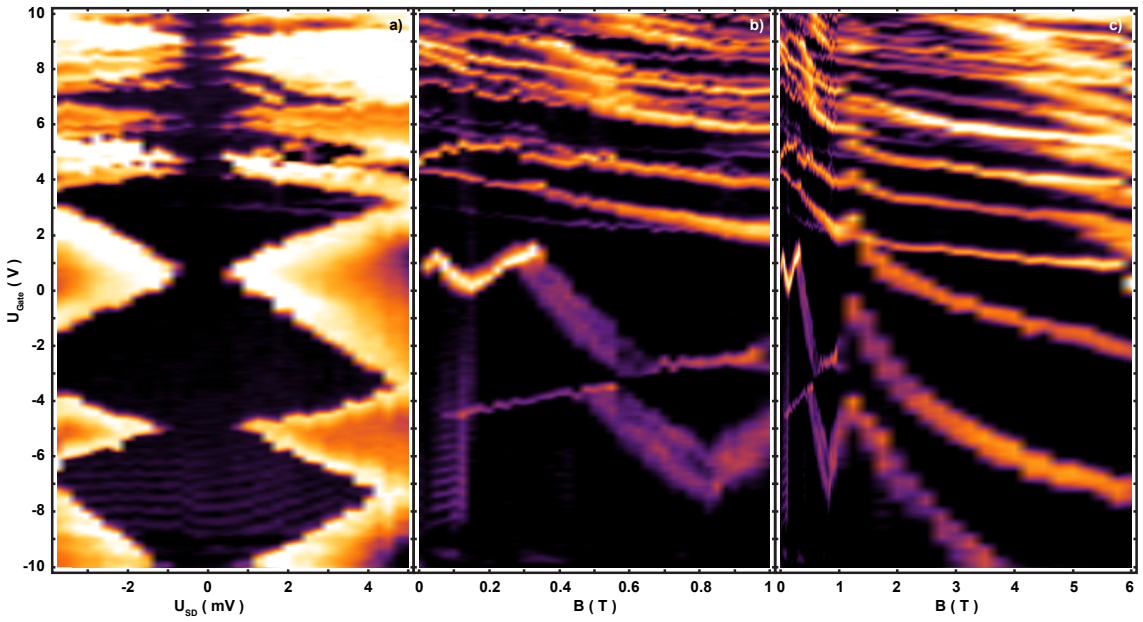

Fig. A.1: a) dI/dU plotted in color scale in the plane of (U_G,U_{SD}^{DC}) displaying the stability diagram on a 250 nm vQDot already presented in figures 6.9a-c, 6.12 and 6.13a. In the black, diamond shaped areas, also denoted as Coulomb diamonds, the number of electrons on the QDot is fixed. Electronic transport occurs only at their edges. The different sizes are based on the contributions from quantum confinement in the vQDot. An intrinsic blockade in series with the QDot leads to open diamonds at bias voltages $U_{SD}^{DC} \approx 0$ mV. Evolution of the electrochemical potentials $\mu(N)$ vs. the magnetic field on this vQDot is displayed for b) low and c) high magnetic fields. The measurements are affected by telegraphic noise and the high sample resistance.

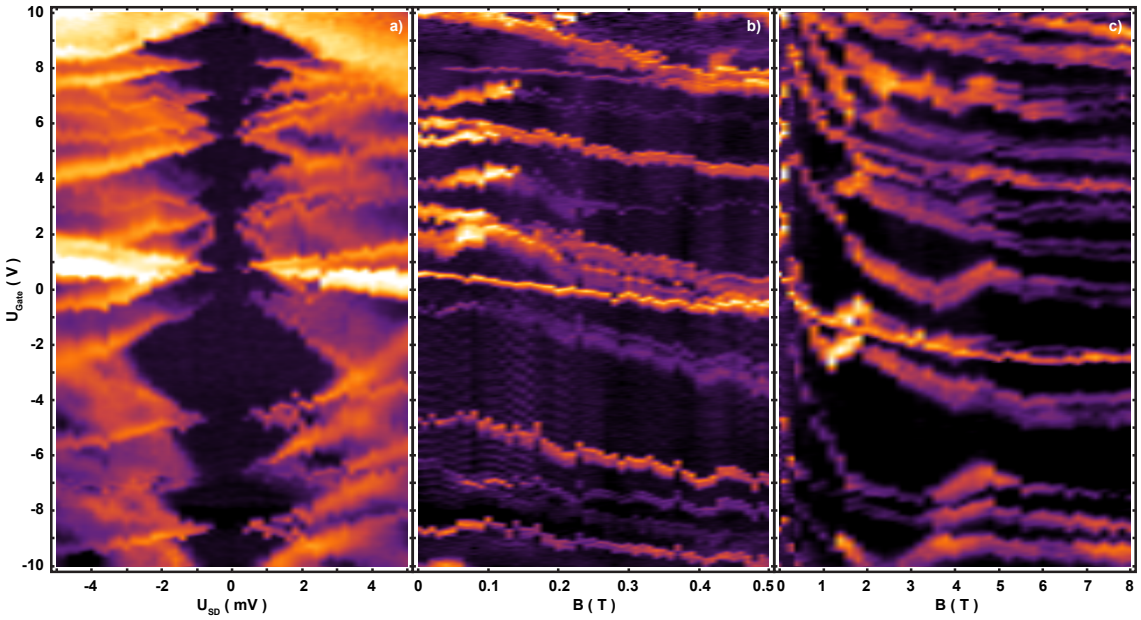

Fig. A.2: a) dI/dU plotted in color scale in the plane of (U_G,U_{SD}^{DC}) displaying the stability diagram on a 250 nm vQDot already presented in figure 6.11. In the black, diamond shaped areas, also denoted as Coulomb diamonds, the number of electrons on the QDot is fixed. Electronic transport occurs only at their edges. The different sizes are based on the contributions from quantum confinement in the vQDot. An intrinsic blockade in series with the QDot leads to open diamonds at bias voltages $U_{SD}^{DC} \approx 0$ mV. Evolution of the electrochemical potentials $\mu(N)$ vs. the magnetic field on this vQDot is displayed for b) low and c) high magnetic fields. The measurements are affected by telegraphic noise and the high sample resistance.

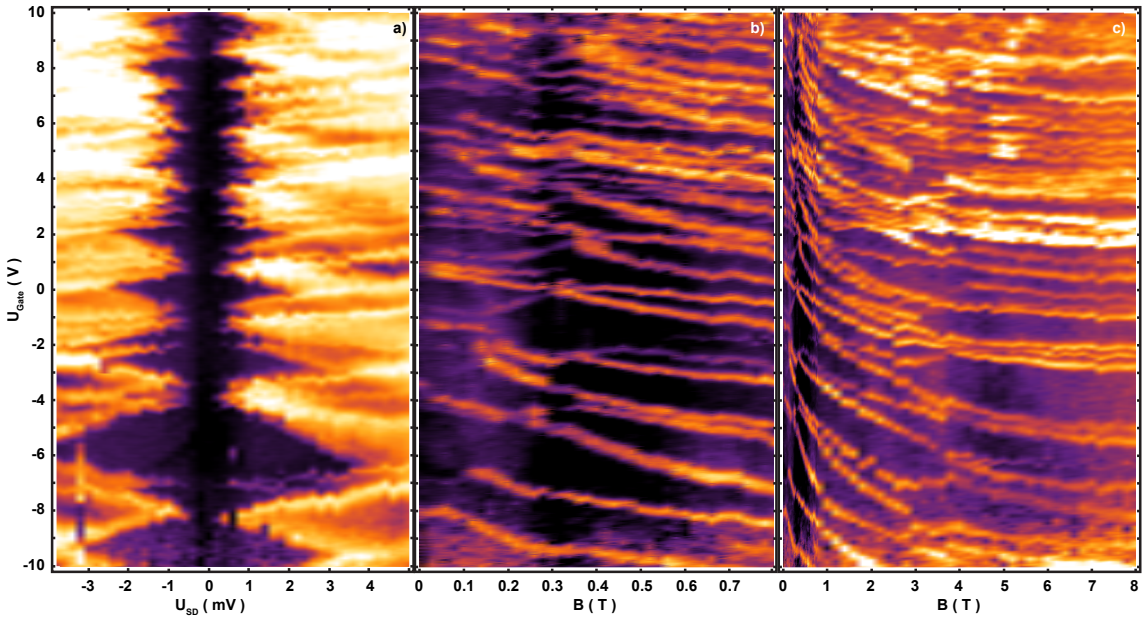

Fig. A.3: a) dI/dU plotted in color scale in the plane of (U_G,U_{SD}^{DC}) displaying the stability diagram on a 250 nm vQDot already presented in figures 6.9d-e and 6.13b. In the black, diamond shaped areas, also denoted as Coulomb diamonds, the number of electrons on the QDot is fixed. Electronic transport occurs only at their edges. The different sizes are based on the contributions from quantum confinement in the vQDot. An intrinsic blockade in series with the QDot leads to open diamonds at bias voltages $U_{SD}^{DC} \approx 0$ mV. Evolution of the electrochemical potentials $\mu(N)$ vs. the magnetic field on this vQDot is displayed for b) low and c) high magnetic fields. The measurements are affected by telegraphic noise and the high sample resistance.

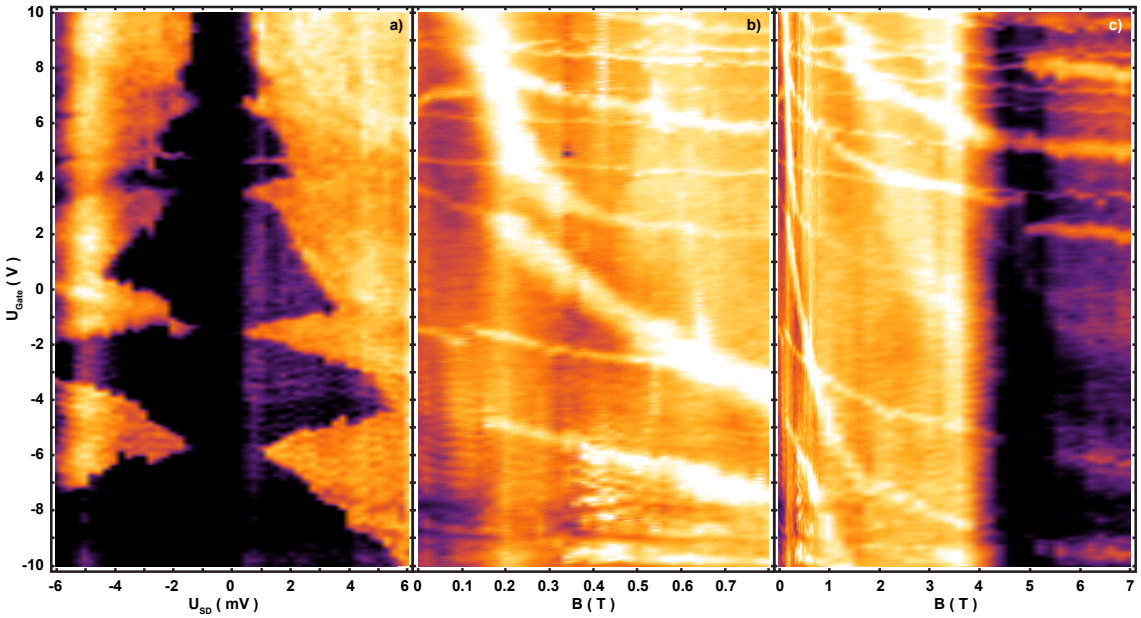

Fig. A.4: a) dI/dU plotted in color scale in the plane of (U_G,U_{SD}^{DC}) displaying the stability diagram on a 250 nm vQDot. In the black, diamond shaped areas, also denoted as Coulomb diamonds, the number of electrons on the QDot is fixed. Electronic transport occurs only at their edges. The different sizes are based on the contributions from quantum confinement in the vQDot. An intrinsic blockade in series with the QDot leads to open diamonds at bias voltages $U_{SD}^{DC} \approx 0$ mV. Evolution of the electrochemical potentials $\mu(N)$ vs. the magnetic field on this vQDot is displayed for b) low and c) high magnetic fields. The measurements are affected by telegraphic noise and the high sample resistance.

Appendix B

Alternative bridge technology for nanopillars

In the course of the development of the fabrication process of artificial atoms the issue of misalignment when contacting the ≤ 250 nm wide pillars had to be addressed. Due to the small pillar dimensions, shifts of 10 to 50 nm of the air-bridge post at the pillar site can cause an electrical contact to the gate electrode surrounding the pillar (see fig. B.2a). The resulting short between top and gate contact makes the device unusable as a gated vQDot. One possibility to overcome this threat is based on the manual correction of the

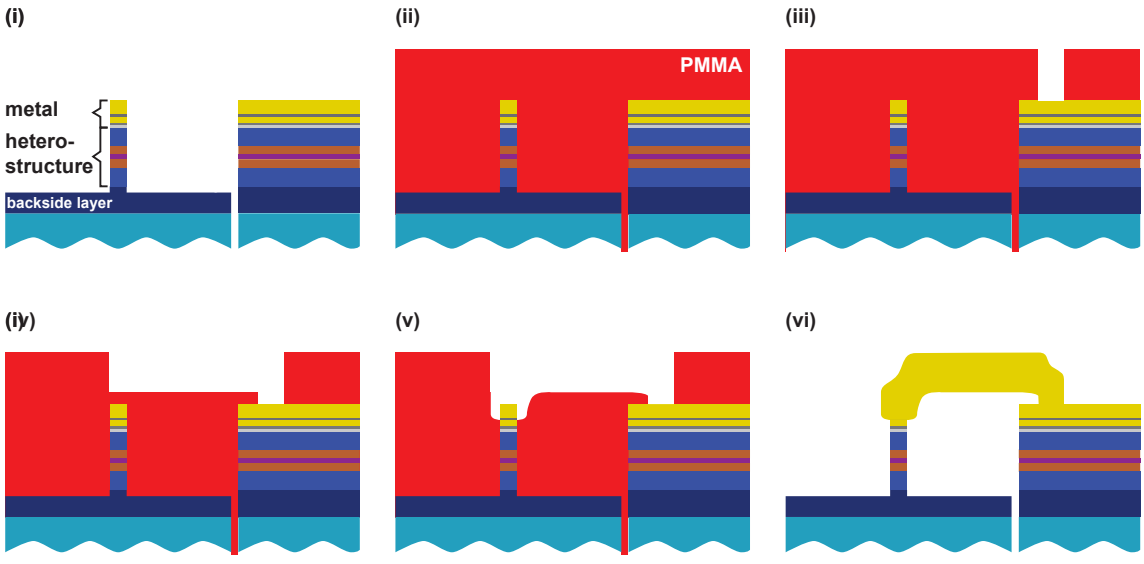

Fig. B.1: Schematics of the fabrication process of the alternative bridge technology. A device containing a nanopillar (i) is covered by a thick PMMA resist (ii). The air-bridge post is exposed by 30 kV (iii), followed by the exposure of the span using an adequate low acceleration voltage (iv). A slightly higher low acceleration voltage exposes the post at the pillar (v), but not penetrating the resist entirely. After development the air-bridge is fabricated by metal evaporation and lift-off (vi).

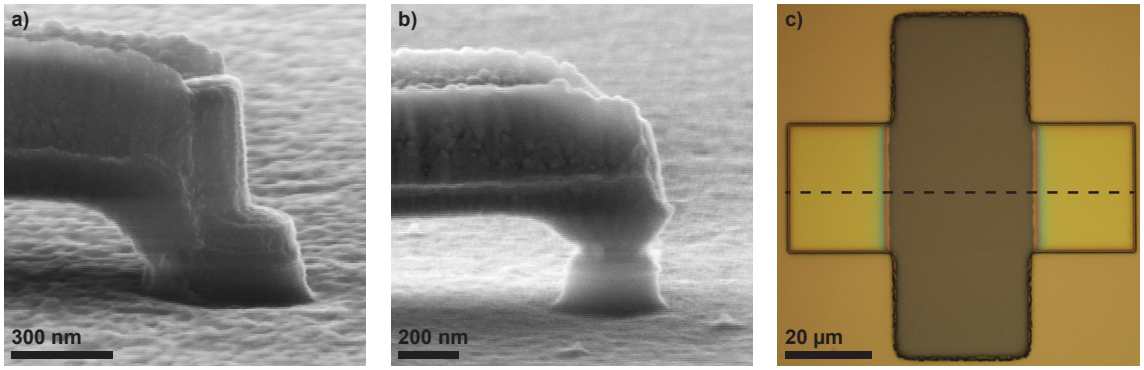

Fig. B.2: SEM micrographs a) showing a misaligned air-bridge touching the side of a 450 nm pillar and b) a 250 nm pillar connected by an air-bridge fabricated using the alternative method. c) Optical image of a test structure used to determine the protective resist thickness along the dashed line, after using the alternative technology.

shift. Since the gate electrode fabrication step as well as the air-bridge step use the same set of alignment marks, the systematic shift determined in the gate electrode step can also be corrected in the air-bridge step. But in the case that the shift is non-systematic this method can no further be applied.

In order to still guarantee a proper contact of the pillars' top contact without the threat of creating a short to the gate, the air-bridge technique developed by Borzenko [Borz 04] is modified. A schematic of the alternative air-bridge technique is depicted in figure B.1. The starting point of this fabrication step is any device ready to be fitted with an air-bridge, i.e. simply a pillar for testing purposes as shown in step i. Then the thick resist for air-bridge fabrication, in this thesis it is the earlier described 5-layer resist system from 950K (3%) (×3) and 950K (5%) (×2), is spun onto the sample, covering it with the necessary thickness (see part ii). Subsequently just the bridge post at the bonding contact is exposed by using an acceleration voltage of 30 kV (part iii). The air-bridge span is defined by exposing the pattern using a low acceleration voltage (part iv). Because of their low energy, electrons penetrate the resist as far as a certain depth. This depth has been previously determined by Borzenko for different acceleration voltages [Borz 04]. In this thesis the typical acceleration voltage used, was between 6.3 kV and 6.5 kV, dependent on the actual resist thickness. Finally the air-bridge posts at the pillar site are exposed. Instead of using an acceleration voltage of 30 kV, once again a low acceleration voltage is used. This step makes use once again of the specific penetration depth of the electrons in the resist at a given acceleration voltage, as in the case of the span fabrication. The choice of the voltage is very important at this point. It has to be higher than the one used for the span, but low enough to avoid any connection of the bridge post to the gate electrode. The optimal voltage is defined such, that after development only the pillars top contact metal protrudes the resist surface as depicted in part v of the scheme. After developing and 10 sec O_2-plasma the sample is metalized as usual with 10 nm Ti / 400 nm Au and the excess metal removed by lift-off. Part v of figure B.1 displays schematically the fabricated air-bridge. By choosing a post wider than the actual pillar diameter one

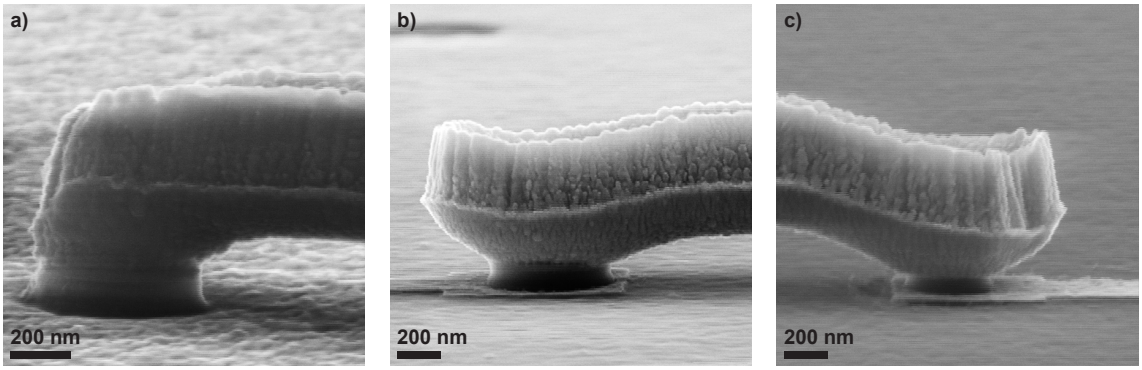

Fig. B.3: SEM micrographs of a) a 500 nm non-gated pillar, b) a 350 nm gated and c) a 250 nm gated pillar connected by an air-bridge fabricated using the alternative technology. b) and c) show that there is no connection between the air-bridge and the gate electrode.

circumvents missing the pillars top contact. Furthermore the sample surface is naturally protected by the maximum penetration depth of the electrons at a given acceleration voltage. This way a short between the air-bridge at the top and the gate is very simply avoided. A pillar connected by the described procedure is displayed in figure B.2b. It shows how the bridge is connected to the pillar by just touching its top contact.

The choice of the correct acceleration voltage for the post is verified by a test structure. The used test structure is shown in figure B.2c, where the vertical square has been exposed by kV and the horizontal one by the lower acceleration voltage used for the air-bridge post at the pillar. Right after development the resist thickness is determined with the surface profilometer Dektak6M. From the difference between the resist surface in the horizontal square and the sample surface in the vertical square, measured along the indicated dashed line, the remaining protective resist thickness is determined. In the case that this thickness is to small, the fabrication step can be repeated without any damage to the device, which adds an additional advantage to the reliability of the fabrication process.

Figure B.3 displays SEM micrographs of different devices, which used this modified bridge technique. Especially figures B.3b and B.3c show the technique applied to gated samples. It is clear that while the pillar's top is contacted there is no connection between the air-bridge and the gate electrode, which proves the reliability of the method.

Appendix C

Process recipes

C.1 Basic process

A) **Cleaning & contact enhancement**

a) Rinsing with Acetone (Ace) and Isopropanol (IPA)

b) Chemical cleaning: preheated Methyl isobutyl ketone (MIBK) @ 80 °C for ∼15 min

c) Plasma cleaning : 10 sec Reactive Ion Etching (RIE) O_2-plasma @ 20 W (program 'Miniclean')

d) Metalization: 7 nm Ti / 80 nm Au

B) **E-beam exposure of global & local marks (PMMA - positive process)**

a) Resist: PMMA 950K (5%), 40 sec @ 5000 rpm, 15 min @ 200 °C

b) Exposure: 30 kV (accel. volt.), 10 μm (aperture), 81.92 μm (working field), 4 pixel (5 nm) (step size), 450 $\mu As/cm^2$ (dose)

c) Development: 60 sec IPA (solvent), 2 min H_2O

d) Metalization: 165 nm Ti

e) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

f) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

g) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

C) **E-beam exposure of trenches (AR4060 - negative process)**

a) Resist:

i) Hexamethyldisiloxane (HMDS) coating and 20 sec wait, 40 sec @ 5000 rpm

ii) AR4060 40 sec @ 4000 rpm, 15 min @ 90 °C (using fresh bottled resist)

b) Exposure:
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 300 μAs/cm^2
   ii) 30 kV, 60 μm, 819.2 μm, 2 pixel (25 nm), 310 μAs/cm^2
   iii) 30 kV, 60 μm, 81.92 μm, 16 pixel (20 nm), 310 μAs/cm^2 (windows for resist thickness measurement)

c) Development:
   i) Reversal bake: 5 min @ 105 °C
   ii) UV-exposure: 25 sec
   iii) Developing: 60 sec AR300-26:H_2O (1:4), 5 min H_2O

d) Resist thickness measurement (RTM) with Dektak6M (profilometer) (expected thickness: $\sim$ 660 nm)

e) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) Metalization: 165 nm Ti

g) Lift-off: preheated Ace @ 50 °C for $\sim$30 min, low power 2 sec ultrasonic pulses (US-pulses) every 5 min, IPA

h) Metal thickness measurement (MTM) with Dektak6M

D) **Etching trenches with Chemical Assisted Ion Beam Etching (CAIBE)**

a) CAIBE dry etching
   i) 3 min 35 sec Ar-etch @ 90° (program GD_Ar3)
   ii) 19 min BCl_3 assisted Ar-etch @ 90° (program GD_RTD4)

b) H_2O-rinse for 10 min

c) Etch depth measurement (EDM) with Dektak6M: Ti - Semiconductor

d) Wet etch of Ti metal mask: $\sim$25 sec HF:H_2O (1:200), 5 min H_2O

e) EDM with Dektak6M: Au - Semiconductor

f) Chemical cleaning: preheated MIBK @ 80 °C for $\sim$30 min

E) **E-beam exposure of pillars & top bonding contacts (PMMA - positive process)**

a) Resist:
   i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C
   ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C
   iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 800 μAs/cm^2 (pillars)

ii) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 μAs/cm^2 (bonding contacts)

iii) 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 μAs/cm^2 (windows for EDM)

c) Development: 60 sec IPA, 2 min H_2O

d) Plasma cleaning: 7 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

e) Metalization: 65 nm Ti

f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

g) MTM with Dektak6M: Ti - Au

F) **Etching pillars with CAIBE**

a) CAIBE dry etching with program Gabriel01RTD70deg

i) 3 min 35 sec Ar-etch @ 70° (program GD_Ar3)

ii) ∼1 min BCl_3 assisted Ar-etch @ 70° (program GD_RTD4)
(prior to etching, calculation of etching time including the subsequent wet etching step)
(testing the times with the aid of a second piece of wafer beforehand)

iii) EDM with Dektak6M: Ti - Semiconductor

iv) H_2O-rinse for 10 min

v) Wet etching: 3 - 5 sec $K_2Cr_2O_7$+H_2SO_4, 5 min H_2O

vi) EDM with Dektak6M: Ti - Semiconductor

G) **Backside contacts & Ti mask removal (optical lithography - positive process)**

a) Resist: AR4040 40 sec @ 5000 rpm, 2 min @ 94 °C

b) UV-exposure: 14 sec

c) Development: 23 sec AR300-26:H_2O (1:4), 5 min H_2O

d) Metalization: 10 nm Ti / 120 nm Au

e) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

f) Wet etch of Ti metal mask: 5 - 20 sec HF:H_2O (1:200) (dependent of Ti mask thickness, optical check), 5 min H_2O

g) EDM with Dektak6M: Au - Semiconductor

H) **Ti adhesion layer (optical lithography - positive process)**

a) Resist: AR4040 40 sec @ 5000 rpm, 2 min @ 94 °C

b) UV-exposure: 14 sec

c) Development: 23 sec AR300-26:H_2O (1:4), 5 min H_2O

d) Metalization: 1 - 2 nm Ti

e) 1 min @ air, 10 min in pure O_2 environment, 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

I) **Insulator deposition**

a) PECVD Si_3N_4 @ 200 °C
(deposition time dependent on required thickness determined from EDM)

J) **E-beam exposure of gate (PMMA - positive process)**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:

c) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 600 $\mu As/cm^2$

d) Development: 60 sec IPA, 2 min H_2O

e) Metalization: 5 nm Ti / 10 nm Au

f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

g) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

h) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

K) **E-beam exposure of gate bonding pads (PMMA - positive process)**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:

c) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 $\mu As/cm^2$

d) Development: 60 sec IPA, 2 min H_2O

e) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) Metalization: 10 nm Ti / 120 nm Au

g) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

h) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

i) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

L) **Removal of insulator on pillar top & bonding contacts**

a) Resist:
   i) PMMA 950K (3%), 40 sec @ 5000 rpm, 1 min @ 200 °C (×3)
   ii) PMMA 950K (5%), 40 sec @ 6000 rpm, 1 min @ 200 °C
   iii) PMMA 950K (5%), 40 sec @ 5000 rpm, 60 min @ 200 °C

b) Exposure: (opening marks & bonding contacts)
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (local marks)
   ii) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 1000 μAs/cm^2 (bonding contacts)
   iii) 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 μAs/cm^2 (windows for RTM & global marks)

c) Development: 4 min AR600-56:IPA (1:1), 10 sec IPA

d) Exposure: 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (opening pillar top)

e) Development: 4 min AR600-56:IPA (1:1) (2 sec US-pulses every 45 sec), 10 sec IPA

f) Insulator etching: (for 50 nm insulator: sequence ×2)
   i) 30 sec RIE CHF_3:O_2 (5:1)-plasma @ 30 W (program 'SiN-etch')
   ii) 40 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

g) CAIBE dry etch: 10 sec Ar-etch @ 90° (program GD_Ar3)

h) Chemical cleaning: 30 min AR300-72 (N-Ethyl-2-pyrrolidon (NEP)@ 60 °C (low power 2 sec US-pulses every 5 min))

i) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

j) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

M) **E-beam exposure of bridges for pillars & gates (PMMA - positive process)**

a) Resist:
   i) PMMA 950K (3%), 40 sec @ 5000 rpm, 1 min @ 200 °C (×3)
   ii) PMMA 950K (5%), 40 sec @ 6000 rpm, 1 min @ 200 °C
   iii) PMMA 950K (5%), 40 sec @ 5000 rpm, 60 min @ 200 °C

b) Exposure: (opening marks)
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (local marks)
   ii) 30 kV, 60 μm, 81.92 μm, 16 pixel (20 nm), 1000 μAs/cm^2 (windows for RTM & global marks)

c) Development: 4 min AR600-56:IPA (1:1), 10 sec IPA

d) RTM with Dektak6M

e) Exposure: (bridges)

   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (posts)

   ii) low acceleration voltage (6.1 - 6.4 kV), 10 μm, 81.92 μm, 16 pixel (20 nm), 1000 μAs/cm^2 (span)

f) Development: 4 min AR600-56:IPA (1:1) (2 sec US-pulses every 45 sec), 10 sec IPA

g) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

h) Metalization: 10 nm Ti / 410 nm Au

i) Lift-off: preheated Ace @ 50 °C for ∼30 min, IPA

j) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

k) Plasma cleaning: 30 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

N) **Wire Bonding**

a) Top and backside bonding contacts: normal bonding method

b) Gate bonding contacts: soft bonding method

C.2 Improved process

A) **Cleaning & contact enhancement**

a) Rinsing with Acetone (Ace) and Isopropanol (IPA)

b) Chemical cleaning: preheated Methyl isobutyl ketone (MIBK) @ 50 °C for ∼15 min

c) Plasma cleaning : 10 sec Reactive Ion Etching (RIE) O_2-plasma @ 20 W (program 'Miniclean')

d) Metalization: 5 nm Ti / 100 nm Au

B) **E-beam exposure of global & local marks (PMMA - positive process)**

a) Resist: PMMA 950K (5%), 40 sec @ 5000 rpm, 15 min @ 200 °C

b) Exposure: 30 kV (accel. volt.), 10 μm (aperture), 81.92 μm (working field), 4 pixel (5 nm) (step size), 450 $\mu As/cm^2$ (dose)

c) Development: 60 sec IPA (solvent), 2 min H_2O

d) Metalization: 160 nm Ti

e) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

f) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

g) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

C) **E-beam exposure of trenches (AR4060 - negative process)**

a) Resist:

i) Hexamethyldisiloxane (HMDS) coating and 20 sec wait, 40 sec @ 5000 rpm

ii) AR4060 40 sec @ 4000 rpm, 15 min @ 90 °C (using fresh bottled resist)

b) Exposure:

i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 300 $\mu As/cm^2$

ii) 30 kV, 60 μm, 819.2 μm, 2 pixel (25 nm), 310 $\mu As/cm^2$

iii) 30 kV, 60 μm, 81.92 μm, 16 pixel (20 nm), 310 $\mu As/cm^2$ (windows for resist thickness measurement)

c) Development:

i) Reversal bake: 5 min @ 105 °C

ii) UV-exposure: 25 sec

iii) Developing: 60 sec AR300-26:H_2O (1:4), 5 min H_2O

d) Resist thickness measurement (RTM) with Dektak6M (profilometer) (expected thickness: ∼ 660 nm)

e) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) Metalization: 130 nm Ti

g) Lift-off: preheated Ace @ 50 °C for ∼30 min, low power 2 sec ultrasonic pulses (US-pulses) every 5 min, IPA

h) Metal thickness measurement (MTM) with Dektak6M

D) **Etching trenches with Chemical Assisted Ion Beam Etching (CAIBE)**

a) CAIBE dry etching

i) 3 min 35 sec Ar-etch @ 90° (program GD_Ar3)

ii) 19 min BCl_3 assisted Ar-etch @ 90° (program GD_RTD4)

b) H_2O-rinse for 10 min

c) Etch depth measurement (EDM) with Dektak6M: Ti - Semiconductor

d) Wet etch of Ti metal mask: ∼25 sec HF:H_2O (1:200), 5 min H_2O

e) EDM with Dektak6M: Au - Semiconductor

f) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

E) **E-beam exposure of pillars & top bonding contacts (PMMA - positive process)**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:

i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 800 $\mu As/cm^2$ (pillars)

ii) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 $\mu As/cm^2$ (bonding contacts)

iii) 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 $\mu As/cm^2$ (windows for EDM)

c) Development: 60 sec IPA, 2 min H_2O

d) Plasma cleaning: 7 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

e) Metalization: 65 nm Ti

f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

g) MTM with Dektak6M: Ti - Au

F) **Etching pillars with CAIBE**

a) CAIBE dry etching with program Gabriel01RTD70deg

i) 3 min 35 sec Ar-etch @ 70° (program GD_Ar3)

ii) ∼1 min BCl_3 assisted Ar-etch @ 70° (program GD_RTD4)
(prior to etching, calculation of etching time including the subsequent wet etching step)
(testing the times with the aid of a second piece of wafer beforehand)
iii) EDM with Dektak6M: Ti - Semiconductor
iv) H_2O-rinse for 10 min
v) Wet etching: 3 - 5 sec $K_2Cr_2O_7$+H_2SO_4, 5 min H_2O
vi) EDM with Dektak6M: Ti - Semiconductor

G) **Backside contacts (optical lithography - positive process)**

a) Resist: AR4040 40 sec @ 5000 rpm, 2 min @ 94 °C
b) UV-exposure: 14 sec
c) Development: 23 sec AR300-26:H_2O (1:4), 5 min H_2O
d) Metalization: 10 nm Ti / 120 nm Au
e) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

H) **Ti adhesion layer (optical lithography - positive process)**

a) Resist: AR4040 40 sec @ 5000 rpm, 2 min @ 94 °C
b) UV-exposure: 14 sec
c) Development: 23 sec AR300-26:H_2O (1:4), 5 min H_2O
d) Metalization: 1 - 2 nm Ti
e) 1 min @ air, 10 min in pure O_2 environment, 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')
f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

I) **Removing Ti mask**

a) Resist:
i) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C
ii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C
b) Exposure:
i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 400 $\mu As/cm^2$ (small field bonding contacts)
ii) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 $\mu As/cm^2$ (bonding contacts)
iii) 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 $\mu As/cm^2$ (windows for EDM & @ global marks)
c) Development: 60 sec IPA, 2 min H_2O

d) RTM with Dektak6M

e) Wet etch of Ti mask on bonding contacts: ∼25 sec HF:H_2O (1:200), 5 min H_2O

f) RTM with Dektak6M (@ global marks)

g) Plasma cleaning: 8 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

h) RTM with Dektak6M (@ global marks)
(repeat last two steps if necessary, until the resist thickness is smaller than the global marks height)

i) CAIBE dry etch: 45 sec Ar-etch @ 70° (program GD_Ar3)

j) Chemical cleaning: 30 min AR300-72 (N-Ethyl-2-pyrrolidon (NEP)@ 80 °C (low power 2 sec US-pulses every 5 min))

k) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

J) **Insulator deposition**

a) PECVD Si_3N_4 @ 200 °C
(deposition time dependent on required thickness determined from EDM)

K) **E-beam exposure of gate (PMMA - positive process)**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:

c) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 600 $\mu As/cm^2$

d) Development: 60 sec IPA, 2 min H_2O

e) Metalization: 5 nm Ti / 10 nm Au

f) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

g) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

h) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

L) **E-beam exposure of gate bonding pads (PMMA - positive process)**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 6000 rpm, 30 min @ 180 °C

b) Exposure:

c) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 μAs/cm^2

d) Development: 60 sec IPA, 2 min H_2O

e) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) Metalization: 10 nm Ti / 120 nm Au

g) Lift-off: preheated Ace @ 50 °C for ∼15 min, IPA

h) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

i) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

M) **Removal of metal & insulator on pillar top**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 6000 rpm, 15 min @ 200 °C

ii) PMMA 950K (3%), 40 sec @ 6000 rpm, 15 min @ 180 °C

b) Exposure: 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 μAs/cm^2 (windows for RTM & global marks)

c) Development: 60 sec IPA , 2 min H_2O

d) RTM with Dektak6M

e) Plasma cleaning: 8 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) RTM with Dektak6M
(repeat last two steps if necessary, until the resist thickness is smaller than the global marks height)

g) CAIBE dry etch: 15 sec Ar-etch @ 70° (program GD_Ar3)

h) RTM with Dektak6M

i) Insulator etching: (for 50 nm insulator: sequence ×2)

i) 30 sec RIE CHF_3:O_2 (5:1)-plasma @ 30 W (program 'SiN-etch')

ii) 40 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

j) RTM with Dektak6M

k) Chemical cleaning: 30 min AR300-72 (N-Ethyl-2-pyrrolidon (NEP)@ 60 °C (low power 2 sec US-pulses every 5 min))

l) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

N) **Removal of insulator on bonding contacts**

a) Resist:

i) PMMA 600K (4%), 40 sec @ 5000 rpm, 1 min @ 200 °C

ii) PMMA 600K (4%), 40 sec @ 6000 rpm, 30 min @ 200 °C

iii) PMMA 950K (3%), 40 sec @ 5000 rpm, 30 min @ 200 °C

b) Exposure: (opening marks & bonding contacts)
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 400 μAs/cm^2 (local marks)
   ii) 30 kV, 120 μm, 819.2 μm, 2 pixel (25 nm), 550 μAs/cm^2 (bonding contacts)
   iii) 30 kV, 120 μm, 81.92 μm, 16 pixel (20 nm), 550 μAs/cm^2 (windows for RTM & global marks)

c) Development: 60 sec IPA, 2 min H_2O

d) RTM with Dektak6M

e) Plasma cleaning: 5 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

f) RTM with Dektak6M

g) Insulator etching: (for 50 nm insulator: sequence $\times 2$)
   i) 30 sec RIE CHF_3:O_2 (5:1)-plasma @ 30 W (program 'SiN-etch')
   ii) 40 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

h) RTM with Dektak6M

i) CAIBE dry etch: 15 sec Ar-etch @ 70° (program GD_Ar3)

j) Plasma cleaning: 30 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

k) Chemical cleaning: 30 min AR300-72 (N-Ethyl-2-pyrrolidon (NEP)@ 50 °C (low power 2 sec US-pulses every 5 min))

l) Chemical cleaning: preheated MIBK @ 80 °C for $\sim$30 min

m) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

O) **E-beam exposure of bridges for pillars & gates (PMMA - positive process)**

a) Resist:
   i) PMMA 950K (3%), 40 sec @ 5000 rpm, 1 min @ 200 °C ($\times 3$)
   ii) PMMA 950K (5%), 40 sec @ 6000 rpm, 1 min @ 200 °C
   iii) PMMA 950K (5%), 40 sec @ 5000 rpm, 60 min @ 200 °C

b) Exposure: (opening marks)
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (local marks)
   ii) 30 kV, 60 μm, 81.92 μm, 16 pixel (20 nm), 1000 μAs/cm^2 (windows for RTM & global marks)

c) Development: 4 min AR600-56:IPA (1:1), 10 sec IPA

d) RTM with Dektak6M

e) Exposure: (bridges)
   i) 30 kV, 10 μm, 81.92 μm, 4 pixel (5 nm), 1000 μAs/cm^2 (posts)
   ii) low acceleration voltage (6.1 - 6.4 kV), 10 μm, 81.92 μm, 16 pixel (20 nm), 1000 μAs/cm^2 (span)

f) Development: 4 min AR600-56:IPA (1:1) (2 sec US-pulses every 45 sec), 10 sec IPA

g) Plasma cleaning: 10 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

h) Metalization: 10 nm Ti / 410 nm Au

i) Lift-off: preheated Ace @ 50 °C for ∼30 min, IPA

j) Chemical cleaning: preheated MIBK @ 80 °C for ∼30 min

k) Plasma cleaning: 30 sec RIE O_2-plasma @ 20 W (program 'Miniclean')

P) **Wire Bonding**

a) Top and backside bonding contacts: normal bonding method

b) Gate bonding contacts: soft bonding method

Bibliography

[Albe 05] K. F. Albertin and I. Pereyra. *Microelectronic Engineering*, Vol. 77, pp. 144 – 149, 2005.

[Asho 96] R. C. Ashoori. *Nature*, Vol. 379, pp. 413 – 419, 1996.

[Asta 02] G. V. Astakhov, D. R. Yakovlev, V. P. Kochereshko, W. Ossau, W. Faschinger, J. Puls, F. Henneberger, S. A. Crooker, Q. McCulloch, D. Wolverson, N. A. Gippius, and A. Waag. *Physical Review B*, Vol. 65, p. 165335, 2002.

[Aust 96] D. G. Austing, T. Honda, and S. Tarucha. *Semiconductor Science and Technology*, Vol. 11, pp. 388 – 392, 1996.

[Aust 97] D. G. Austing, T. Honda, and S. Tarucha. *Semiconductor Science and Technology*, Vol. 12, No. 5, pp. 631 – 637, 1997.

[Bass 83] E. Bassous, L. M. Ephrath, G. Pepper, and D. J. Mikalsen. *Journal of The Electrochemical Society*, Vol. 130, pp. 478 – 484, 1983.

[Bent 92] P. H. Benton, L. Eaves, and P. C. Main. *Physical Review Letters*, Vol. 69, p. 2995, 1992.

[Born 90] D. E. Bornside. *Journal of The Electrochemical Society*, Vol. 137, pp. 2589 – 2595, 1990.

[Borz 03] T. Borzenko, F. Lehmann, G. Schmidt, and L. W. Molenkamp. *Microelectronic Engineering*, Vol. 67, pp. 720 – 727, 2003.

[Borz 04] T. Borzenko, C. Gould, G. Schmidt, and L. Molenkamp. *Microelectronic Engineering*, Vol. 75, pp. 210 – 215, 2004.

[Borz 05] T. Borzenko, V. Hock, D. Supp, C. Gould, G. Schmidt, and L. Molenkamp. *Microelectronic Engineering*, Vol. 78 - 79, pp. 374 – 380, 2005.

[Borz 07] T. Borzenko, T. Slobodskyy, D. Supp, C. Gould, G. Schmidt, and L. W. Molenkamp. *Microelectronic Engineering*, Vol. 84, pp. 1566 – 1569, 2007.

[Brus 01] P. Bruschi, A. Diligenti, and M. Piotto. *Microelectronic Engineering*, Vol. 57, pp. 959 – 965, 2001.

[Chan 74] L. Chang, L. Esaki, and R. Tsu. *Applied Physics Letters*, Vol. 24, pp. 593 – 595, 1974.

[Chau 00] C. Chauvet, Tournié, and J.-P. Faurie. *Physical Review B*, Vol. 61, pp. 5332 – 5336, 2000.

[Chot 82] T. Chot. *Physica Status Solidi A*, Vol. 70, pp. 311 – 316, 1982.

[Cior 00] M. Ciorga, A. S. Sachrajda, P. Hawrylak, C. Gould, P. Zawadski, S. Jullian, Y. Feng, and Z. Wasilewki. *Physical Review B*, Vol. 61, pp. R16315 – R16318, 2000.

[Darw 30] C. G. Darwin. *Proceedings of the Cambridge Philosophical Society*, Vol. 27, pp. 86 – 90, 1930.

[Dell 91] M. W. Dellow, P. H. Benton, M. Henini, P. C. Main, L. Eaves, S. P. Beaumont, and C. D. W. Wilkinson. *Electronic Letters*, Vol. 27, pp. 134 – 136, 1991.

[Dell 92a] M. W. Dellow, P. H. Benton, C. J. G. M. Langerak, T. J. Foster, P. C. Main, L. Eaves, M. Henini, S. P. Beaumont, and C. D. W. Wilkinson. *Physical Review Letters*, Vol. 68, pp. 1754 – 1757, 1992.

[Dell 92b] M. W. Dellow, P. H. Benton, P. C. Main, T. J. Forster, L. Eaves, A. F. Jezierski, W. Kool, M. Henini, S. P. Beaumont, and C. D. W. Wilkinson. *Semiconductor Science and Technology*, Vol. 7, pp. B442 – B445, 1992.

[Deng 12] R.-G. Dengel, A. Frey, K. Brunner, C. Gould, and L. W. Molenkamp. *Nanotechnology*, Vol. 23, p. 395301, 2012.

[Dhar 98] I. M. Dharmadasa. *Progress in Crystal Growth and Characterization of Materials*, Vol. 36, pp. 249 – 290, 1998.

[Dula 91] J. Dulak, B. J. Howard, and C. Steinbrüchel. *Journal of Vacuum Science and Technology A*, Vol. 9, pp. 775 – 778, 1991.

[Esak 58] Esaki. *Physical Review*, Vol. 109, pp. 603 – 604, 1958.

[Farr 91] H. H. Farrell, M. C. Tamargo, J. L. de Miguel, F. S. Turco, D. M. Hwang, and R. E. Nahory. *Journal of Applied Physics*, Vol. 69, No. 10, pp. 7021 – 7028, 1991.

[Feng 99] Y. Feng, A. S. Sachrajda, P. Zawadski, S. Kolind, J. H. Buchanan, M. Smet, J. Lapointe, and P. A. Marshall. *Journal of Vacuum Science and Technology B*, Vol. 17, pp. 3231 – 3234, 1999.

[Fock 28] V. Fock. *Zeitschrift für Physik*, Vol. 47, pp. 446 – 448, 1928.

[Ford 88] C. J. B. Ford, T. J. Thornton, R. Newbury, M. Pepper, and A. H. *Supperlattices and Microstructures*, Vol. 4, pp. 541 – 544, 1988.

[Fran 02] G. Franz, R. Kachel, and S. Sotier. *Materials Science in Semiconductor Processing*, Vol. 5, pp. 45 – 50, 2002.

[Frey 09] A. Frey, F. Lehmann, P. Grabs, C. Gould, G. Schmidt, K. Brunner, and L. W. Molenkamp. *Semiconductor Science and Technology*, Vol. 24, p. 035005, 2009.

[Frey 10a] A. Frey, U. Bass, S. Mahapatra, C. Schumacher, J. Geurts, and K. Brunner. *Physical Review B*, Vol. 82, p. 195318, 2010.

[Frey 10b] A. Frey, M. Ruth, R.-G. Dengel, C. Schumacher, C. Gould, G. Schmidt, K. Brunner, and L. W. Molenkamp. *Journal of Crystal Growth*, Vol. 312, pp. 1036 – 1039, 2010.

[Frey 12] A. Frey. *Spin-dependen tunneling and heterovalent heterointerface effects in diluted magnetic II-VI semiconductor heterostructures*. PhD thesis, Julius-Maximilians-Universität Würzburg, 2012.

[Furd 87] J. K. Furdyna and N. Samarth. *Journal of Applied Physics*, Vol. 61, pp. 3526 – 3531, 1987.

[Furd 88] J. K. Furdyna. *Journal of Applied Physics*, Vol. 64, pp. R29 – R64, 1988.

[Gaj 79] J. A. Gaj, R. Planel, and G. Fishman. *Solid State Communications*, Vol. 29, pp. 435 – 438, 1979.

[Gloe 75] P. G. Gloersen. *Journal of Vacuum Science and Technology*, Vol. 12, pp. 28 – 36, 1975.

[Gold 87] V. J. Goldman, D. C. Tsui, and J. E. Cunningham. *Physical Review B*, Vol. 36, pp. 7635 – 7637, 1987.

[Goul 06] C. Gould, A. Slobodskyy, D. Supp, T. Slobodskyy, P. Grabs, P. Hawrylak, F. Qu, G. Schmidt, and L. W. Molenkamp. *Physical Review Letters*, Vol. 97, p. 017202, 2006.

[Goul 98] C. Gould, P. Hawrylak, A. S. Sachrajda, Y. Feng, and Z. Wasilewki. *Physica B: Condensed Matter*, Vol. 256, p. 141, 1998.

[Guer 92a] P. Gueret, N. Blanc, T. Gerhard, and H. Rothuizen. *Physical Review Letters*, Vol. 68, pp. 1896 – 1899, 1992.

[Guer 92b] P. Gueret, N. Blanc, R. Germann, and H. Rothuizen. *Semiconductor Science and Technology*, Vol. 7, pp. B462 – B464, 1992.

[Hans 07] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen. *Reviews of Modern Physics*, Vol. 79, pp. 1217 – 1265, 2007.

[Hinz 06] J. Hinz, H. Buhmann, M. Schäfer, V. Hock, C. R. Becker, and L. W. Molenkamp. *Semiconductor Science and Technology*, Vol. 21, pp. 501 – 506, 2006.

[Inos 86] T. Inoshita, S. Ohnishi, and A. Oshiyama. *Physical Review Letters*, Vol. 57, pp. 2560 – 2563, 1986.

[Inos 88] T. Inoshita, S. Ohnishi, and A. Oshiyama. *Physical Review B*, Vol. 38, pp. 3733 – 3740, 1988.

[Kell 04] D. Keller. *Optische Eigenschaften ZnSe-basierter zweidiminsionaler Elektronengase und ihre Wechselwirkung mit magnetischen Ionen.* PhD thesis, Julius-Maximilians-Universität Würzburg, 2004.

[Kim 00] M. Kim, C. S. Kim, S. Lee, J. K. Furdyna, and M. Dobrowolska. *Journal of Crystal Growth*, Vol. 214, pp. 325 – 329, 2000.

[Kina 90] W. B. Kinard, M. H. Weichold, and W. P. Kirk. *Journal of Vacuum Science and Technology B*, Vol. 8, pp. 393 – 396, 1990.

[Kita 07a] T. Kita, D. Chiba, Y. Ohno, and H. Ohno. *Applied Physics Letters*, Vol. 91, p. 232101, 2007.

[Kita 07b] T. Kita, D. Chiba, Y. Ohno, and H. Ohno. *Applied Physics Letters*, Vol. 90, p. 062102, 2007.

[Kita 08] T. Kita, D. Chiba, Y. Ohno, and H. Ohno. *Physica E*, Vol. 40, pp. 1930 – 1932, 2008.

[Koen 99] B. Koenig, U. Zehnder, D. R. Yakovlev, W. Ossau, T. Gerhard, M. Keim, A. Waag, and G. Landwehr. *Physical Review B*, Vol. 60, pp. 2653 – 2660, 1999.

[Kouw 01] L. P. Kouwenhoven, D. G. Austing, and S. Tarucha. *Reports on Progress in Physics*, Vol. 64, pp. 701 – 736, 2001.

[Kouw 97] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen. "Electron transport in quantum dots". In: L. L. Sohn, L. P. Kouwenhoven, and G. Schön, Eds., *Mesoscopic Electron Transport*, pp. 105 – 214, Kluwer Academic Press, 1997.

[Kram 10] C. Krammel. *Development of gate-technology based on Si_3N_4.* Bachelor thesis, 2010.

[Krum 73] J. P. Krumme and H. Dimigen. *IEEE Transactions on Magnetics*, Vol. 9, pp. 405 – 408, 1973.

[Kuo 90] Y. Kuo. *Journal of The Electrochemical Society*, Vol. 137, pp. 1235 – 1239, 1990.

[Land 70] A. Landsberg and C. L. Hoatson. *Journal of the Less Common Metals*, Vol. 22, pp. 327 – 339, 1970.

[Land 99] H. H. Landolt and R. Börnstein. *Landolt-Börnstein - Group III: Condensed Matter - Semiconductors*. Springer Verlag, 1999.

[Latu 08] E. Latu-Romain, P. Gilet, P. Noel, J. Garcia, P. Ferret, M. Rosina, G. Feuillet, F. Lvy, and A. Chelnokov. *Nanotechnology*, Vol. 19, p. 345304, 2008.

[Leps 97] M. I. Lepsa. *Two and three terminal double barrier resonant tunneling devices*. PhD thesis, Technische Universiteit Eindhoven, 1997.

[Liu 95] L. Liu, G. Lindauer, W. B. Alexander, and P. H. Holloway. *Journal of Vacuum Science and Technology B*, Vol. 13, pp. 2238 – 2244, 1995.

[Loth 92] J. R. Lothian, F. Ren, and S. J. Pearton. *Semiconductor Science and Technology*, Vol. 7, pp. 1199 – 1210, 1992.

[Lunz 96] U. Lunz, J. Kuhn, F. Goschenhofer, U. Schussler, S. Einfeldt, C. R. Becker, and G. Landwehr. *Journal of Applied Physics*, Vol. 80, p. 6861, 1996.

[Lutw 91] M. I. Lutwyche and D. F. Moore. *Journal of Micromechanics and Microengineering*, Vol. 1, pp. 237 – 246, 1991.

[Mach 74] R. Mach, H. Treptow, and W. Ludwig. *Physica Status Solidi A*, Vol. 25, pp. 567 – 573, 1974.

[Maxi 04] S. Maximov, T. Slobodskyy, A. Grger, F. Lehmann, P. Grabs, L. Hansen, C. R. Becker, C. Gould, G. Schmidt, and L. W. Molenkamp. *Semiconductor Science and Technology*, Vol. 19, pp. 946 – 950, 2004.

[Meir 90] U. Meirav, M. A. Kastner, and S. J. Wind. *Physical Review Letters*, Vol. 65, pp. 771 – 774, 1990.

[Miya 92] T. Miyajima, H. Okuyama, and K. Akimoto. *Japanese Journal of Applied Physics*, Vol. 31, pp. L1743 – L1745, 1992.

[Mizu 95] H. Mizuta and T. Tanoue. *The physics and applications of resonant tunnelling diodes*. Cambridge University Press, 1995.

[Nede 77] D. D. Nedeoglo, D. H. Lam, and A. V. Simashkevich. *Physica Status Solidi A*, Vol. 44, pp. 83 – 89, 1977.

[Nguy 04] P. Nguyen, H. T. Ng, T. Yamada, M. K. Smith, J. Li, J. Han, and M. Meyyappan. *Nano Letters*, Vol. 4, pp. 651 – 657, 2004.

[Oleg 87] D. J. Olego. *Applied Physics Letters*, Vol. 51, pp. 1422 – 1424, 1987.

[Oost 99] T. H. Oosterkamp. *Artificial atoms and molecules: on many body effects and coherence in semiconductor quantum dots*. PhD thesis, Delft University of Technology, the Netherlands, 1999.

[Park 90] Y. C. Park, W. B. Jackson, N. M. Johnson, and Hagstrom. *Journal of Applied Physics*, Vol. 68, pp. 5212 – 5221, 1990.

[Park 93] Y. C. Park, W. B. Jackson, D. L. Smith, and N. M. Johnson. *Journal of Applied Physics*, Vol. 74, pp. 381 – 386, 1993.

[Reed 88] M. A. Reed, J. N. Randall, R. J. Aggarwal, R. J. Matyi, T. M. Moore, and A. E. Wetsel. *Physical Review Letters*, Vol. 60, pp. 535 – 537, 1988.

[Reim 02] S. M. Reimann and M. Manninen. *Review on Modern Physics*, Vol. 74, pp. 1283 – 1342, 2002.

[Ruth 11a] M. Ruth. *A comprehensive study of dilute magnetic semiconductor resonant tunneling diodes*. PhD thesis, Julius-Maximilians-Universität Würzburg, 2011.

[Ruth 11b] M. Ruth, C. Gould, and L. W. Molenkamp. *Physical Review B*, Vol. 83, p. 155408, 2011.

[Samu 82] G. M. Samuelson and K. M. Mar. *Journal of The Electrochemical Society*, Vol. 129, pp. 1773 – 1778, 1982.

[Scha 10] P. Schäfer. *Development of gate-technology based on SiO_2*. Bachelor thesis, 2010.

[Shap 84] Y. Shapira, S. Foner, D. H. Ridgley, K. Dwight, and A. Wold. *Physical Review B*, Vol. 30, pp. 4021 – 4023, 1984.

[Sher 93] M. E. Sherwin, R. Corless, and J. R. Wendt. *Journal of Vacuum Science and Technology B*, Vol. 11, pp. 339 – 340, 1993.

[Sher 94] M. E. Sherwin, J. A. Simmons, T. E. Eiles, N. E. Harff, and J. F. Klem. *Applied Physics Letters*, Vol. 65, pp. 2326 – 2328, 1994.

[Shib 88] N. Shibata, A. Ohki, and A. Katsui. *Journal of Crystal Growth*, Vol. 93, pp. 703 – 707, 1988.

[Simp 94] P. J. Simpson, C. J. B. Ford, D. R. Mace, I. Zailer, M. Yosefin, M. Pepper, J. T. Nicholls, D. A. Ritchie, J. E. F. Frost, M. P. Grimshaw, and G. A. C. Jones. *Surface Science*, Vol. 305, pp. 453 – 459, 1994.

[Slob 03] A. Slobodskyy, C. Gould, T. Slobodskyy, C. R. Becker, G. Schmidt, and L. W. Molenkamp. *Physical Review Letters*, Vol. 90, p. 246601, 2003.

[Smit 96] D. L. Smith and S. M. Kogan. *Physical Review B*, Vol. 54, pp. 10354 – 10357, 1996.

[Some 76] S. Somekh. *Journal of Vacuum Science and Technology*, Vol. 13, pp. 1003 – 1007, 1976.

[Stau 10] F. Staub. *Entwicklung und Optimierung eines Trockentzprozesses zur Herstellung von sub-m Pillar basierend auf ZnSe-Heterostructuren*. Bachelor thesis, 2010.

[Stei 85] C. Steinbrüchel, H. W. Lehmann, and K. Frick. *Journal of The Electrochemical Society*, Vol. 132, pp. 180 – 186, 1985.

[Su 91] B. Su, V. J. Goldman, M. Santos, and M. Shayegan. *Applied Physics Letters*, Vol. 58, pp. 747 – 749, 1991.

[Swan 69] R. K. Swank, M. Aven, and J. Z. Devine. *Journal of Applied Physics*, Vol. 40, pp. 89 – 97, 1969.

[Taru 95] S. Tarucha, D. Austing, and T. Honda. *Superlattices and Microstructures*, Vol. 18, pp. 121 – 130, 1995.

[Taru 96] S. Tarucha, D. G. Austing, and T. Honda. *Physical Review Letters*, Vol. 77, pp. 3613 – 3616, 1996.

[Taru 97] S. Tarucha, D. G. Austing, T. Honda, R. van der Hage, and L. P. Kouwenhoven. *Japanese Journal of Applied Physics*, Vol. 36, pp. 3917 – 3923, 1997.

[Tayl 93] R. P. Taylor, J. A. Adams, M. Davies, P. A. Marshall, and R. Barber. *Journal of Vacuum Science and Technology B*, Vol. 11, pp. 628 – 633, 1993.

[Tewo 92] M. Tewordt, L. Martin-Moreno, V. J. Law, M. J. Kelly, R. Newbury, M. Pepper, D. A. Ritchie, J. E. F. Frost, and G. A. C. Jones. *Physical Review B*, Vol. 46, pp. 3948 – 3952, 1992.

[Thor 86] T. J. Thornton, M. Pepper, H. Ahmed, D. Andrews, and G. J. Davies. *Physical Review Letters*, Vol. 56, pp. 1198 – 1201, 1986.

[Thur 82] G. Thurner, H. Herold, H. Ruder, G. Schlicht, and G. Wunner. *Physical Letters A*, Vol. 89, p. 133 138, 1982.

[Twar 83] A. Twardowski, T. Dietl, and M. Demianiuk. *Solid State Communications*, Vol. 48, pp. 845 – 848, 1983.

[Twar 84] A. Twardowski, M. von Ortenberg, M. Demianiuk, and R. Pauthenet. *Solid State Communications*, Vol. 51, pp. 849 – 852, 1984.

[Tyag 75] M. S. Tyagi and S. N. Arora. *Physica Status Solidi A*, Vol. 32, pp. 165 – 172, 1975.

[Wang 94a] J. Wang, P. H. Benton, N. Mori, H. Buhmann, L. Mansouri, L. Eaves, P. C. Main, T. J. Foster, and M. Henini. *Applied Physics Letters*, Vol. 65, pp. 1124 – 1126, 1994.

[Wang 94b] J. Wang, P. H. Benton, N. Mori, L. Eaves, H. Buhmann, L. Mansouri, P. C. Main, T. J. Foster, and M. Henini. *Physical Review Letters*, Vol. 73, pp. 1146 – 1149, 1994.

[Wata 86] H. Watanabe and T. Inoshita. *Optoelectronics - Devices and Technologies*, Vol. 1, pp. 33 – 39, 1986.

[Wens 09] J. Wensorra, M. I. Lepsa, S. Trellenkamp, J. Moers, K. M. Indlekofer, and H. Lüth. *Nanotechnology*, Vol. 20, p. 465402, 2009.

[Whit 83] L. K. White. *Journal of The Electrochemical Society*, Vol. 130, pp. 1543 – 1548, 1983.

[Will 03] K. R. Williams, K. Gupta, and M. Wasilik. *Journal of Microelectromechanical Systems*, Vol. 12, pp. 761 – 778, 2003.

[Will 96] K. R. Williams and R. S. Muller. *Journal of Microelectromechanical Systems*, Vol. 5, pp. 256 – 269, 1996.

[Wils 86] R. H. Wilson and P. A. Piacente. *Journal of The Electrochemical Society*, Vol. 133, pp. 981 – 984, 1986.

[Yaco 95] A. Yacoby, M. Heiblum, D. Mahalu, and H. Shtrikman. *Physical Review Letters*, Vol. 74, pp. 4047 – 4050, 1995.

[Yoh 98] K. Yoh, H. Kazama, and T. Nakano. *Physica B*, Vol. 249, pp. 243 – 246, 1998.

Acknowledgements

This work and its results have been made possible by the contribution and support of many people.

- First of all I would like to thank Prof. Laurens W. Molenkamp the head of the EP3 for giving me the opportunity to work in his group and for all the discussions, guiding and support.
- Many thanks also to PD Dr. Charles Gould the leader of the spintronics group. His guiding, comments and insight in the scientific world were always fruitful and helped to look as well as think out of the box.
- Many thanks also to Prof. Seigo Tarucha and Akira Oiwa for the helpful and interesting comments on my work and results.
- Many thanks also to Philip Hartmann, Michael Rüth, Stefan Mark, Tobias Bock, Torsten Kloß and Michael Schneider, the members of C114a, for creating a great working environment inside and outside the lab.
- Thanks to Bastian Büttner and Andreas Riegler for having a nice time as lab-mates and helpful discussions about processing.
- Thanks to Alexander Frey for growing the II-VI RTD heterostructures.
- Special thanks to Volkmar Hock for support and interesting discussions during processing in the clean room.
- Special thanks to Tanja Borzenko for helpful insights on electron beam lithography and processing.
- Many thanks to all the people who contributed to discussions, measurement setups etc.: Petra Wolf-Müller, Roland Ebert, Hans, Tobias Kiessling, Claus Schumacher, Martin Zipf and everyone else from EP3.
- I also would like to gratefully acknowledge financial support from the German DFG (Mo771-8).
- Finally, vielen vielen Dank an meine Eltern und die mich mein ganzes Leben immer unterstützt und gefördert haben. Insbesondere auch Danke für das geduldige Zuhören über physikalische Probleme während des Studiums, der Diplomarbeit und der Promotion, auch wenn diese völlig unverständlich erschienen.

- To Katja: Thanks for your great support and patience when the samples were not working and I was spending many hours at the lab. Also special thanks for the support while writing this thesis.